

LISA Phasemeter development

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Abstract. The baseline concept of LISA had been developed within an industrial investigation by Astrium/EADS ([1]) and is being reviewed since 2005 in an ongoing formulation phase. One of the most important key technology development issues remains the demonstration of the interferometric readout of the main science measurement. This includes the hardware development of an appropriate Phase Measurement System (PMS). We present the status of our work concerning the design and implementation of a LISA-like PMS with particular emphasis on the hardware development based on Field Programmable Gate Arrays (FPGA's) as main technology platform and we report on our first results demonstrating the performance of the PMS with synthetic signals.

Keywords: LISA, phase measurement, PLL, FPGA

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INTRODUCTION

LISA measures the path length variation between the free floating proof masses aboard the spacecraft by means of heterodyne interferometry. The primary quantities to be measured by the LISA interferometers are the phases of the sinusoidal beat notes of the heterodyne interferometers coming from photo detectors located on the optical bench. Path length variations of one wavelength ($\approx 1 \mu\text{m}$) translate into a phase variation of the heterodyne signal of one cycle or 2π rad.

Since the relative path length changes need to be measured with a precision of $1 \text{ pm}/\sqrt{\text{Hz}}$ (allocated noise budget for the Phase measurement system (PMS) out of the optical metrology budget of $12 \text{ pm}/\sqrt{\text{Hz}}$ for each single link), the phase of the heterodyne signal needs to be measured with a sensitivity of $1 \mu\text{ cycle}/\sqrt{\text{Hz}}$ or $2\pi \times 10^{-6} \text{ rad}/\sqrt{\text{Hz}}$. The relevant measurement band is the frequency regime from 0.1 mHz to 100 mHz.

Due to the relative spacecraft motion at DC, depending on the orbital dynamics of each spacecraft, the heterodyne frequency gets affected by Doppler shifts of $\pm 10 \text{ MHz}$. This leads to variations of the heterodyne frequency from a few MHz up to 20 MHz. The beat note phase resp. frequency needs to be measured with respect to a system wide reference oscillator (USO) on each spacecraft.

Beside the main science measurement, the phase fluctuations of each USO with respect to those on the other spacecraft need to be measured for the on ground data post-processing performed by Time Delay Interferometry (TDI [2]). This clock noise information will be exchanged between the spacecraft by additional FM sidebands at 2 GHz with 10% of the carrier light power (figure 1)

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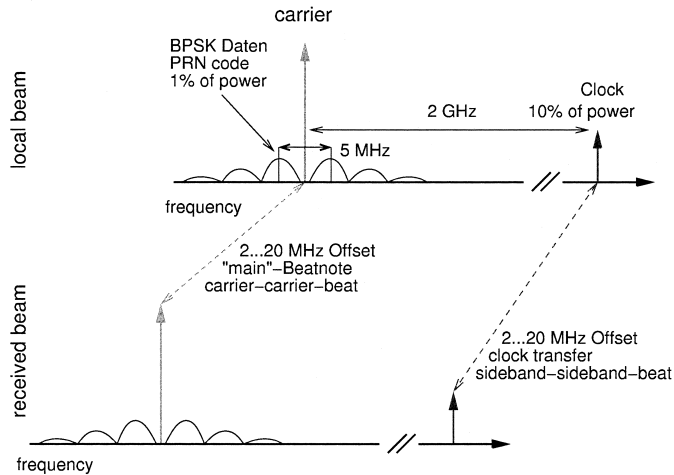


FIGURE 1. Proposed frequency scheme for LISA. Besides the main science carrier the first order FM sidebands contain the information of the USO noise of the independent spacecraft master oscillators. For the inter-spacecraft ranging a pseudo-random noise code sequence provides the length measurement.

Another necessary information for the laser frequency noise subtraction performed by the TDI algorithm is the relative position of the spacecraft with respect to each other. Therefore a GPS-like ranging measurement will be conducted by modulating a pseudo-random noise code with 1% of the carrier light power. This code sequence can also be used to transfer data between the spacecraft.

The LISA phase measurement system needs to provide the following features:

- to measure the relative phase variations between the detected heterodyne signals (carrier-carrier beat) and the local reference oscillator,
- to measure the clock noise between the individual spacecraft-wide master oscillators,
- to demodulate and to decode the pseudo-random noise code sequence for inter-satellite ranging and data transfer.

PHASE MEASUREMENT TECHNIQUES

Different phase measurement techniques are currently under investigation. The zero crossing technique has been demonstrated for a single fixed frequency [3]. This measurement is based on counting fast clock cycles between (e.g. positive) zero crossings of the heterodyne signal (figure 2).

For the LISA precursor mission LISA Pathfinder, a different type of PMS has been successfully implemented. In contrast to the LISA beat signal, the LISA Pathfinder interferometer is operated at a constant heterodyne frequency in the kHz range. A digital two quadrature (I-Q) demodulator has been implemented as phase measurement system. This technique is called SBDFT (Single Bin Discrete Fourier Transform) and the

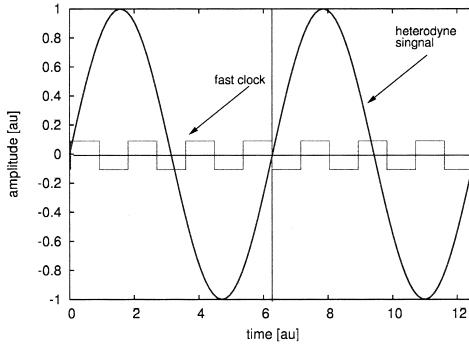


FIGURE 2. Illustration of zero crossing phase measurement technique. A counter counts the clock cycles between e.g. positive zerocrossings of the heterodyne signal.

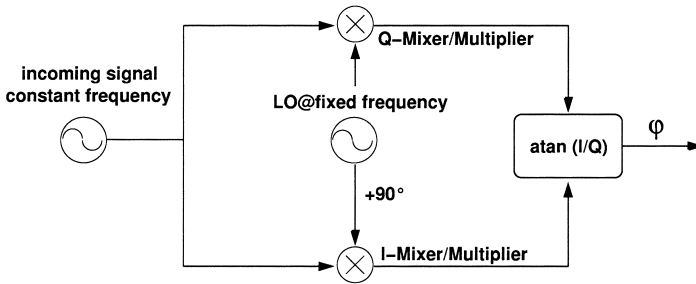


FIGURE 3. I-Q phase demodulation for a signal with constant frequency. A digital version has been implemented for the PMS for LISA Pathfinder. Mathematically this demodulation is equivalent with a DFT (Discrete Fourier Transform) for one frequency.

principle of operation can be seen in figure 3 ([4, 5]). In order to obtain a phase φ , the signal sampled by an ADC (represented as x_i) will be multiplied with both quadratures of the local oscillator of the same frequency and added up over the length of the DFT N :

$$\Re(F) = \sum_{i=0}^{N-1} x_i \cdot c_i \quad ; \quad \Im(F) = \sum_{i=0}^{N-1} x_i \cdot s_i, \quad (1)$$

where $c_i = \cos(\frac{2\pi i k}{N})$ and $s_i = \sin(\frac{2\pi i k}{N})$. (This corresponds to picking the single frequency bin 'k' out of a full discrete fourier transform (DFT) result).

Due to the frequency drift occurring to the LISA beat notes, a slightly modified PMS system will be necessary where the frequency of the local oscillator can be locked to the frequency of the heterodyne signal. Therefore, an additional PLL that tracks the incoming frequency will be implemented into the LISA Pathfinder demodulation scheme.

The frequency or phase measurement can be derived from the local oscillator feedback signal (φ_1 in figure 4). In order to measure phase noise outside the bandwidth of the

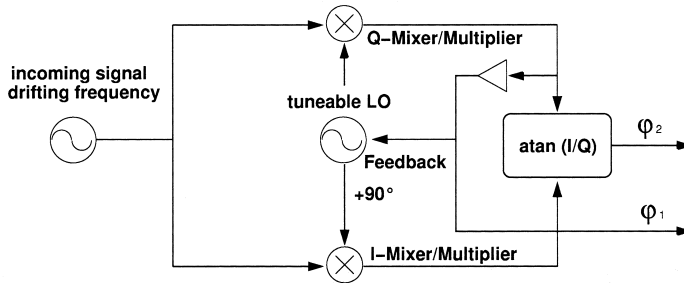


FIGURE 4. I-Q phase demodulation for a signal with drifting frequency that will be tracked by a PLL loop.

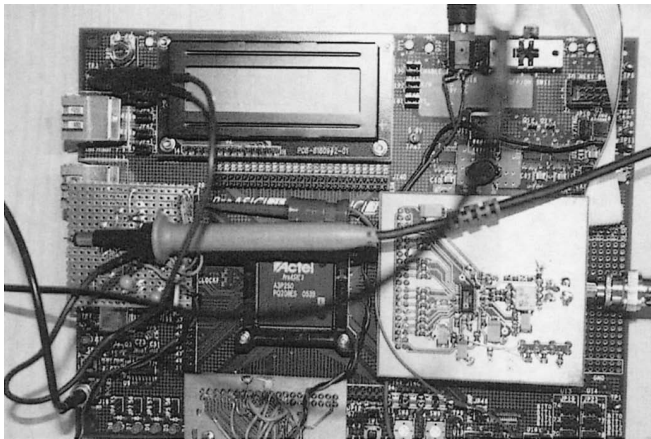


FIGURE 5. First prototype based on a FPGA Evaluation Kit and additional electronics (e.g. ADC) has been implemented for study purposes.

PLL or to measure residual noise within its bandwidth, the I-Q demodulation can be processed as implemented in the LISA Pathfinder PMS (φ_2 in figure 4).

HARDWARE IMPLEMENTATION

The platform that has been chosen for the hardware implementation of the phasemeter core is based on reprogrammable logic. For our purposes, an FPGA seemed to be the most suitable choice. For the prototype design, an Actel A3P250 with 250 kGates running at 80MHz has been used (see figure 5). The digitization of the incoming beat note with a frequency between 2 and 20MHz drifting with up to 4Hz/s is provided by a 12 bit AD converter (AD9236) running at 80MHz. The resolution of the ADC has been reduced to 8 bit to simulate available space qualified ADC's at these frequencies.

The digitized heterodyne signal is mixed in a 8x8 bit digital multiplier with the

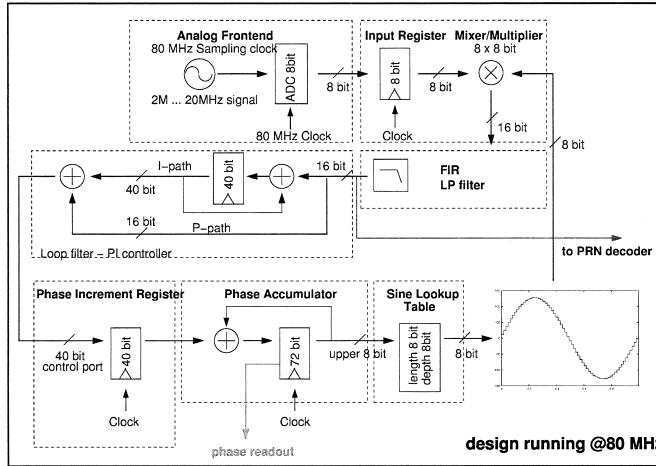


FIGURE 6. Overview of the PLL core that consists mainly of an all digital phase lock loop (ADPLL) and has been implemented on an Actel FPGA. The design has been tested at 80MHz system clock.

synthesized sine wave generated by a Direct Digital Synthesis (DDS) system. The DDS consists of a 72 bit accumulator with a 40 bit phase increment register which is the core of the DDS. The 8 most significant bits (MSB's) of the accumulator are connected to a 256 element sine table with a precision of 8 bit. The whole design is synchronously driven with the same 80MHz clock that drives the ADC frontend. For further processing, a 90 degree phase shifted DDS provides the second quadrature of the heterodyne signal. Currently the phase is reconstructed from the phase increment register (PIR) of the DDS. An appropriate low pass filter removes the higher frequency terms. The filtered error signal is fed back to the phase increment register (PIR) of the DDS via a standard proportional-integral (PI) controller with a transfer function:

$$G_F(\omega) = G_p + \frac{G_i}{i\omega}, \quad (2)$$

with a cutoff frequency of $f_c = \frac{G_i}{G_p}$. Figure 7 shows the simulated Open Loop Gain of the digital PLL. The unity gain frequency is in the order of about 100 Hz.

PRELIMINARY RESULTS

In order to test the synthetic performance of this implementation, a second independent DDS system synthesizes a signal of constant frequency at 20MHz. This DDS has been implemented in the same FPGA, acting as a simulated input signal, whilst the local oscillator (LO) starts with 5kHz to investigate lock acquisition behavior. After the LO has been locked to the 20MHz input signal, its phase noise has been measured. The aim of this test is to verify the expected performance of the ADPLL. The results can be seen in figure 8.

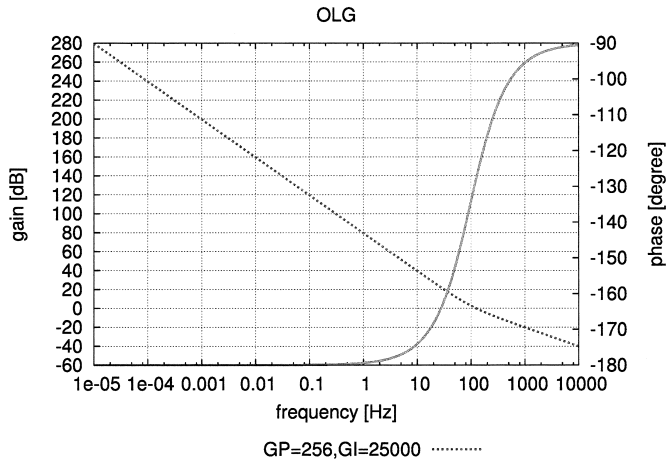


FIGURE 7. Open loop gain of the ADPLL.

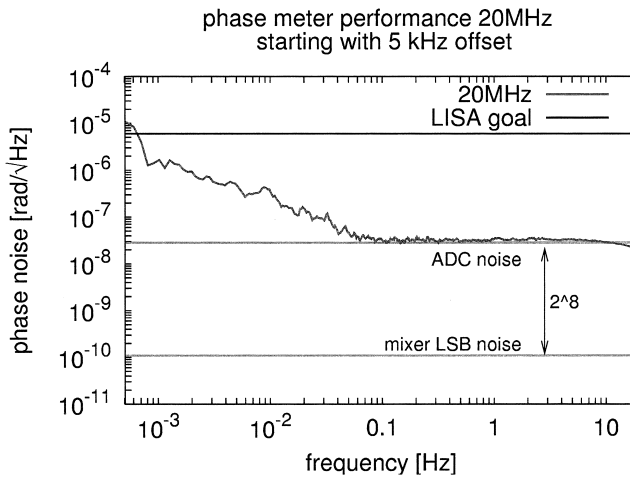


FIGURE 8. Synthetic noise performance of the PMS with an internal generated 20MHz reference signal representing the heterodyne signal. The noise floor is dominated by the digitization noise induced by the 8 bit sine look-up table generating the signals. The origin of the increasing noise level at low frequencies is currently under investigation. A first test indicates errors in the data transfer via the enhanced parallel port (EPP) to the floating point processor.

In order to perform a more realistic measurement, and to test the hardware including the ADC, a function generator running at 20 MHz has been utilized as reference signal instead of the second DDS system. Its output has been sampled by the ADC frontend of the PMS prototype, and the internal reference oscillator of the signal generator has been locked to the 80 MHz PMS system clock. The result of the test can be seen in figure 9

Currently, a new hardware design has been implemented and is under testing. Its

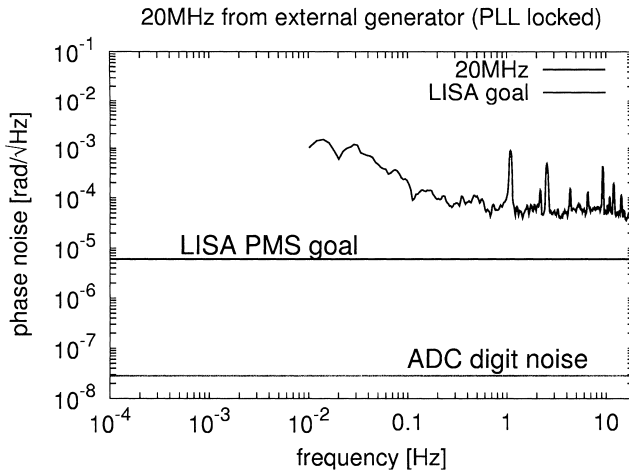


FIGURE 9. Result of the noise performance test of the ADPLL

TABLE 1. List of components used on the new prototype PMS board

Component	type	specification	intended purpose
AD converter	AD9446	16 bit @ 125 MHz max.	frontend, digitization of photodiode output
DA converter	AD9744	14 bit @ 210 MHz max.	DA conversion of feedback signals for Nd:YAG laser stabilization
EPP interface		output rate 1 MBit max	transfer phase data intermediate integer results at appr. 100 Hz to floating point hardware, send RAM data to the PMS board for configuration
RAM	TI	1 Mword with 16 bit wordsize, 6 ns access time	store data e.g. sinetable or IIR/FIR*filter coefficients

* infinite impulse response/finite impulse response

main components and features are listed in table 1. The AD conversion of the new PMS board will be realized by a 16 bit ADC whereas 8 bit are effectively used (the extended resolutions can be used for diagnostic purposes). The maximum sampling frequency is 125 MHz, but it is currently running at 80MHz. These design restrictions have been taken, due to the availability of space qualifiable components. Since the PMS needs to perform the frequency offset phase lock of the LISA lasers, two 14 bit DAC's are foreseen to control the piezo electric transducer (PZT) and crystal temperature frequency actuators of the laser. A dedicated RAM is provided to store sets of IIR/FIR¹ filter

¹ infinite impulse response/finite impulse response

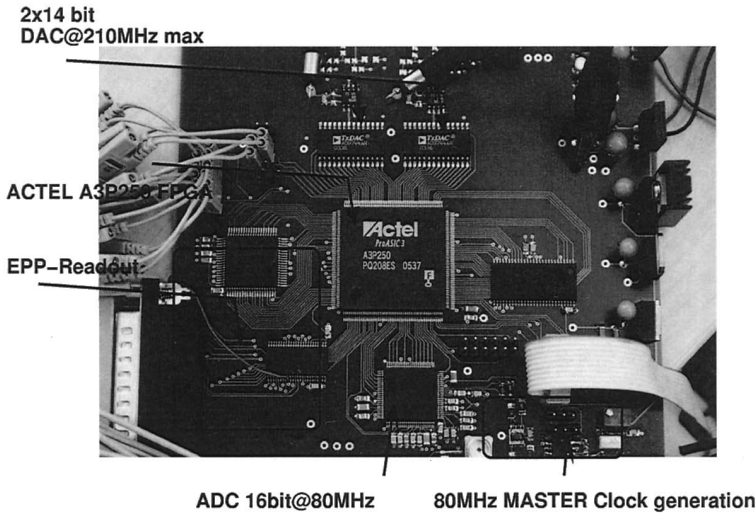


FIGURE 10. The figure shows the implemented hardware of the LISA PMS prototype, which is under test now and is the first of several prototypes to be built during the prototyping process.

coefficients and/or sine tables. An enhanced parallel port (EPP) implementation, including a dedicated FIFO, is the interface to transfer data between the PMS board and a floating point DSP (e.g. a standard of the shelf PC).

CONCLUSION

We have presented the status and first results of our activities concerning the LISA PMS hardware development. Our hardware prototype based on a commercial FPGA Evaluation Kit has been implemented and tested. The synthetic performance has been measured and meets the requirement of $2\pi \times 10^{-6} \text{ rad}/\sqrt{\text{Hz}}$ allocated for the phase readout, even in the presence of technical noise. A test with more realistic signals has been shown. Furthermore, our own hardware implementation of a PMS prototype has begun.

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