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Abstract

In this paper we propose a structure dependent method for the systematic design of self-checking error detection circuits which is well adapted to the technical fault model considered. For on- line detection,the hardware is in normal operation mode,and for testing in test mode.In the test mode,these error detection circuits guarantee a 100 % fault coverage for single stuck-at-0/1 faults and a high fault coverage for arbitrary faults.

1 Introduction

Different design for testability methods, and methods for on-line error detection are investigated world-wide. Test methods can be divided into structure independent,and structure dependent methods.In the case of structure independent methods,linear shift registers are often used to generate pseudorandom inputs for the circuit under test, and to compress the outputs of the circuit [Fr 77]. In the case of structure dependent methods, weighted pseudorandom inputs and special circuits for data compression are used. This approach, for example is applied to the testing of PLAs [Ag 86]. In another structure dependent method, the test set of a given circuit is deterministically generated by either a non-linear shift register [Da 83], a controlled counter [Wa 88], or a more general automaton [Wa 90]. An interesting modification of a structure independent method into a structure dependent method for the testing of a multiple-output combinational circuit was recently proposed in [ZA 90].

On the other hand the systematic design of an optimal error detection circuit for a circuit with an arbitrarily given functional error model was described in [GG 87,Go 91].Every fault in the considered fault model of the monitored circuit is detected immediately after affecting the output of the monitored automaton if the checker does not fail.

However,some faults of the checker may remain undedected.

In [Se 79] it was proposed that the methods of on-line error detection by duplication and comparison, and testing be combined to use the same hardware, but in different operational modes. For on-line detection, the hardware is set in normal operation mode, and for testing, in test mode. These ideas were further developed in [Fu 84, RF 89] and in [So 88]. In [Fu 84] it is shown, how for an arbitrary prediction function, a self-checking error detection circuit can be designed which may also be used for exhaustive testing in its test mode. But the method is not adapted to the special structure of the monitored circuit or to specific physical faults. In [So 88], the independent outputs of the monitored combinational circuit are added modulo 2 and only this modified circuit is duplicated, inverted, and compared with the original circuit in normal operation mode and in test mode.

But till now for random logic there do not exist systematic built-in self-test methods which are optimally adapted to the fault model and which guarantee, with reasonable costs, a 100% fault coverage for the technical fault model considered. This is true even for the simple stuck-at-0/1 fault model.

As a generalization of [So 88], we propose in this paper a structure dependent method for the systematic design of self- checking error detection circuits which is well adapted to the fault model considered.In the test mode, these error detection circuits guarantee a 100% fault coverage for the single stuck-at- 0/1 faults and also provides high fault coverage for other fault models. Instead of the independent outputs in [So 88] in this paper, weakly independent outputs of the monitored circuit are summed modulo 2. Two outputs are weakly independent with respect to a given fault if there exists an input such that in the presence of the fault considered, only one of the outputs is erroneous.

2 Basic notions and notations

In this section we introduce the basic notations "functional error model", "weakly independent outputs", and "complete set of weakly independent outputs" with respect to a given functional error model.

We consider a combinational circuit f_c implementing a function f, f : X----> Y with $X = \{0,1\}^m$, $Y = \{0,1\}^n$ and $f = (f^1,...,f^n)$, where f^i:X--->{0,1}, i=1,...,n are m-ary Boolean functions.

Physical faults $\phi_1,...,\phi_K$ such as shortage to ground of one or more lines, shortage of one or of more lines to power supply,broken lines,bridging between lines, and others are modelled by a functional error model.

A functional error model F(f) of a circuit f_c,which implements the function f with the faults $\phi_1,...,\phi_K$, is a set of functions

$F(f) = \{f(0)=f,f(1),...,f(K)\}$, $f(i):X \dashrightarrow Y,i=1,...,K.$ (1)

The function f(i), i = 1,..., K of the error model is the function which f_C implements instead of f(0) = f if the fault ϕ_i occurs [GG 87].

To explain this notion we consider the AND-gate of Fig. 1. The input and the output lines of the AND-gate are numbered from 1 to 3. The following faults are considered:

ϕ_1:input line 1 is stuck-at-1

ϕ_2:input line 2 is stuck-at-1

ϕ_3:output line 3 is stuck-at 1

ϕ_4:input line 1 is stuck-at-0

ϕ_5:input line 2 is stuck-at-0,

ϕ_6:output line 3 is stuck-at-0.

If line 1 is fixed at 1,(ϕ_1), the faulty AND-gate implements the error function $f(1) =1 \wedge x_2 = x_2$. If the line 2 is stuck-at-1, (ϕ_2), the error function $f(2) = x_1 \wedge 1 = x_1$ is implemented. In case of ϕ_3 the error function f(3) = 1 is caused by a stuck-at-1 fault of line 3.

Thus the functional error model $F_1(x_1 \wedge x_2) = \{x_1 \wedge x_2,x_2,x_1,1 \}$ functionally models the stuck-at-1 faults ϕ_1, ϕ_2, ϕ_3, that is, all stuck-at-1 faults of a single line.

If one of the lines 1,2 or 3 is stuck-at-0, (ϕ_4, ϕ_5, ϕ_6), the faulty AND-gate of Fig. 1 implements the function f(4) = f(5) = f(6) = 0. If we assume that both stuck-at-1 and stuck-at-0 faults may occur, the corresponding functional error model is

$F_{0,1}(x_1 \wedge x_2) = \{x_1 \wedge x_2,x_1,x_2,0,1\}$. (2)

If multiple stuck-at-0/1 faults of the AND-gate are also considered no new error functions have to be added to the functional error model given by (2).

To illustrate the ability to describe bridging faults, Fig. 2 shows a 3-input AND-gate implementing the function $f(x_1,x_2,x_3) = x_1 \wedge x_2 \wedge x_3$.

Let ϕ_1 be a bridging fault between line 1 and line 2. If bridging between lines can be modelled by a "wired OR" then the corresponding error function f(1) is

$f(1) = (x_1 \vee x_2) \wedge x_3$.

The other error functions for the bridging faults ϕ_2 (lines 1, 3), ϕ_3 (lines 2,3), and ϕ_4 (lines 1,2,3) are $f(2) = (x_1 \vee x_3) \wedge x_2$, $f(3) = x_1 \wedge (x_2 \vee x_3)$, and $f(4) = x_1 \vee x_2 \vee x_3$ respectively.

If ϕ_5, ϕ_6, ϕ_7 are the respective bridging faults between input line 1 and output line 4, input line 2 and output line 4, and input line 3 and output line 4, the corresponding error functions are $f(5) = (x_1 \wedge x_2 \wedge x_3) \vee x_1 = x_1$, $f(6) = (x_1 \wedge x_2 \wedge x_3) \vee x_2 = x_2$, $f(7) = (x_1 \wedge x_2 \wedge x_3) \vee x_3 = x_3$, resp.

Thus the functional error model $F_{brid}(f)$ caused by bridging faults is

$F_{brid}(f) = \{ x_1 \wedge x_2 \wedge x_3, (x_1 \vee x_2) \wedge x_3, (x_1 \vee x_3) \wedge x_2, x_1 \wedge (x_2 \vee x_3)\ x_1 \vee x_2 \vee x_3, x_1, x_2, x_3 \}$.

(3)

Physical faults sometimes cause combinational circuits to become sequential or to result in oscillating behaviour.

In this paper we assume that physical faults may be described by a functional error model consisting of a set of combinational functions.

We now introduce the concept of weakly independent outputs as a generalization of the notion of independent outputs. Outputs of a circuit usualy are called independent, if they are implemented without any common gates.

If a single fault concerning only a single gate occurs at most one of the independent outputs of a circuit may be erroneous. This is true for abitrary inputs. The modulo-2-sum of a group of independent outputs will be erroneous if the fault considered changes one of this outputs. The concept of weakly independent outputs with respect to an error function f(k) corresponding to a physical fault ϕ_k is introduced by definition 1.

Definition 1. Let $J(r) = \{j_1,...,j_r\}, r \in n$, be a set of r outputs of the circuit f_c. Then $j_1,...,j_r$ are weakly independent outputs with respect to $f(k) \in F(f)$, if there exists an $x_k \in X$ such that

$$f^{j1}(x_k) \oplus f^{j2}(x_k) \oplus .... \oplus f^{jr}(x_k) \neq f^{j1}(k;x_k) \oplus f^{j2}(k;x_k) \oplus ... \oplus f^{jr}(k;x_k). \tag{4}$$

The condition given by (4) is satisfied if the number of values $f^{ji}(k;x_k)$ different from $f^{ji}(x_k)$ is odd for at least one input x_k.

For $r = 2$, two outputs j_1 and j_2 are weakly independent with respect to f(k) if there exists an $x_k \in X$ such that either $f^{j1}(k;x_k) \neq f^{j1}(x_k)$, or $f^{j2}(k,x_k) \neq f^{j2}(x_k)$, but not both (or if $f^{ji} = f^{ji}(k)$).

Independent outputs are weakly independent with respect to faults concerning only single gates.

Definition 2. The outputs $j_1,..., j_r$, $1 < r \leq n$ of a circuit f_c are weakly independent with respect to a subset $F'(f) \subseteq F(f)$ of the error model if they are weakly independent with respect to every function f(k) of the subset F'(f).

We now consider different sets of outputs $J_1, J_2,..., J_L$ of the circuit f_c which are weakly independent with respect to the subsets $F'_1(f), F'_2(f),..., F'_L(f)$ of the error model F(f).

Definition 3. Let $F'_1(f)$, $F'_2(f),\dots,$ $F'_L(f)$ with $F'_i(f) \subseteq F(f)$ be subsets of the functional error model $F(f)$ and let $J_1,\dots,J_L$ be subsets of outputs of the circuit f_c which are weakly independent with respect to $F'_1(f),\dots, F'_L(f)$ respectively. Then $\{J_1,\dots, J_L\}$ is a complete set of weakly independent subsets of the outputs of f_c with respect to the error model $F(f)$ if

$$F(f) = F'_1(f) \cup F'_2(f) \cup \dots \cup F'_L(f) . \qquad (5)$$

Remarks. Because of (5) every error function $f(k) \in F(f)$ is contained in at least one of the subsets $F'_i(f)$, $i= 1,\dots, L$.

In (5) we have not assumed

$$F'_i(f) \cap F'_j(f) = \emptyset, \qquad \text{for } i \neq j. \qquad (6)$$

Now to every error function $f(k) \in F(f)$ and to every subset $i_1, \dots, i_l$ of outputs a subset of inputs $X(i_1, \dots, i_l, k) \subseteq X$ is assigned for which an odd number of these outputs is erroneous due to the fault ϕ_k corresponding to the error function $f(k)$.
If this set is not empty the outputs $i_1, \dots, i_l$ are weakly independent with respect to $f(k)$.
For every single output i, $0 < i \leq n$, and for a fault ϕ_k the subset $X(i;k)$ is given by

$$X(i;k) = \{ x \mid f'(x) \neq f'(k;x) \}. \qquad (7)$$

$X(i;k)$ is the set of inputs for which the i-th output of f_c implementing the error function $f(k)$ in case of fault ϕ_k, differs from the i-th output of the standard function f.
If $X(i;k) \neq \emptyset$ then the fault ϕ_k which causes f_c to implement $f(k)$ instead of f, is testable.
We assume here that every fault ϕ_k , $k \in \{ 1, \dots, K\}$ is testable.
We denote $\overline{X}(i;k) = X \setminus X(i;k)$.
Then for $x' \in \overline{X}(i;k)$ we have $f'(x') = f'(k;x')$.
Since $X(i_1,i_2,\dots,i_l;k) \subseteq X$ is the subset of inputs for which an odd number of values of $f^{i1}(k),f^{i2}(k),\dots,f^{il}(k)$ is erroneous we have

$$\begin{aligned}
&X(i_1,i_2;k) = X(i_1;k) \cap \overline{X}(i_2;k) \cup \overline{X}(i_1;k) \cap X(i_2,k)\\
&X(i_1,i_2,i_3;k) = X(i_1;k) \cap \overline{X}(i_2;k) \cup \overline{X}(i_3;k) \cup\\
&\qquad X(i_1;k) \cap X(i_2;k) \cap \overline{X}(i_3;k) \cup\\
&\qquad \overline{X}(i_1;k) \cap \overline{X}(i_2;k) \cap X(i_3;k) \cup\\
&\qquad X(i_1;k) \cap X(i_2;k) \cap X(i_3;k), \qquad (8)
\end{aligned}$$

. . .

and $X(i_1, \dots, i_l, k)$ can be computed from $X(i_j;k)$ and $\overline{X}(i_j;k)$, $j = 1, \dots, l$, resp.

$X(i_1,...,i_l;k) \neq \emptyset$ implies that the outputs $i_1,..., i_l$ are weakly independent with respect to the error function f(k) which corresponds to the physical fault ϕ_k.

For a subset F_j of F(f) the outputs $i_1, ..., i_l$ are weakly independent with respect to this subset if for all $f(k) \in F_j'$ the set $X(i_1,...,i_l;k)$ is not empty.
Thus the computation of $X(i_1,...,i_l;k)$ allows us to decide whether the outputs $i_1, ..., i_l$ are weakly independent with respect to f(k) or F_j' or not. Practically this is possible for very small examples only. A heuristik method for the determination of complete groups of weakly independent outputs is described later on.

3 Self-checking and self-testing circuits by use of weakly independent outputs

Fig 3. shows the basic design of a self-checking and self-testing circuit based on the concept of weakly independent outputs. This method is well-adapted to the error model F(f) of the tested circuit which is determined by the physical faults under consideration.
Let $J = \{J_1,J_2,...,J_K\}$ with
$J_i = \{ j_{i,1}...j_{i,ri}\}$, i= 1,...,K (9)
be a complete set of weakly independent outputs of the circuit f_c with respect to the error model F(f).Then for i=1,...,K the outputs $j_{i,1},...j_{i,ri}$ of the set J_i are summed modulo 2 as shown in Fig. 3. In the fault free case we have for i = 1,...,K

$$z_i(x) = f^{ji,1}(x) \oplus f^{ji,2}(x) \oplus ... \oplus f^{ji,ri}(x).$$

The additional circuit g_c implements the K functions $z_1'(x) = \overline{z_1}(x)$, ..., $z_K'(x) = \overline{z_K}(x)$ which are compared with $z_1(x),...,z_K(x)$ by use of a self-checking comparator SCC.
Depending on the control signal on the multiplexer MUX, the circuit is in either test mode, or normal operation mode. In the test mode the test input generator TIG inputs the test signals simultaneously to f_c and g_c. If we assume that the test input generator TIG generates an exhaustive test, then

- every fault ϕ_k of f_c corresponding to an error function $f(k) \in F(f)$, $f(k) \neq f$,
- every fault ϕ'_l of g_c which changes g into g(l) with $g(l) \neq g$,and
- every single stuck-at-0/1 fault of the self-checking comparator SCC,is detected if all possible correct input combinations are applied to the SCC. In general we do not specify whether the TIG generates an exhaustive, a pseudorandom, a weighted pseudorandom, or a deterministic test. For more specific fault models more specific results may be obtained.

In normal operation mode, all single faults are detected when they affect the outputs of f_c,g_c or SCC for the first time.

4 100% fault coverage for stuck-at-0/1 faults

In this section we assume that only single stuck-at-0/1 faults occur and that the weakly independent outputs of f_c are determined according to this fault model.

For the case of single stuck-at-0/1 faults we show that a 100% fault coverage can be achieved by the method proposed. Thereby we assume that both the circuits f_c and g_c are testable with respect to every single stuck-at-0/1 fault. The transformation of an arbitrary circuit into a circuit testable with rerspect to every single stuck-at-0/1 fault is described in [SM 77].

A direct testable implementation of a Boolean function f^1 or a tupel of Boolean functions f= $(f^1,...,f^K)$ can be achieved by use of irredundant representations of f^i by prime implicants [Le89,SL90].

We do not go into details here but assume that both f_c and g_c are testable with respect to all single stuck-at-0/1 faults.

If the TIG generates an exhaustive test, all single stuck-at-0/1 faults of f_c and g_c are detected in the test mode.

We now discuss the detection of all single stuck-at-0/1 faults of the SCC. A well known SCC with 2x2 = 4 inputs and 1x2 = 2 outputs described in [CS 68] is shown in Fig. 4. Possible fault free inputs are 0101,0110,1001,and 1010. Fault free outputs are 01,and 10. All single stuck-at-0/1 faults are only detected if all the four possible fault free inputs are actually applied to the SCC. If only a subset of these inputs occurs, then according to [KR 90] the situation can be improved by including two delay elements on two of the input lines of the SCC as shown in Fig. 5. Let us suppose that only the fault free inputs 0101 and 1010 are applied to the original SCC. Then due to the delay elements all of the four fault free inputs occur as inputs to the modified SCC given in Fig.5. If we assume that none of the input lines of the original SCC are constant over all time, then by use of this method, all possible input combinations occur as inputs of the modified SCC and all single stuck-at-0/1 faults of the SCC will be detected during normal operation.

A SCC with more than four inputs can be implemented in the usual manner as a tree of SCCs with four inputs and two outputs. Thus we have shown that a 100% fault coverage of all single stuck-at-0/1 faults can be in priciple achieved by the described method.

Another possible SCC with only one output was proposed in [So 81]. This SCC is shown in Fig. 6. An additional input x_0 , $x_0 \in \{ 0, 1 \}$ changes its value to its opposite value every time-cycle. For the inputs $(a_i,a'_i) \in \{01,10\}$, the outputs of all the XOR-gates which are directly connected to the inputs a'_i,i=1,..., n, are equal to $\overline{x_0}$ as long as no fault occurs. All multiple stuck-at-0/1 faults of the XOR- gates are detected during normal operation with the exception of a stuck-at-1 fault on the direct output of the SCC which is true even if not all possible fault free inputs are applied to the SCC. If only none of the input lines of the SCC is constant then all the stuck-at-0/1 faults will be detected. Since only the stuck-at-0 faults on the inputs of the AND-gate and the stuck-at-1 faults of the NOR-gate can be detected during normal operation these AND- and NOR-gates are redundantely designed. The time-delay of this checker is independent on the number of its 2n+1 inputs where the number of internal signal lines is n.

In normal operation mode every single stuck-at-0/1 fault is immediately detected the first time if it influences the outputs of f_c, g_c, or the SCC resp.

5 Fault coverage for arbitrary faults

The circuit of Fig. 3 was designed to detect the faults of a specific fault model and is well-suited to this special purpose. Regardless of this fact we now suppose that due to arbitrary faults (not necessarily from the fault model considered till now), the outputs of f_c as well as the outputs of g_c are arbitrarily erroneous with equal probability.

We suppose that the TIG generates an m-dimensional input sequence of length l. Then the circuit f_c outputs an n-dimensional output sequence of length l which is transformed by modulo 2 additions of the corresponding weakly independent outputs into an K-dimensional sequence of length l. The circuit g_c also outputs an K-dimensional output sequence of length l. We now assume that due to an arbitrary fault, each of the principally possible 2^{2Kl} output sequences of lenght l occurs with equal probability. One of these sequences is correct, and $2^{2Kl} - 1$ sequences are erroneous. Among the 2^{2Kl} sequences are 2^{Kl} sequences for wich we have $z'_i = \overline{z_i}$, i = 1,..., K for the entire length l of the sequence considered. One of these sequences is the correct one,and $2^{KI}- 1$ of them are erroneous, but they can not be detected as erroneous by the circuit of Fig. 3. Thus $2^{Kl} -1$ of the $2^{2Kl} - 1$ erroneous sequences can not be detected as erroneous, and the probability of not detecting an arbitrarily erroneous sequence of the length l due to an arbitrary fault is

$$p = \frac{2^{kl} - 1}{2^{2kl} - 1} \approx \frac{1}{2^{kl}} \qquad (10)$$

Since the circuit f_c has m binary inputs the lenght l (for an exhausive test) is of the order of 2^m. For $m = 8$ and $K = 2$ we have $p \approx 1/2^{512}$, and for $m = 10$ and $K = 2$, $p \approx 1/2^{2048}$.

K is the number of different sets of weakly independent outputs of f_c. Thus the fault coverage of the proposed method for arbitrary faults is as good as for the method described in [ZA90].

Under the assumption that all output sequences occur with equal probability the proposed method provides much better fault coverage then in signature analysis. Applying signature analysis using a signature register with r Flip-Flop elements it is only possible to achieve $p = 2^{-r}$. In signature analysis this result is independent on the test length.

6 An heuristic method for the determination of groups of weakly independent outputs

Groups of weakly independent outputs can be determined by hardware simulation of the circuit f_c and fault injection of the faults from the fault model considered.

Since the problem of determing "optimal groups" of weakly independent outputs is of large complexity, heuristic methods must be used. One possible heuristic solution will now be described.

Let f_c be the circuit implementing the n-tupel of m-ary Boolean functions $f = (f^1,..., f^n)$ and let $F(f) = \{ f(0) = f(1),..., f(K) \}$ be the functinal error model as previously described.

Then for the first set $J_1(n)$ of weakly independent outputs, we choose the set $J_1(n) = \{1,..., n \}$ of all outputs of f_c .

According to the proposed method, all the outputs of $J_1(n)$, that is all the outputs of f_c, are added modulo 2 to form z_1, i.e. the parity bit. $J_1(n)$ is weakly independent with respect to all error functions $f(j)$, $f(j) \in F(j)$, for wich there exists an input x_j, $x_j \in X$, such that $f(j;x_j)$ is erroneous at an odd number of outputs.

Let $F_{odd}(f)$ be the set of these functions wich are erroneous at an odd number of outputs for at least one input. Then we remove these functions from F(f) and we compute

$$F_{even}(f) = F(f) \setminus F_{odd}(f) .$$

The set $F_{even}(f) = \{ f_{even,1}, ..., f_{even,L} \}$ consists of all functions of the error model which for all inputs are erroneous only at an even number of outputs of f_c. Practically, $F_{even}(f)$ is a relatively small set of error functions.

For every function $f_{even,k} \in F_{even}(f)$ we fix an input x_k such that for at least one $j \in \{1,..., n\}$ we have $f_{even,k}{}^j(x_k) \neq f^j(x_k)$.
If the circuit f_c implements $f_{even,k}$ and the input x_k is submitted then at least the j-th output of f_c is erroneous.

We define an (L; n)-matrix $T = (T_{k,l})$, $k= 1, ...,L$; $l = 1, ...,n$ by

$$T_{k,l} = \begin{cases} 1 & \text{if} \quad f_{even,k}{}^l(x_k) \neq f^l(x_k) \\ 0 & \text{otherwise} \end{cases}$$

$T_{k,l}$ equals 1 if the l-th output of f_c is erroneous due to the implementation of the error function $f_{even,k}$ when input x_k is applied to f_c. For every column l, l = 1, ..., n, corresponding to the l-th output of f_c, we count the number of 1's.

This number of 1's is the number of error functions $f_{even,k} \in F_{even}(f)$ with erroneous output l if the previously fixed inputs x_k, k = 1, ..., L, are applied.

From the till now unmarked columns of T we choose the one with maximal value and mark this column by *. If more than one column has the maximal value, then one of these columns is arbitrarily choosen.
Let r be this column. Then all rows j of T for which $T_{j,r} = 1$ are also marked by *. These rows correspond to the error functions $f_{even,j}$, which under input x_j are erroneous at output r. These errors are detected by observing output r.
Let j be a row of T marked by *. Then all columns m of T, $m \neq r$, for which $T_{j,m} = 1$ are marked by +.
Let m' be a column marked by +. Then we have $T_{j,m'} = 1$ and $T_{j,r} = 1$ and the outputs m' and r are simultaneously erroneous under input x_j if the error function $f_{even,j}$ is implemented by f_c. Therefore the outputs r and m' should not be added modulo 2.
Generally outputs corresponding to columns of T marked by + should not be added modulo 2 to outputs marked by *.
Now all the rows marked by * are deleted from T. The described procedure is repeated until all the columns are marked by either * or +. The columns marked by * correspond to a group of weakly independent outputs $\{ i_{1,1}, ..., i_{1,r1} \} = J_2$ and are added modulo 2.
The columns of T marked by * and the rows of T marked by * are deleted from T.
Next the markings + are deleted and the described procedure is again applaid to determine the next group of weakly independent outputs $\{ i_{2,1}, ..., i_{2,r2} \} = J_3$, ... until all the rows have been removed from T.
Fig. 7 shows the corresponding self-checking and self-testing combinational circuit with M+1 groups of weakly independent outputs.

The values $z_1, z_2, ..., z_M$ correspond to the modulo 2 sum of the groups of weakly independent outputs $J_1, J_2, ..., J_M$.

Since $J_2, ..., J_M$ are mutually disjoint z_1 can be computed by the modulo 2 sum of $z_2, ..., z_M$ and all the additional outputs not contained in $J_2, ..., J_M$. Thus the computation of $z_1, z_2, ..., z_M$ needs exactly as many XOR-gates as the computation of the parity z_1 of the outputs of f_c.

7 Examples

As a first example, we consider here the design of a self-testing and self-checking one-bit-adder A. The adder is shown in Fig. 8. For the sum bit s we have $s = a \oplus b \oplus c_-$ and for the carry out c_+ : $c_+ = a \wedge b \vee (a \oplus b) \wedge c_-$, whereas a and b are the operands and c_- denotes the carry-in.

We assume that only single stuck-at-0/1 faults can occur. In Fig.8 the gates of A are numbered from 1 to 5. Faults of gate 2 can only influence output 1; and faults of gates 3,4 and 5 can only influence output 2. Gate 1 is the only gate where faults can act on both outputs 1 and 2. To show that outputs 1 and 2 are weakly independent with respect to all stuck-at-0/1 faults of all the gates of A, we only have to show that the outputs 1 and 2 are weakly independent with respect to the 6 stuck-at-0/1-faults $\phi_{10}, \phi_{11}, \phi_{20}, \phi_{21}, \phi_{30}$, and ϕ_{31} of lines 1, 2 and 3 of gate 1, where ϕ_{ij} denotes that line i is stuck-at-j, $i \in \{1,2,3\}, j \in \{0,1\}$.

Then we have

$X(1; \phi_{10}) = \{abc_- = 100,101,110,111\}$

$\overline{X}(1; \phi_{10}) = X \backslash X(1, \phi_{10}) = \{000,001,010,011\}$

$X(2; \phi_{10}) = \{101\}$

$\overline{X}(2; \phi_{10}) = X \backslash X(2; \phi_{10}) = \{000,001,010,011,100,110,111\}$

$X(1,2; \phi_{10}) = X(1;\phi_{10}) \cap \overline{X}(2; \phi_{10}) \cup \overline{X}(1; \phi_{10}) \cap X(2; \phi_{10})$

$=\{100,110,111\} \neq \emptyset$ and the outputs 1 and 2 are weakly independent with respect to ϕ_{10}. In a similar way, it is easy to show that the outputs 1 and 2 are weakly independent with respect to the remaining faults ϕ_{ij}. Since the gates 2, 3, 4, and 5 influence only one of the outputs, all faults of these gates affect one output only and the outputs 1 and 2 are weakly independent with respect to all the single stuck-at-0/1 faults. Furthermore, the adder A of Fig.8 is testable with respect to every single stuck-at-0/1 fault.

The outputs 1 and 2 as weakly independent outputs, have to be added modulo 2 and inverted. The additional circuit g_c has to implement

$$\overline{s \oplus c_+} = a \wedge b \wedge c \vee \overline{a \vee b \vee c} .$$

The corresponding self-testing and self-checking adder is shown in Fig.9.

The implementation of g_c in Fig.9 is testable with respect to every single stuck-at-0/1 fault of its gates. If both the adder A and the additional circuit g_c are fault free, the SCC outputs $\overline{x_0}$. It is easy to see that the solution based on the concept of weakly independent outputs is much more cost effective than duplication and comparision. The stuck-at-1 faults on the inputs of the AND-gate, and a stuck-at-0-fault on the input of the NOR-gate of the SCC will not be detected during normal operation.

We now apply the described heuristic method for determining groups of weakly independent outputs to the circuit f_c shown in Fig.11. In this circuit we have

$$y_1 = x_1 \oplus (x_2 \wedge x_3)$$
$$y_2 = x_4 \oplus (x_2 \wedge x_3).$$

The circuit f_c is one of the rare examples where certain faults simultaneously influence for all inputs all the outputs of the circuit. Here the faults of gate 1 affect all outputs.The circuit f_c of Fig. 11 was only choosen as a simple example to illustate the proposed heuristic method for detereming groups of weakly independent outputs. All faults are assumed to be single stuck-at-0/1 faults of the gates 1, 2, and 3 resp.

All stuck-at-0/1 faults of gate 2 influence only output 1, and all stuck-at-0/1 faults of gate 3 influence only output 2. For the first set $J_1(2)$ of weakly independent outputs of f_c we choose $J_1(2) = \{ 1, 2 \}$.

The outputs 1 and 2 are to be added modulo 2, $z_1' = \overline{y_1 \oplus y_2} = \overline{x_1 \oplus x_4}$ and $J_1(2)$ is weakly independent with respect to all single stuch-at-0/1 faults of the gates 2 and 3. All the stuck-at-0/1 faults of gate 1 influence both the outputs 1 and 2 of the circuit shown in Fig. 11.

The error model for the AND-gate as described in section Error model is F(AND) = $\{ x_1 \wedge x_2, x_1, x_2, 1, 0 \}$. The (4, 2)-matrix $T = (T_{i,j})$ is given by

T =

	output:	
error fct.	1	2
x_1	1	1
x_2	1	1
1	1	1
0	1	1
sum:	4	4

The sum of 1's in every column of T is 4. One of the columns with the maximal value 4 is column 2. Column 2 is marked by *. Since $T_{i,j} = 1$ for i = 1, ...,4, every row is also marked by *. Column 1 is marked by + since, for example, row 1 is marked by * and $T_{2,2}$ =1.

T =

	+	*
*	1	1
*	1	1
*	1	1
*	1	1

All the rows of T are now deleted and output 2 forms a group of weakly independent outputs with respect to the stuck-at-0/1 faults of gate 1. Thus the heuristically determined complete set of weakly independent outputs is $J_1(2) = \{ 1, 2 \}$ and $J_2(1) = \{ 2 \}$.

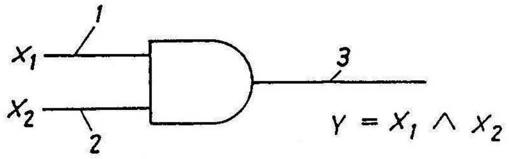

Figure 1

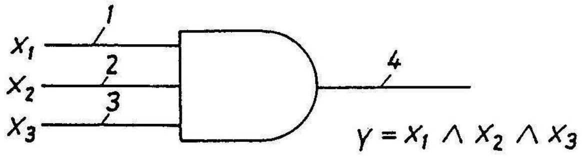

Figure 2

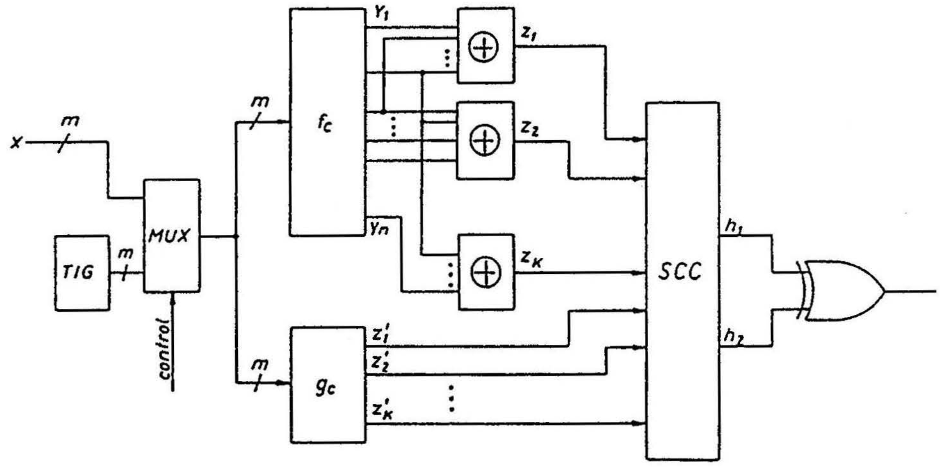

Figure 3

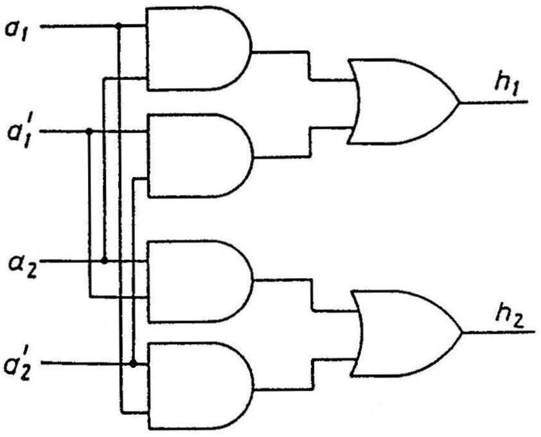

Figure 4

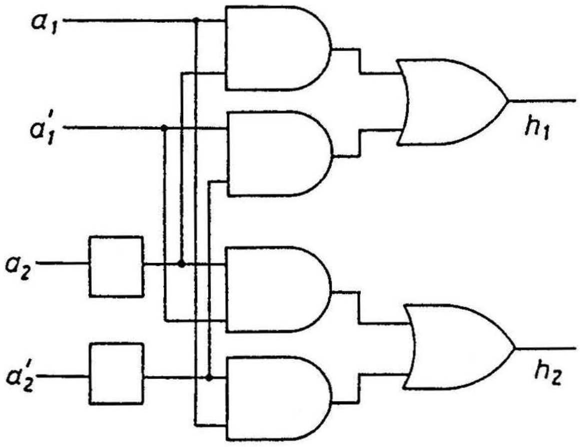

Figure 5

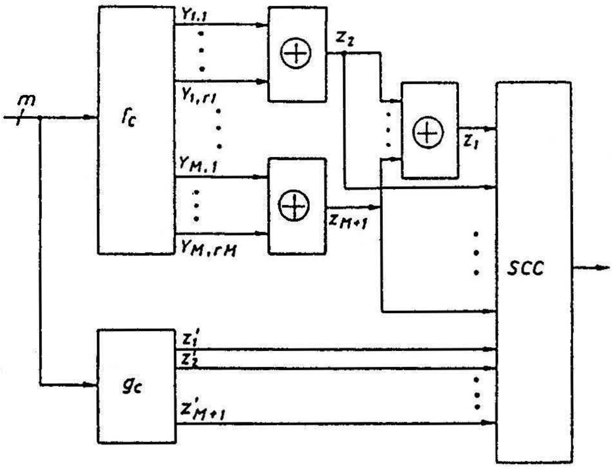

Figure 7

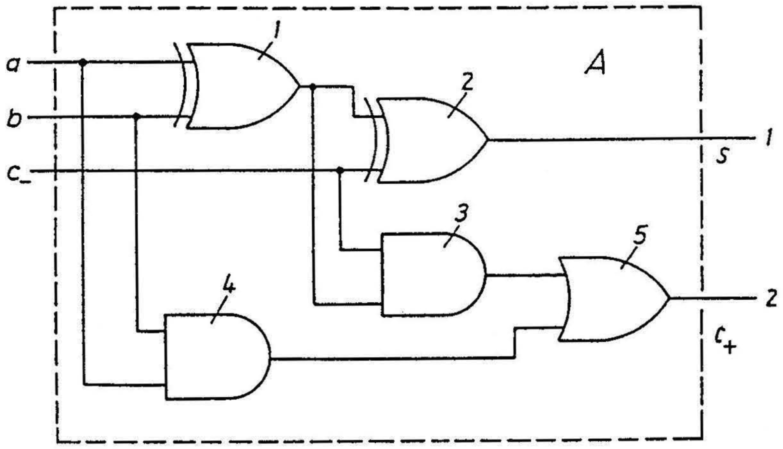

Figure 8

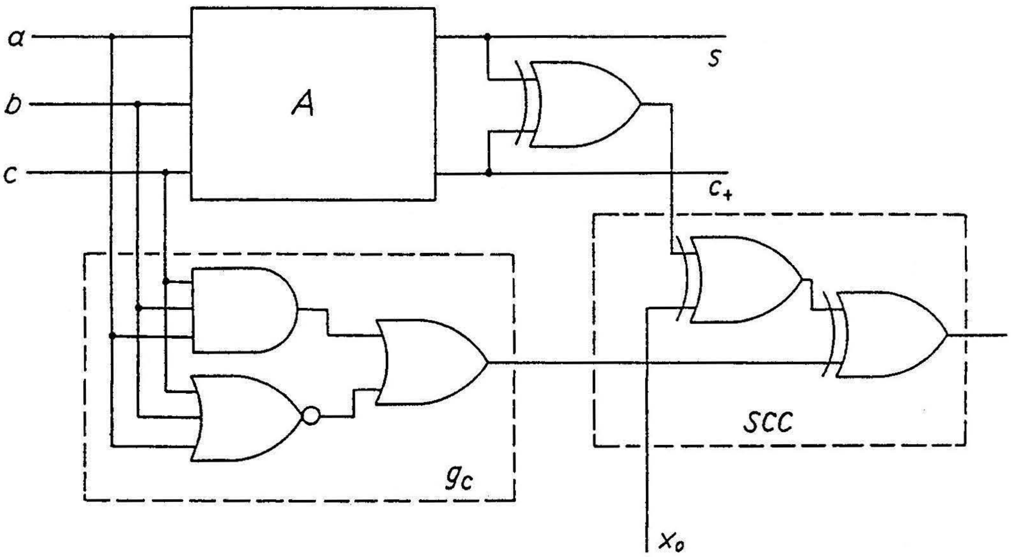

Figure 9

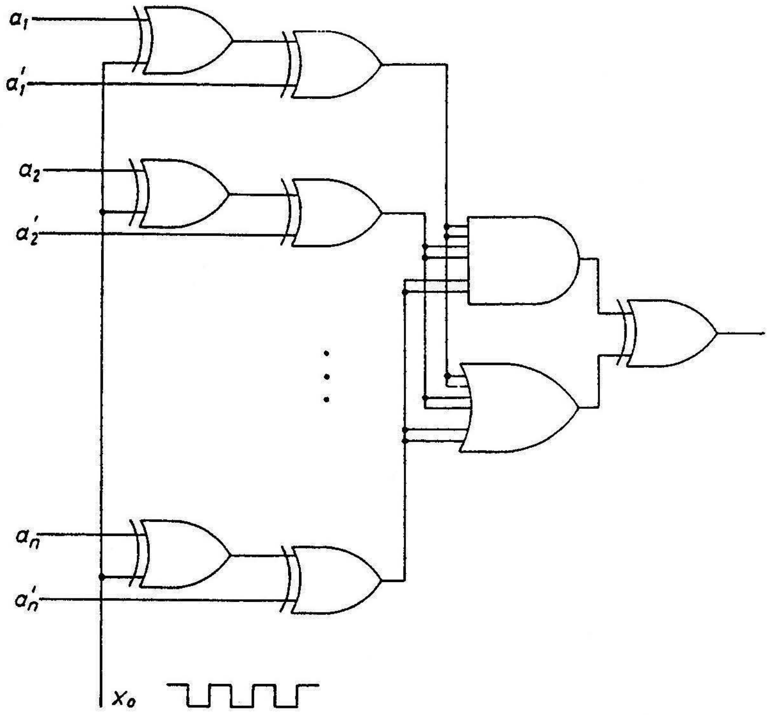

Figure 6

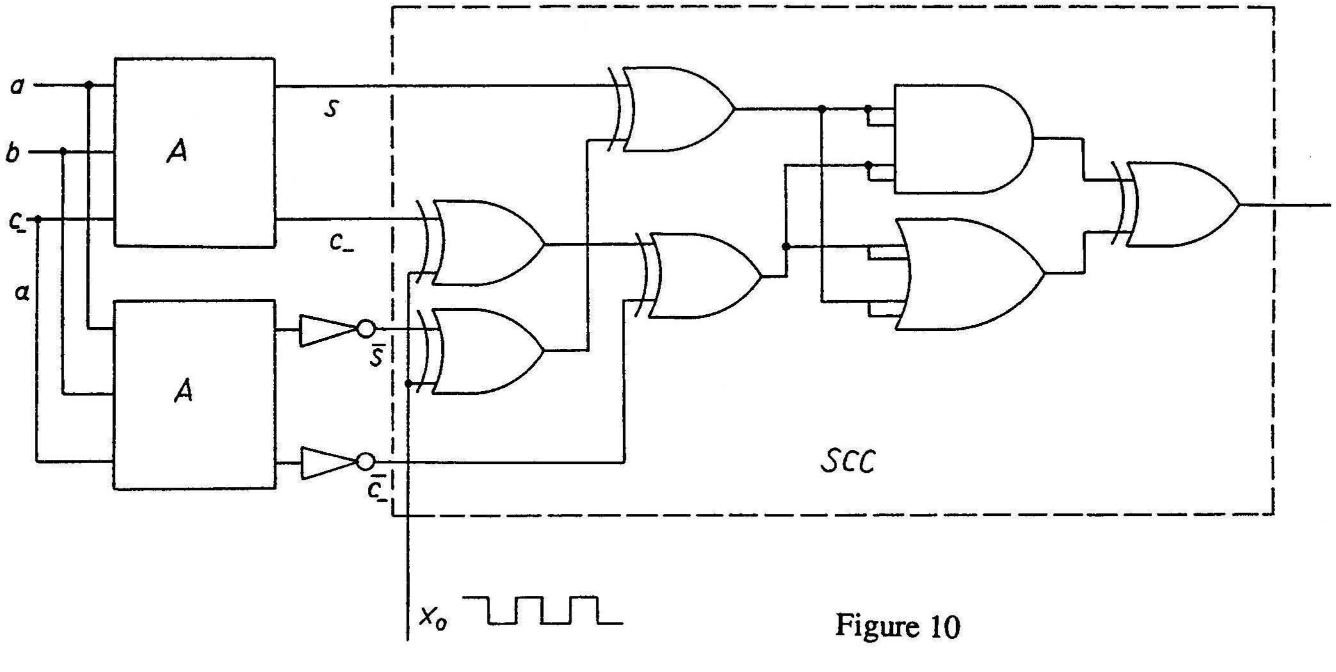

Figure 10

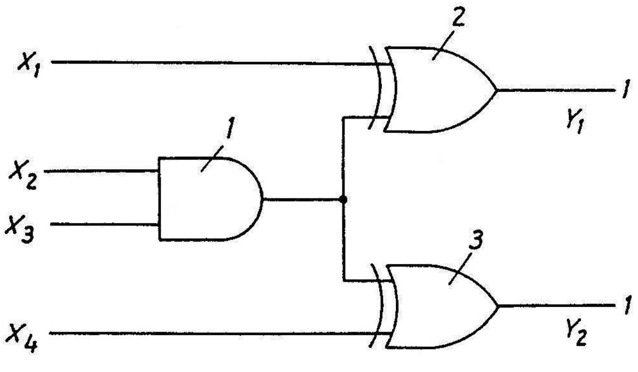

Figure 11

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