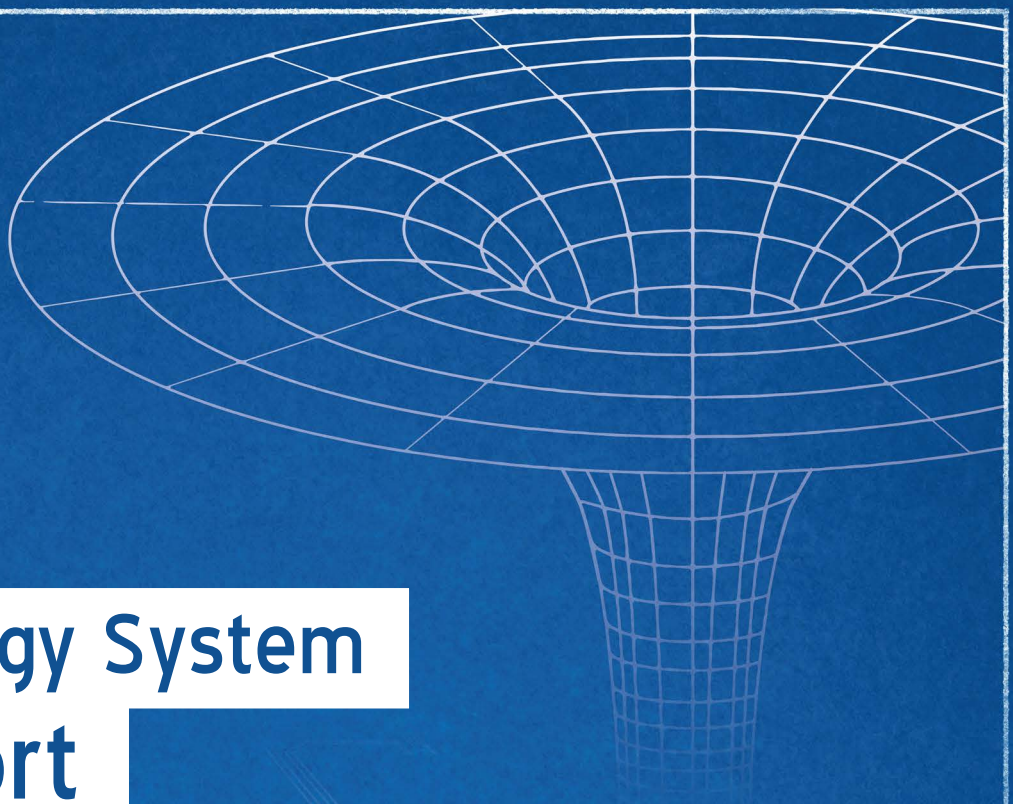

LISA Metrology System
Final Report

ESA ITT AO/1-6238/10/NL/HB

LISA METROLOGY SYSTEM

FINAL REPORT

DESIGN, DEVELOPMENT, MANUFACTURING, TESTING AND VALIDATION OF A BREADBOARD MODEL OF THE LISA METROLOGY SYSTEM

June 2011 – February 2014

National Space Institute, Lyngby, Denmark
Technical University of Denmark

with

Albert Einstein Institute, Hannover, Germany
Max Planck Institute for Gravitational Physics

and

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THE FUTURE OF ASTRONOMY

It will be the largest laser interferometer ever constructed: Three spacecraft, separated by millions of kilometers, sending laser light back and forth. A LISA-class mission will enable us to listen to the sound of the Universe.

The detection of tiny distance fluctuations between LISA spacecraft will reveal not only the existence of gravitational waves as predicted by Einstein's theory of General Relativity. It will open a new window to the Universe. With LISA we can—for the very first time—learn details about dark objects as yet hidden from our instruments: black holes, neutron stars, and even the echo of Big Bang itself.

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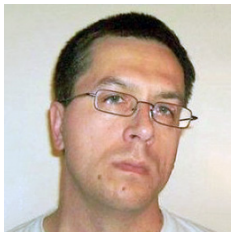

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Part I

INTRODUCTION

Gravitational Waves will open an entirely new window to the Universe, different from all other astronomy in that the gravitational waves will tell us about large-scale mass motions even in regions and at distances totally obscured to electromagnetic radiation. The most interesting sources are at low frequencies (mHz to Hz) inaccessible on ground due to seismic and other unavoidable disturbances. For these sources observation from space is the only option, and has been studied in detail for more than 20 years as the LISA concept.
Consequently, *The Gravitational Universe* has been chosen as science theme for the L3 mission in ESA's Cosmic Vision program.

The primary measurement in LISA and derived concepts is the observation of tiny (picometer) pathlength fluctuations between remote spacecraft using heterodyne laser interferometry. The interference of two laser beams, with MHz frequency difference, produces a MHz beat note that is converted to a photocurrent by a photodiode on the optical bench. The gravitational wave signal is encoded in the phase of this beat note. The next, and crucial, step is therefore to measure that phase with µcycle resolution in the presence of noise and other signals. This measurement is the purpose of the LISA metrology system and the subject of this report.

1 LISA MISSION

We have come a long way since Isaac Newton's 1687 inverse-square law of gravity. In fact, it was Newton himself who questioned his own theory. For him the assumption that gravitation acts instantaneously, regardless of distance and even through a vacuum, was "so great an absurdity that, I believe, no man who has in philosophic matters a competent faculty of thinking could ever fall into it." [1]

1.1 GRAVITATIONAL WAVES

Although Newton's theory of gravity is still used today as excellent approximation for most physical situations—including calculations as critical as spacecraft trajectories—it is wrong.

1.1.1 EINSTEIN'S THEORY OF GENERAL RELATIVITY

The currently unrefuted hypothesis as to the cause of the gravitational force was described by Albert Einstein in 1915 in his theory of General Relativity. His conclusion: gravitation is not propagating through space, and it is not a force of a field or substance penetrating empty space. Instead gravitation is mediated by the deformation of spacetime, a mathematical model that combines the three dimensions of space and the one-dimensional time into a single four-dimensional continuum. While mass, energy, momentum, pressure, or tension (all combined in the stress-energy-tensor $T_{\mu\nu}$, which measures the matter content) will curve spacetime, matter simply follows the geodesics of spacetime.

> *Spacetime tells matter how to move;*
> *matter tells spacetime how to curve.*
>
> — John Wheeler [2]

This is the main message of General Relativity and illustrated in Figure 1.1. The geometry of spacetime is described in the Einstein tensor $G_{\mu\nu}$, which measures its curvature. Each tensor has 10 independent components and the relationship between both was formulated in the Einstein field equations as

$$G_{\mu\nu} + \Lambda g_{\mu\nu} = \frac{8\pi G}{c^4} T_{\mu\nu} \tag{1}$$

where G is the same gravitational constant as in Newton's law and c is the speed of light. The Λ in Equation 1 is the famous cosmological

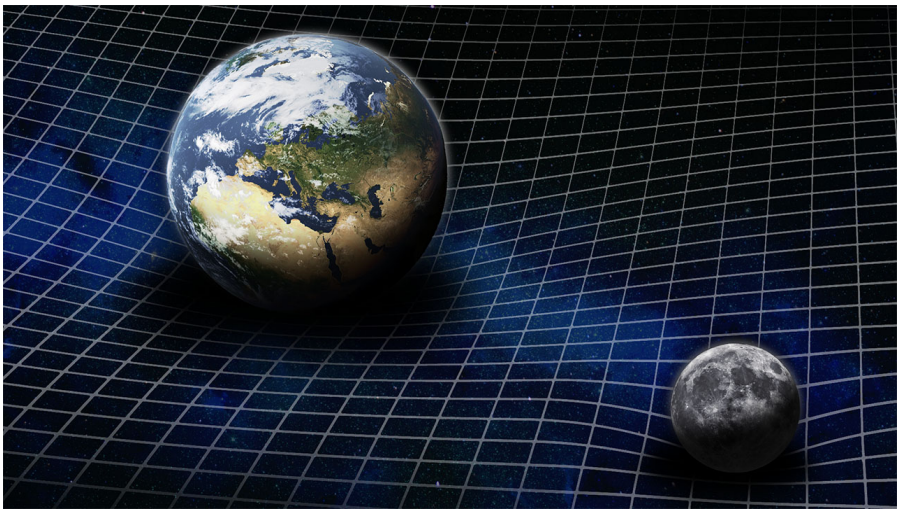


Figure 1.1: Illustration showing the Earth and the Moon warping the fabric of spacetime. *© AEI / S. Barke*

constant, an energy density in otherwise empty space influencing the metric tensor $g_{\mu\nu}$ (or, simplified, the gravitational field).

The Einstein field equations are capable of much more than just explaining gravity; they have given us a toolset to understand the workings of the Universe. Beside black holes and gravitational lensing the maybe most exciting consequence of Einstein's theory is the postulation of gravitational waves. The field equations predict that accelerated matter emits gravitational quadrupole radiation.

There are many indirect observations of gravitational waves, like the measurement of the orbital decay of the Hulse–Taylor binary pulsar (PSR B1913+16) which is in perfect agreement with General Relativity and was awarded the Nobel Prize in Physics in 1993. [3]. Most recently a divergence-free, curl only (B-mode) polarization pattern in the cosmic microwave background was discovered in data of the BICEP2 telescope. [4] While at small scales this can be an effect of gravitational lensing, the large scale patterns are potentially due to gravitational waves produced during **cosmic inflation**, a theorized period of rapid expansion of the Universe that occurred approximately 10^{-36} seconds after the big bang. This epoch is not accessible by electromagnetic radiation, yet we can learn details about the process of cosmic inflation and discard certain theories like brane cosmology related ekpyrotic models. [5] Thus this result—if confirmed by an independent experiment—marks the very first time where gravitational waves extend our knowledge about the otherwise invisible Universe.

The theory of **cosmic inflation** was proposed in 1980. It explains the large-scale structure of the cosmos as quantum fluctuations instantaneously magnified to cosmic size. While the detailed mechanism behind inflation is not known, many predictions made on the basis of the inflation hypothesis have been confirmed by observation. The B-mode polarization is the most compelling evidence so far.

In general, gravitational waves stretch and compress spacetime perpendicular to the direction of travel and cause directly observable distance fluctuations between freely falling objects. This is illustrated in Figure 1.2 for a ring of such objects and gravitational radiation originating from your point of view. The distance between the mases

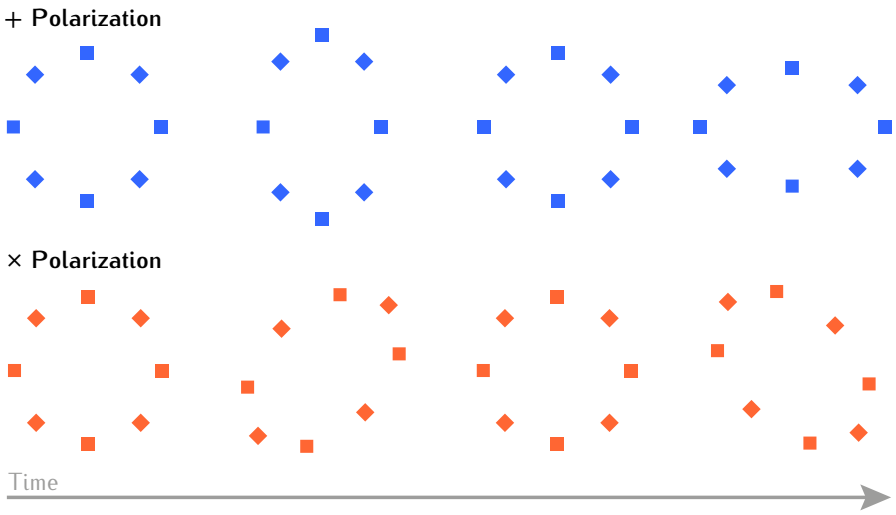


Figure 1.2: Gravitational waves change the distance between freely falling objects perpendicular to the direction of travel. Displayed are the most common polarization states: plus (+, blue) and cross (×, red) for gravitational radiation originating from your point of view.

oscillates with time, the direction of this oscillation depends on the polarization of the gravitational waves. The usual basic set of polarization states are plus (+) and cross (×) polarization, others can be formed by linear combinations of these two.

While the strength of the gravitational field falls off with the square of the distance, this effect, an amplitude, falls off linearly proportional to the distance [6] and even sources located at the other end of the observable universe can produce relative distance fluctuations on the order of 10^{-20} or more, depending on the frequency of the signal.

EXAMPLE: At a distance of 4 kilometers, relative distance fluctuations of 10^{-20} correspond to 40 attometers. This is much smaller than an atomic nucleus. For a distance of 1 million kilometers, the same fluctuations correspond to 10 picometers, which is ten times smaller than the diameter of a hydrogen atom.

This effect, as tiny as it might seem, can tell us about electromagnetically invisible objects and has a huge discovery potential for new physics. Gravitational radiation travels unaffected throughout the entire Universe; in contrast to electromagnetic radiation that interacts strongly with matter and hence is often distorted or blocked. Thus gravitational waves are a superior messenger that holding complimentary or even otherwise completely unobtainable information about processes in the Universe.

Observatories dedicated to the direct detection of gravitational waves will establish a new field of astronomy and open an entirely new windows to the Universe. Since gravitational waves exist in a large variety of frequencies – depending on the source of the gravitational radiation – different detector concepts are necessary to cover the entire spectrum.

1.1.2 SOURCES OF GRAVITATIONAL RADIATION

All accelerated matter (or energy in general) produces gravitational waves as illustrated in Figure 1.3. The frequency components of these waves depend on the nature of the source event and exist—not unlike electromagnetic radiations—in a wide frequency range from sub-millihertz up to the audio band. The following list is not intended to be exhaustive, but features a good overview of the variety of gravitational wave sources, also composed in Figure 1.6.

BURST SIGNALS Rapid violent acceleration produces high frequency burst signals of distinct shape and characteristics. One known source are Type II supernova events, the core collapse and rebounce of stars with mass greater than $\gtrsim 8 \ldots 10\, M_\odot$ at the end of their thermonuclear burning life cycles, see Figure 1.6.5. [7] The strain amplitude depends on the asymmetry of these events. Observations of polarization in the spectra, jets in remnants, and kicks in neutron stars suggest that such supernovae are inherently aspherical. [8] Burst signals only last for a few milliseconds and thus lie in the frequency band between 100 and 1000 Hz.

CONTINUOUS SIGNALS Compact binary star systems or rapidly spinning neutron stars with smaller surface imperfections (on the order of centimeters) produce a constant sinusoidal gravitational wave signal. Depending on the angular velocity of the orbit or rotation, this signal can be visible at sub-millihertz (Figure 1.6.5) or several kilohertz (Figure 1.6.6) frequencies. The radiation of gravitational waves will lead to a loss of angular momentum.

INSPIRAL SIGNALS A sweeping sine signal occurs when two massive objects coalesce. This can be two supermassive black holes in the center of galaxies (see Figure 1.6.1) that produce signals

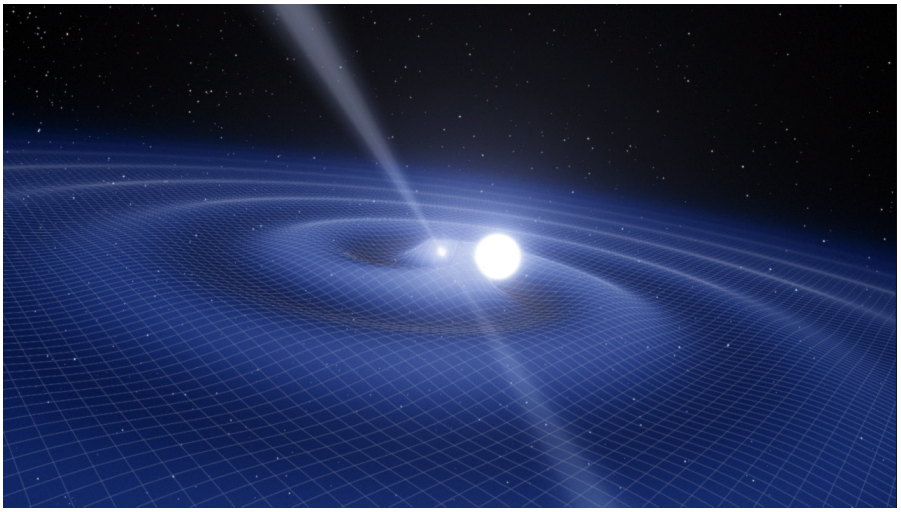


Figure 1.3: Artist's impression of the pulsar PSR J0348+0432 and its white dwarf companion, finishing one orbit every 2.5 hours. This system is radiating gravitational waves, ripples in space-time. *© ESO / L. Calçada*

in the millihertz range—at amplitudes so high that it will be detectable throughout the entire visible Universe—or a merging stellar mass binary system (see Figure 1.6.3) producing a signal at kilohertz frequencies. When two objects with an extreme mass ratio inspiral (see Figure 1.6.2) a complex waveform is generated by the highly relativistic orbits. Its harmonic frequencies shed light on the detailed features of the spacetime structure in the close proximity to this objects, tell us about their mass, spin and eccentricity at plunge, and will make it possible to distinguished between General Relativity and alternative theories of gravity.

UNKNOWN SOURCES Since gravitational radiation is a completely new messenger never utilized before, it has enormous discovery potential. The Big Bang and subsequent inflation (see Figure 1.6.4) caused a rapid expanding of spacetime. A gravitational wave background dating from a period prior to the cosmic microwave background should exist. Other unknown sources like bursts of cosmic strings Figure 1.6.8) are conceivable.

The characteristic gravitational wave strain amplitudes over frequency for example signals caused by the events described above are shown in Figure 1.6.

1.2 DETECTORS

There are a number of concepts on how to detect gravitational waves ranging from solid bars of metal (Weber bars) [9] that are excited at their resonant frequency by gravitational waves to the measurement of shifts in millisecond pulsar signals caused by gravitational waves (e.g. the European Pulsar Timing Array [10]). While the latter utilizes the Earth-pulsar baseline of several kiloparsecs and hence is sensitive for extremely long wavelength (frequency of $10^{-9} \ldots 10^{-6}$ Hz), Weber bars have narrow-band resonance frequencies at the kilohertz range.

The most promising concept for gravitational wave detectors are laser interferometric distance measurements. In the Michelson topology as shown in Figure 1.4, a central laser is split in two directions (arms) and reflected by end mirrors back to the point of origin. Here both beams are superimposed. Constructive and destructive interference patterns (homodyne detection) reveal relative distance fluctuations between the beam splitter and the end mirrors that are caused by gravitational waves. The measurement band is basically determined by the fixed arm lengths, and can be tuned with an additional resonant optical cavity ("Signal recycling").

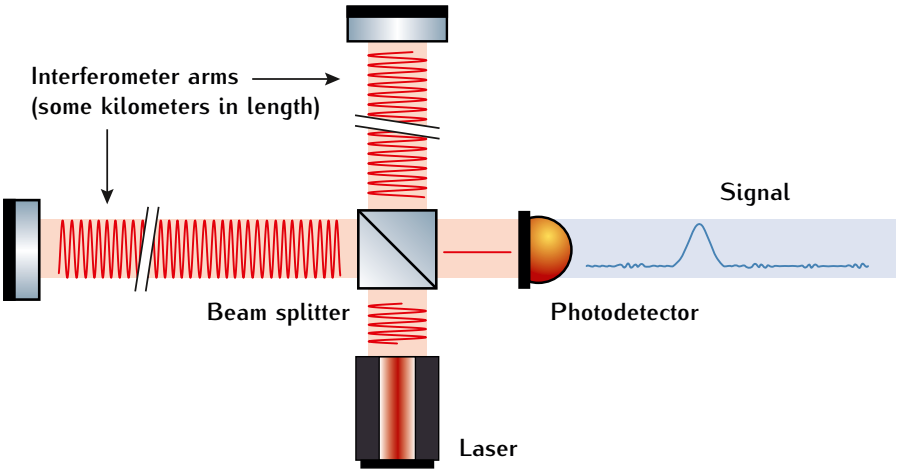


Figure 1.4: Michelson interferometer (homodyne detection) for gravitational wave detection. A laser is split and send along km-scale arms. End mirrors reflect the beams back and the interference pattern is analyzed to detect relative distance fluctuations between the arms.

Current ground based detectors such as LIGO (USA), VIRGO (Italy and France) and GEO600 (Germany and UK) [11–13] reach strain sensitivities of $2 \times 10^{-23} / \sqrt{\text{Hz}}$ at $\approx 200\,\text{Hz}$. The sensitivity of second generation detectors such as Advanced LIGO (USA and India) and KAGRA (Japan) is designed to improve that by one order of magnitude. All of these detectors though are fundamentally limited to frequencies above 10 Hz due to seismic disturbances. This "seismic wall" is obvious in the LIGO and Advanced LIGO sensitivity plots (green traces in Figure 1.7, plotted in characteristic strain amplitude).

Sensitivity at lower frequencies thus cannot be achieved on Earth also because it would require arm lengths on the order of thousands or millions of kilometers. For that reason, space based gravitational wave detectors are currently being developed.

"**LISA Mission**" is the generic name for a laser interferometric gravitational detector concept which is the only credible candidate to realize *The Gravitational Universe* science theme selected by ESA for the L3 mission.

With the selection of *The Gravitational Universe* as the science theme for the L3 mission in ESA's Cosmic Vision program, a space based gravitational wave detector will become operational in the 2030s. The only viable option for such an detector known to date is a heterodyne laser interferometer with arm lengths of a few million km which was studied in great detail over the past decade. It became known as the **LISA Mission**. The sensitivity of one of the latest incarnations, eLISA, is designed to be $\approx 3 \times 10^{-20} / \sqrt{\text{Hz}}$ at 10 mHz and plotted as dimensionless characteristic strain in Figure 1.7 (blue). It covers many of the most exciting gravitational wave sources: supermassive black hole coalescence, Galactic compact binaries, and extreme mass ratio inspirals, all of which are not observable from Earth.

1.3 MISSION DESCRIPTION

In a space based laser interferometric gravitational wave detector, laser light is sent out and received by optical telescopes between dis-

tant spacecraft. Interference happens between the incoming laser light and a local laser source. The actual interferometer topology is synthesized out of multiple interferometric read-outs. LISA (the Laser Interferometer Space Antenna) is the name for the generic mission concept of a number of such gravitational wave detectors—like Classic LISA (NASA/ESA), NGO (ESA), SGO (NASA), and eLISA (ESA)—that all share the following parameters:

- Three spacecraft in a triangular formation
- Arm lengths on the order of 1 . . . 5 million kilometers
- Heliocentric orbit, trailing or ahead the Earth, on a plane inclined by 60° with respect to the ecliptic
- Freely floating proof masses that act as gravitational references
- Drag-free attitude control with µN thrusters
- Optical interferometry, typically at 1064 nm wavelength
- Laser output power in the order of a few watts

A rough sketch of the LISA interferometry is shown in Figure 1.5. With this Classic LISA setup one can construct one virtual Sagnac and three virtual Michelson interferometers. Please note that in the eLISA (2013) concept one laser link is missing and the constellation forms a 2-arm (single virtual Michelson) interferometer.

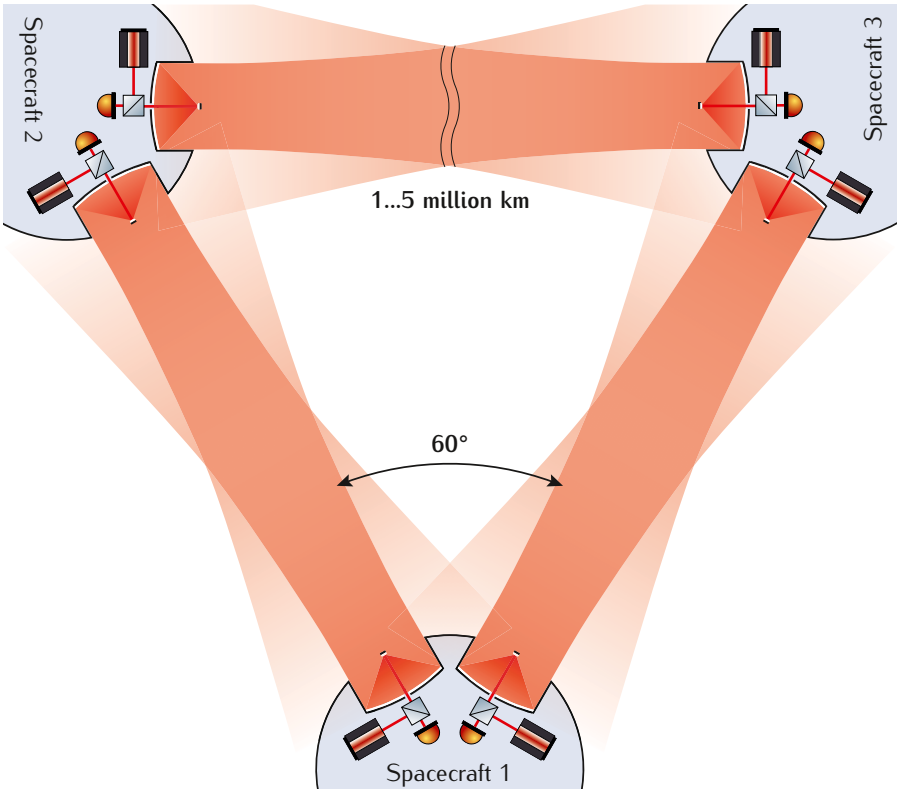
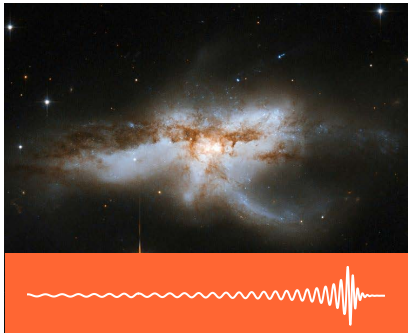
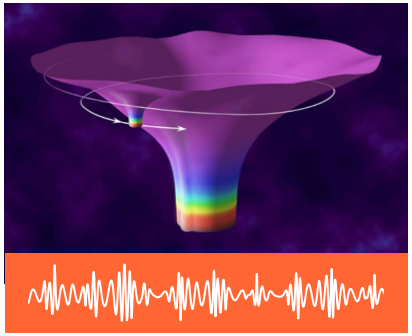


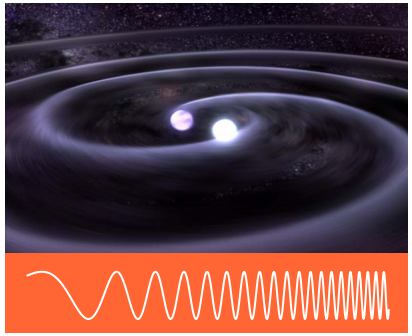
Figure 1.5: The Classic LISA constellation consists of three identical spacecraft separated by 5 million kilometers. Optical telescopes send out and receive laser light. The incoming laser light is combined with a local laser for interferometric read-out. Please note that in the eLISA (2013) concept one laser link is missing and the constellation forms a 2-arm interferometer at 1 million kilometer spacecraft separation distance. The principle remains the same.



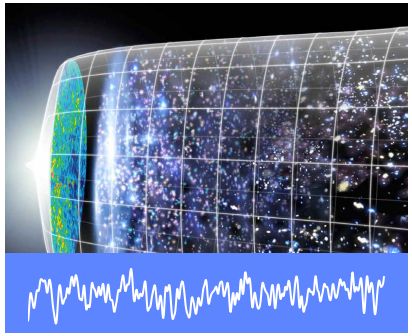
1.6.1: **Black hole binary mergers.** Coalescence of two supermassive black holes (image: merging galaxy NGC 6240) or stellar mass black holes. Waveform: inspiral, merger, ringdown. *© NASA / ESA / HST / A. Evans*



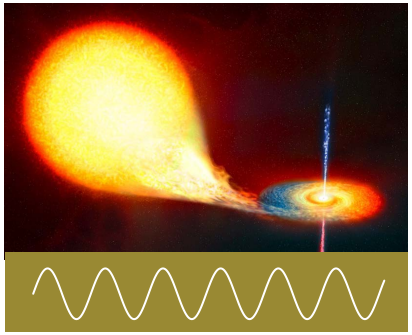
1.6.2: **Extreme mass ratio inspirals.** Neutron star or stellar mass black hole captured in a highly relativistic orbit around a massive black hole. Waveform: enormous amount of information. *© NASA*



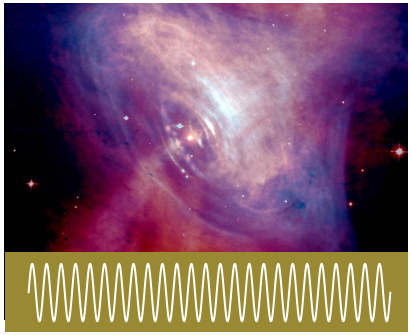
1.6.3: **Neutron star mergers.** Two neutron stars in a close orbit that shrinks until merger due to radiation of gravitational waves. Waveform: sine wave at increasing frequency. *© GSFC / D. Berry*



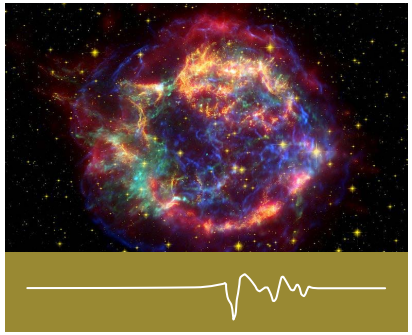
1.6.4: **The Big Bang.** Gravitational waves are the only form of information that can reach us directly from the Big Bang. Wave form: stochastic background (noise). *© NASA / WMAP science team*



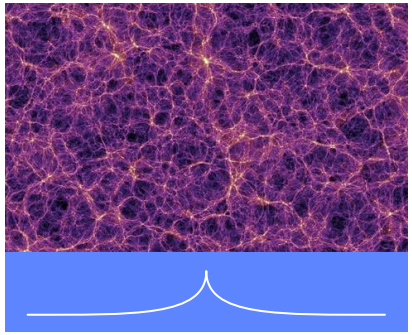
1.6.5: **Compact binaries.** A compact object like a neutron star or a black hole (right) and a companion in very close orbit. Matter transfer leads to Type Ia supernovae. Waveform: high frequency sine. *© ESA*



1.6.6: **Pulsars.** Rapidly spinning neutron star (image: Crab Pulsar) with small (sub-meter) surface imperfection. Waveform: high frequency sine. *© NASA / HST / CXC / ASU / J. Hester et al.*



1.6.7: **Supernovae (Type II).** Asymmetric core-collapse supernovae (image: Cassiopeia A remnant) produce gravitational waves. Waveform: distinct characteristics. *© NASA / ESA / JHU / R. Sankrit & W. Blair*



1.6.8: **The Unknown.** Gravitational waves can originate from cosmic string bursts or totally unknown phenomena invisible to electro-magnetic observations. *© MPI Astrophysics / V. Springel et al.*

Figure 1.6: Overview of different gravitational wave sources and corresponding typical waveforms of expected signals. Characteristic gravitational wave strain amplitudes for example signals of inspiral events (red) and constant or burst events (yellow) are shown in Figure 1.7. The shape of a stochastic gravitational wave background or signals from yet unknown mechanisms (blue) are highly speculative.

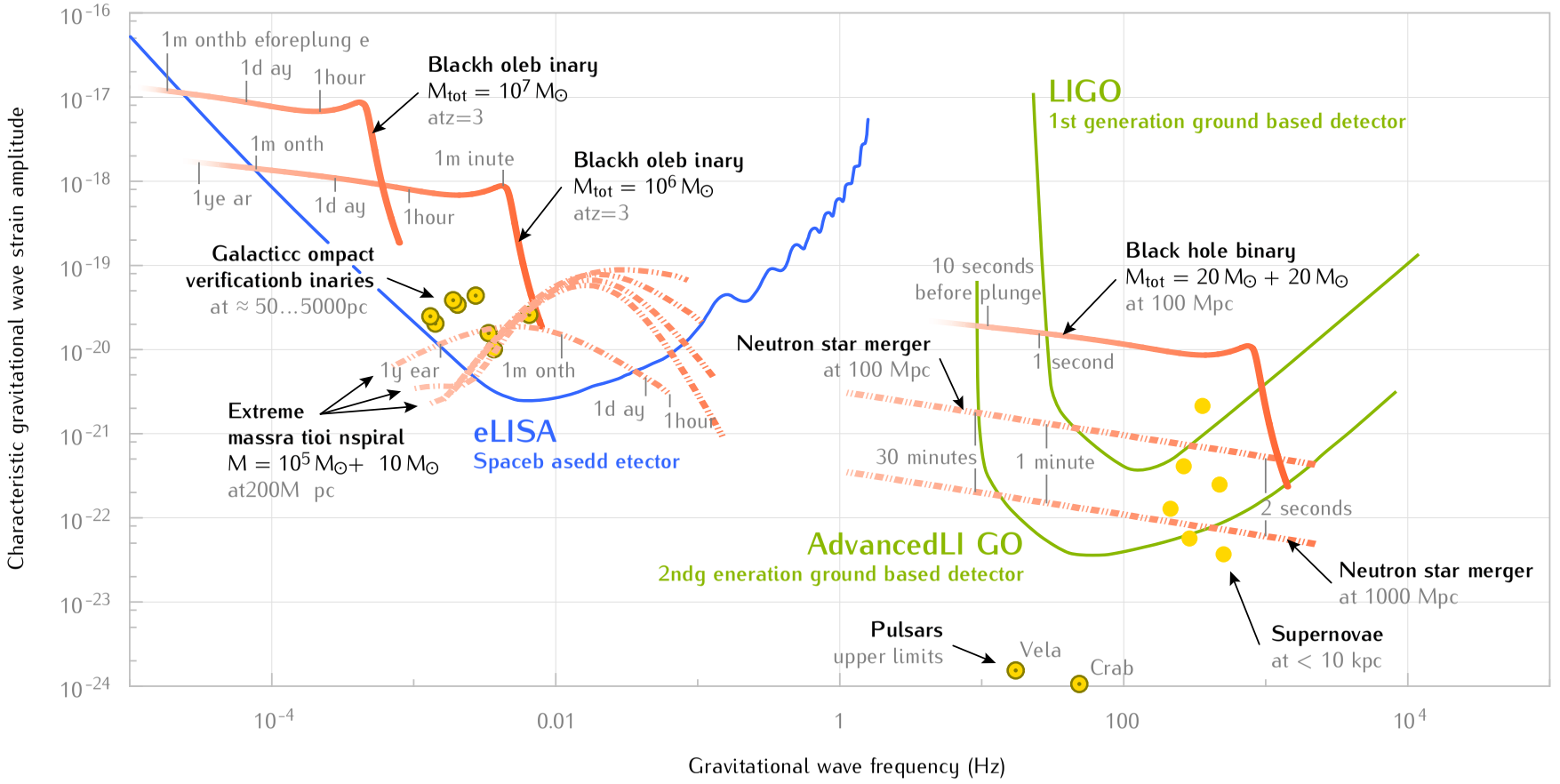


Figure 1.7: Characteristic gravitational wave strain amplitudes over signal frequency for a variety of signals (compare overview in Figure 1.6). Mass and distance for the events are indicated. The sensitivity of decommissioned 1st generation and upcoming 2nd generation ground based detectors is shown in green. They will detect stellar mass black hole binary mergers (Figure 1.6.1) and neutron star binary mergers (Figure 1.6.3), can set constrains on gravitational wave emissions of pulsars by matched filtering analysis (Figure 1.6.6) and may be able to detect burst signals of Type II supernovae (Figure 1.6.7). Designated space based detectors (as shown in blue) operate at much lower frequencies and will observe complementary sources of gravitational waves. They are sensitive to supermassive black hole binary mergers (Figure 1.6.1) within the entire observable universe, several thousand constant signals of Galactic compact binaries (Figure 1.6.5) some of which are already known, and the complex signal (harmonics shown in figure above) of extreme mass ratio inspirals (Figure 1.6.2) out to a distance of several hundreds of megaparsecs. The time before plunge are for inspiral and merger signals and indicate the maximum duration of observation within given detector sensitivity.

The mission parameters mentioned above will result in a shot noise limited design sensitivity which is best at frequencies close to 10 mHz. Here, gravitational waves having a **strain** amplitude less than $\sim 10^{-20}$ will be observable. All other noise sources must be suppressed at their origin or removed in data post-processing to below that level.

The **strain** of a gravitational wave is a measure of relative distance changes in a dimensionless amplitude $2\delta L/L$ caused by the gravitational wave as it passes by.

To reach such sensitivity, the spacecraft themselves – which are influenced not only by gravity but also by solar wind, solar radiation pressure, magnetic fields etc. – cannot act as end mirrors of the interferometer directly. Instead, the spacecraft follow freely floating proof masses (highly reflective cubes) in a drag-free manner. Laser interferometry now is not only applied between spacecraft but also between the spacecraft and their proof masses as shown in Figure 1.8. These proof masses are the actual gravity references.

Acceleration noise, caused by spurious forces on the proof masses along with other spurious forces on the proof masses from magnetic fields, Coulomb force, residual gas pressure etc. [14] are dominant in the low-frequency range. This results in a decrease of sensitivity roughly proportional to f^{-2} at sub-mHz frequencies. On the other hand, distance changes by gravitational waves of wavelengths shorter than the arm length will partly cancel out. This results in a drop of the antenna transfer function (called "arm length response") at high frequencies. A representative curve is presented in Figure 1.6 on page page 10 showing the strain sensitivity in characteristic amplitude (not linear spectral density) over the gravitational wave signal frequency.

1.3.1 CLASSIC LISA VS. ELISA

The detailed mission parameters are a result of a careful trade-off between science output (sensitivity, mission duration) and redundancy

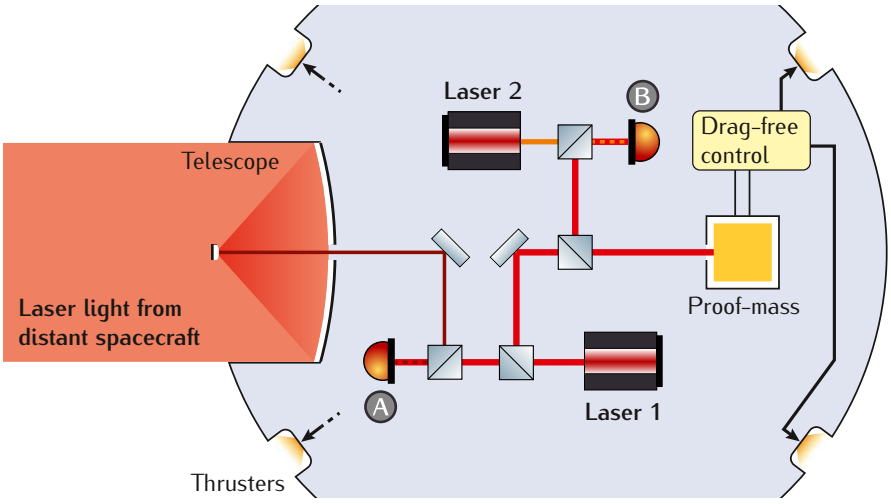


Figure 1.8: Freely floating proof masses inside the LISA spacecraft act as gravity references at each end of one laser link. The measurement of the distance between a local and a remote proof mass (length measurement of one laser link) is divided into 1) spacecraft/spacecraft measurements (detector A) and 2) spacecraft/proof mass measurements (detector B). The spacecraft's position is actuated to follow the motion of the proof mass.

within budgetary and technical constraints. In the last couple of years two very mature mission concepts arose that should be highlighted.

CLASSIC LISA, formally a joint NASA–ESA project [15] and for a long time ESA's Cosmic Vision L1 launch candidate.

ELISA, an ESA-only mission that addresses *The Gravitational Universe* science theme [16] selected in November 2013 for ESA's Cosmic Vision L3 mission.

A comparison of the mission parameters for both concepts is given in Table 5. While Classic LISA consist of three equal spacecraft separated by 5 million kilometers forming a triangular interferometer with 6 laser links, eLISA in its concept proposed in 2013 is a reduced mission due to tighter financial constraints. At the expense of redundancy, eLISA features one Mother and two Daughter spacecraft that form a four-link (two-arm) interferometer. A shorter arm length of 1 million kilometers allows for a reduction of the optical telescope diameter from 40 to 20 cm. Combined with a smaller propulsion module it is possible to launch the eLISA mission by two Soyuz rockets.

While the Classic LISA mission concept follows Earth at a fixed angle of 20° (Figure 1.9, top) eLISA's propulsion module does not allow for a constant trailing orbit. Due to savings in fuel the constellation is slowly drifting away from Earth out of communication range (Figure 1.9, bottom) which limits the maximum mission duration of eLISA to 5 years.

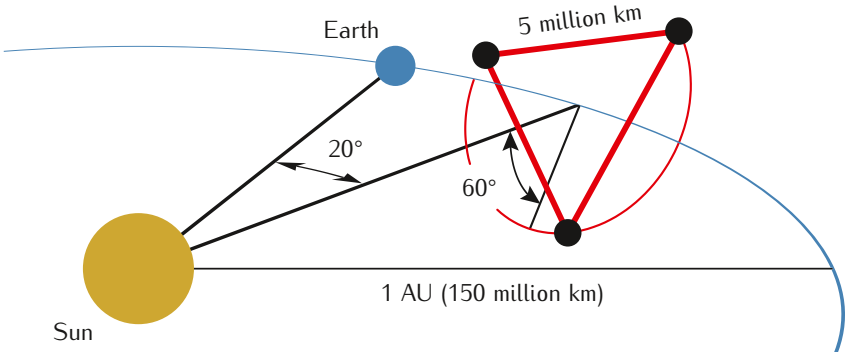
Table 5: Comparison of mission parameters between the Classic LISA mission concept and the eLISA concept of 2013.

	Classic LISA	eLISA (2013)
Launcher	Atlas V 541	2 Soyuz
Propulsion module	New development	Derived from LISA Pathfinder mission
Transfer time	14 months	14 months
Mission duration	5 years nominal, 10 years extended	2 years nominal, 5 years extended
Orbit	Earth-trailing, constant 20°	Earth-trailing, drift away 10 . . . 30°
Spacecraft	All identical	1 Mother, 2 Daughters
Interferometer	Triangular (6 links)	Two-arm (4 links)
Arm length	5 million kilometers	1 million kilometers
Optical telescope	⌀ 40 cm off-axis Schiefspiegler	⌀ 20 cm off-axis Schiefspiegler
Optical power	1 W transmitted, 370 pW received	1 W transmitted, 710 pW received

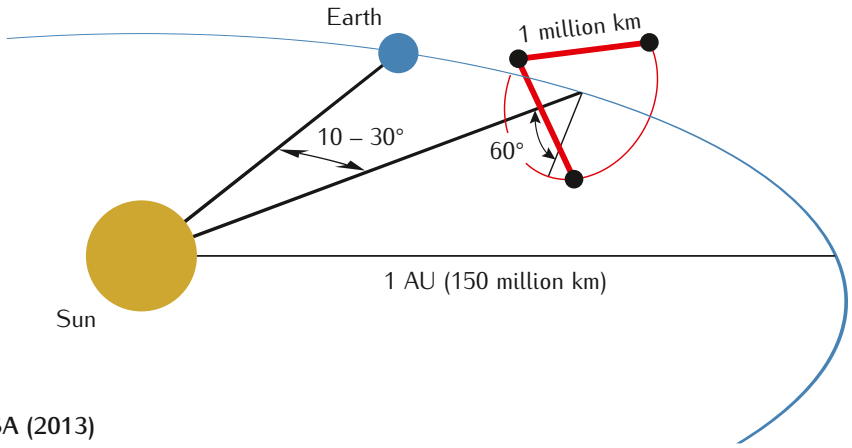
To compute well-founded **sensitivity limits** for both missions it is indispensable to include the antenna transfer functions for the different interferometer topologies and evaluate the astrophysical science case individually. This is done explicitly in the respective Yellow Books [15, 17].

The detection of gravitational waves depends on the mission specific **sensitivity limits** that are designed to be dominated by equivalent length measurement noise of the signal-to-(shot) noise ratio in the inter-spacecraft interferometer. For Classic LISA a conservative calculation results in a value of $10\,\mathrm{pm}/\sqrt{\mathrm{Hz}}$. To get a sense of the strain sensitivity this needs to be compared to the spacecraft separation distance of 5 million kilometers. Due to the higher optical power received at an arm length of only 1 million kilometers, eLISA shows a slightly better equivalent length measurement noise of $7\,\mathrm{pm}/\sqrt{\mathrm{Hz}}$. At the same time the smaller spacecraft separation distance leads to a reduced strain sensitivity.

These numbers imply that both missions would achieve roughly comparable strain sensitivity and have similar performance requirements on the payload. Most importantly the expected science discoveries are exceptional and unprecedented in both cases.



Classic LISA



eLISA (2013)

Figure 1.9: Classic LISA and eLISA differ not only in the spacecraft separation distance and number of laser links. The shorter arm length allows for smaller optical telescopes and an overall more compact spacecraft design. While for Classic LISA the Earth-trailing orbit is kept at a constant 20°, eLISA slowly drifts away from Earth.

1.3.2 ORBIT AND DOPPLER SHIFTS

Ground base detectors are designed to have constant and well-balanced arm lengths such that laser frequency noise automatically cancels, and **homodyne interferometry** can be used. In LISA, however, the inter spacecraft separation distance oscillates over the duration of the mission due to gravitational influences by the Earth–Moon system (and other planets in the solar system) on the individual spacecraft orbits. This is also called constellation or arm length "breathing".

Homodyne interferometry describes interference between two beams at the same frequency. Because of constructive and destructive interference phase difference between the two beams results in a change in the intensity of the light on the detector.

Figure 1.10 illustrates that for optimized orbits these variations can be kept within 2 % of the nominal arm length for both mission concepts. Yet this variation causes the individual arms to differ in length by up to 4 %—or 200 000 km—for Classic LISA (40 000 km for eLISA).

The picometer scale variation of the arm length caused by gravitational waves can be separated from those large motions since they happen at different timescales (minutes vs. months). There are two consequences though that result from the breathing of the constellation.

1) LASER FREQUENCY NOISE: With unequal arm lengths laser frequency noise is not canceled automatically. A post-processing technique that shifts the different interferometer signals in time to synthesize a virtual equal arm length interferometer is required. This technique is called Time Delay Interferometry (TDI)

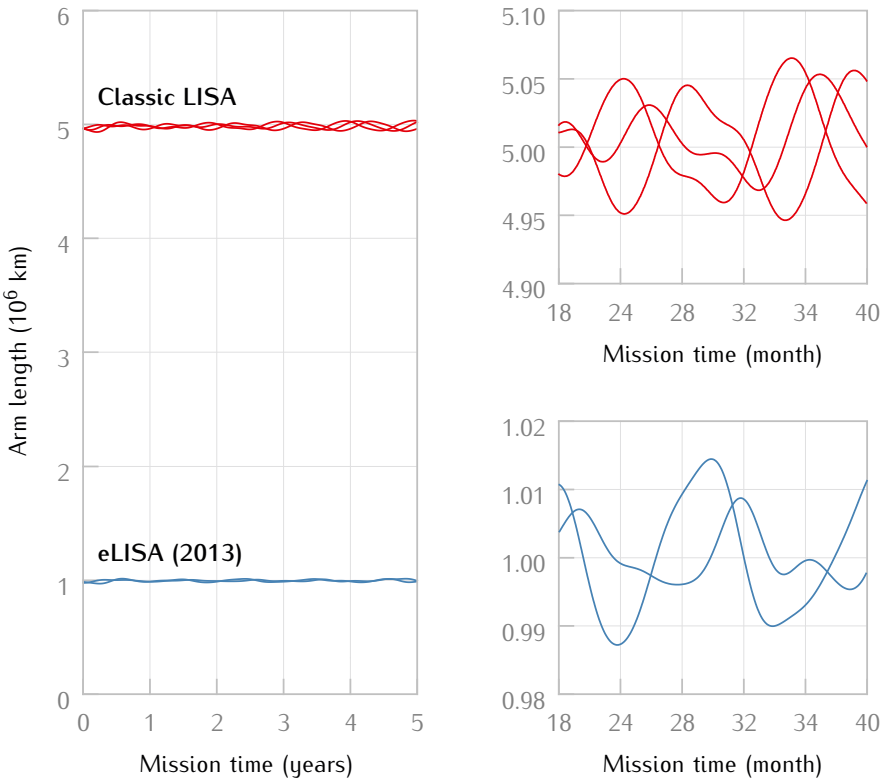


Figure 1.10: Variation of inter spacecraft separation distance due to disturbances within our solar system for Classic LISA and eLISA. All variations can be kept within 2 % of the nominal arm length. Superimposed on these large (but very slow) distance variations would be much smaller variations of higher frequency due to gravitational waves of a multitude of distant sources. The impact of these gravitational waves within a frequency range of roughly 0.1 mHz to 1 Hz is on the order of sub-nm for most sources.

and can suppress the noise by 13 orders of magnitude. [18] This will bring the laser frequency noise below the shot noise limit without removing the gravitational wave signal.

2) DOPPLER SHIFTS: The change in inter spacecraft separation distance over time between any two spacecraft results in a relative velocity in the line of sight of up to $\Delta v = 20\,\mathrm{m\,s^{-1}}$ for Classic LISA ($4\,\mathrm{m\,s^{-1}}$ for eLISA).

The relative velocity along the line of sight translates to a shift Δf in the frequency $f = c/1064\,\mathrm{nm}$ of the received laser light (optical Doppler effect) according to

$$\Delta f = f\left(\frac{\sqrt{c+\Delta v}}{\sqrt{c-\Delta v}} - 1\right) \tag{2}$$

which amounts to a maximum Doppler shift of $\Delta f = 18\,\mathrm{MHz}$ for Classic LISA and $\Delta f = 3.8\,\mathrm{MHz}$ for eLISA (2013).

This prevents the use of homodyne read-out schemes and we have to deal with the interference of two laser beams of unequal frequency.

1.3.3 HETERODYNE INTERFEROMETRY

Light from the incoming laser and the local laser with amplitudes E_{RX} and E_{LO}, and electric fields given by

$$E_{\mathrm{RX}} \sin\left(2\pi f_{\mathrm{RX}} t\right), \quad E_{\mathrm{LO}} \sin\left(2\pi f_{\mathrm{LO}} t + \varphi\right)$$

interferes at a beam splitter and is detected by a photodiode as illustrated in Figure 1.11. The interference creates two new signals at the sum $f_{\mathrm{RX}} + f_{\mathrm{LO}}$ and the difference $f_{\mathrm{RX}} - f_{\mathrm{LO}}$ frequencies with intensities

$$\propto E_{\mathrm{RX}} E_{\mathrm{LO}} \left[\cos\left(2\pi\left[f_{\mathrm{RX}} - f_{\mathrm{LO}}\right]t + \varphi\right) - \cos\left(2\pi\left[f_{\mathrm{RX}} + f_{\mathrm{LO}}\right]t + \varphi\right)\right].$$

Due to the limited bandwidth of the photodiode, only the beat note at the difference frequency is detectable, and is called heterodyne signal.

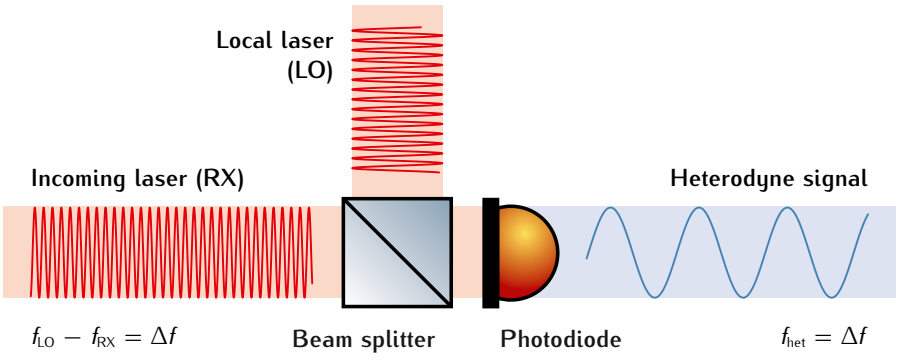


Figure 1.11: LISA uses heterodyne interferometry. The incoming laser light is combined with a local laser at similar (but not equal) frequency. A photodiode detects the heterodyne signal at the difference frequency and converts it to an electrical signal.

The optical output signal will have an amplitude proportional to the product of the amplitudes of the input signals. Within the linear range of the photodiode, it can be assumed that the output signal of the photodiode is proportional to the optical **intensity**, equivalently the squared amplitude of the electrical field.

The **intensity** of the down-mixed difference frequency can (and will) be larger than the intensity of the incoming laser light itself. This is because the weak incoming light is mixed with the much stronger local laser source.

In the presence of a gravitational wave which produces a phase modulation $\phi(t)$ on the incoming laser light, this phase modulation will be conserved:

$$\begin{aligned} & E_{RX} \sin\left(2\pi f_{RX} t + \phi(t)\right) \quad \times \quad E_{LO} \sin\left(2\pi f_{LO} t\right) \\ \propto \quad & E_{RX} E_{LO} \cos\left(2\pi \left[f_{RX} - f_{LO}\right] t - \phi(t)\right) . \end{aligned}$$

If the optical phase of the incoming beam shifts by a certain phase angle, then the phase of the heterodyne signal shifts by exactly the same angle. This correspondence is illustrated in Figure 1.12.

EXAMPLE: A gravitational wave changes the spacecraft separation of 5 000 000 km by 100 pm. This shifts the phase of the laser light (at 1064 nm wavelength) by 100 millionth of a cycle, or $\approx$ 600 µrad. This phase shift is conserved in the heterodyne signal. For a 10 MHz difference frequency (wavelength of $\approx$ 30 m) the same 600 µrad now correspond to a length of $\approx$ 3 mm in the read-out. This is equivalent to a 10^{-11} seconds shift in the signal's arrival time compared to a much harder to detect 3×10^{-19} seconds shift in the original signal.

The phase read-out becomes easier with smaller heterodyne frequency. That is why many LISA requirements scale linearly with the maximum heterodyne frequency. Hence it is desirable to keep all heterodyne frequencies as low as possible. This – and the necessity to

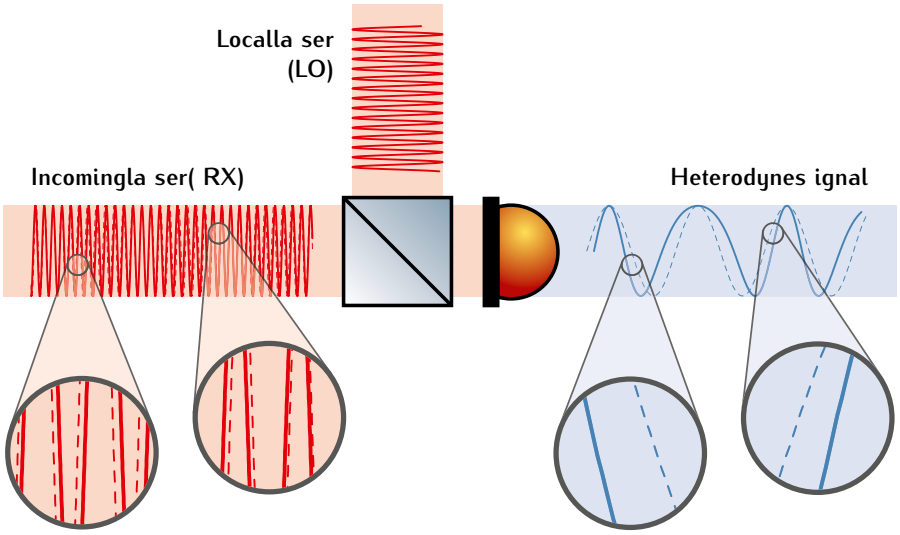


Figure 1.12: In the presence of a gravitational wave the incoming laser light is phase modulated. This phase modulation is conserved in the heterodyne signal which makes it much easier to detect in low frequency signals. Please note that in reality the phase modulation will only be of µrad amplitude at mHz frequencies while the heterodyne signal is at MHz frequencies.

avoid the case of zero heterodyne frequencies – requires the implementation of adaptable offset frequencies between the different lasers in combination with a carefully designed frequency plan.

1.3.4 LOCKING SCHEME AND FREQUENCY PLAN

In the Classic LISA case it is a much harder task than it is for eLISA to keep all heterodyne frequencies below a certain value. This becomes obvious when one compares the Doppler shifts of up to 18.8 MHz in 6 laser links (Classic LISA) with the 3.8 MHz in 4 links for (eLISA).

We have to ensure that the Doppler shifts are the only source of frequency drifts between lasers within the entire LISA constellation. Hence all the lasers are frequency locked to another one, with the only exception of a single laser (the "master") being locked to a stable frequency reference. A possible locking scheme is shown in Figure 1.13.

All of these locks have an offset frequency that will occasionally be changed during the mission lifetime, approximately every few weeks. It should be noted that lasers are also locked onto the Doppler shifted incoming light so that for some heterodyne signals these shifts add up in the locking chain. The task now is to find offset lock frequencies that keep all signals in the optimal detection band.

The optimization conditions are:

- Keep the maximum heterodyne frequency as low as possible
- No zero-crossings (no heterodyne signal must cross 0 MHz)

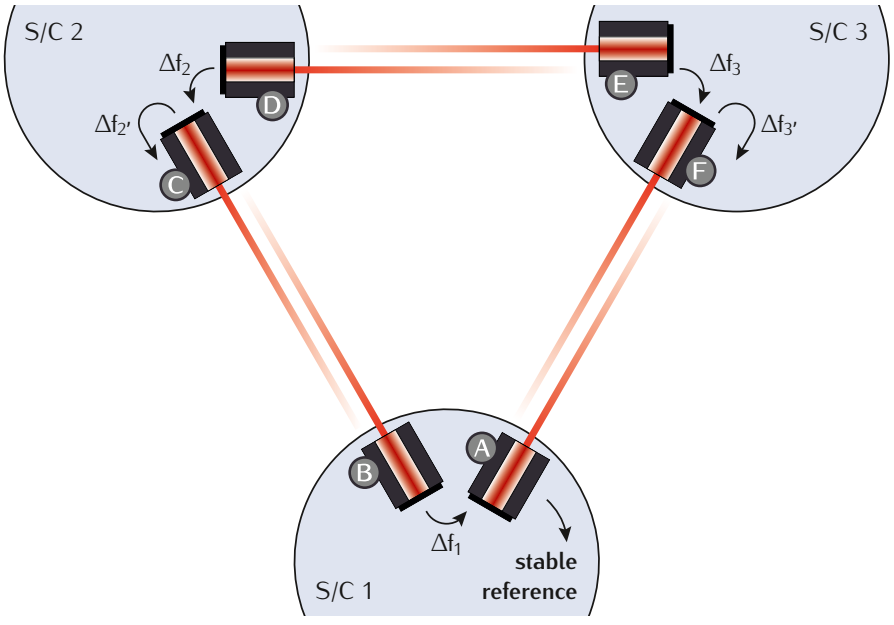


Figure 1.13: Possible locking scheme for Classic LISA. One laser (A) is locked to a stable frequency reference, all other lasers throughout the constellation (B…F) are frequency locked to another laser, either to an on-board one or to the incoming light of a remote laser. Arrows indicate which laser uses which reference. All of these locks have adaptable offset frequencies Δf_1 to $\Delta f_{3'}$.

- Avoid the frequency range dominated by laser power noise
- Have as few offset lock frequency adaptations as possible

The range dominated by laser power noise was measured to be $-5 \ldots 5\,\mathrm{MHz}$ for NPRO lasers that will be used for LISA [19]. This leads to a lower heterodyne frequency limit of 5 MHz. As we will see later in Section 2.1.2 it is beneficial to add another tone at exactly 5 MHz. Also there will be side tones 1 MHz above and below the main heterodyne frequency as described in Section 2.1.3. Since we cannot allow any tones to overlap with the 5 MHz tone, we have to limit the minimum heterodyne frequency to about 6 MHz. Consequently the main heterodyne frequency has to be kept above 7 MHz.

Using a genetic optimization algorithm it could be found that for the described locking scheme one can in fact keep all heterodyne frequencies within a range of $7 \ldots 23\,\mathrm{MHz}$. An exemplary frequency plan that shows the different offset lock frequencies over time is shown in Figure 1.14 (top). The remaining heterodyne frequencies that are not locked and thereby influenced by a summation of Doppler shifts are shown in Figure 1.14 (bottom).

Adding the 1 MHz side tone, and applying some margin, we can conservatively set the maximum heterodyne frequency for Classic

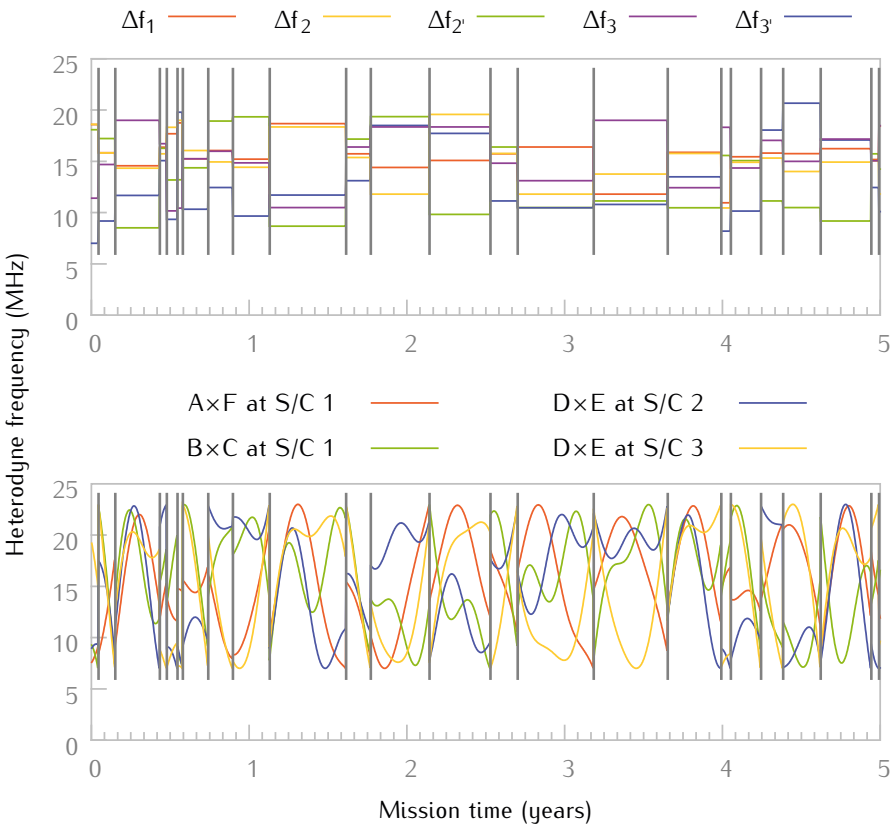


Figure 1.14: Frequency plan (top) and resulting heterodyne frequencies of the remaining beat notes (bottom) for Classic LISA according to the locking scheme shown in Figure 1.13. All frequencies can be kept within a range of $7 \ldots 23\,\mathrm{MHz}$. Times where it is necessary to adapt the offset lock frequencies are highlighted by vertical lines.

LISA to 25 MHz. This applies to all requirements mentioned in this document. For eLISA (2013) due to the much lower Doppler shifts the maximum heterodyne frequency might be as low as 10 MHz and many requirements could be relaxed by a factor of 2 or more.

Since otherwise all other requirements on instruments and payload for Classic LISA and eLISA (2013) are almost identical, **we will only consider the Classic LISA mission concept hereafter**. If whatever solution we find works for Classic LISA, it most certainly works for eLISA with some margin.

1.4 LISA PATHFINDER

Most technologies necessary for a LISA mission were already developed and will be tested in space by a technology demonstration mission named "LISA Pathfinder" (formally known as "SMART-2"). Featuring one LISA arm shrunk to 40 cm in length, this ESA mission will be able to test all disturbances that act locally inside a LISA spacecraft.

In particular, LISA Pathfinder will verify in space:

- Gravity reference sensors (proof masses in electrode housing), free of disturbing accelerations at the $10^{-14}\,\mathrm{m/s^2/\sqrt{Hz}}$ level
- NPRO lasers and the local laser interferometry for proof mass readout at pm level
- Cold gas micro-thrusters (for drag-free control)

The LISA Pathfinder spacecraft will follow one freely floating proof mass by reading out its position with capacitive sensors and laser interferometry as shown in Figure 1.15, and actuates the spacecraft's

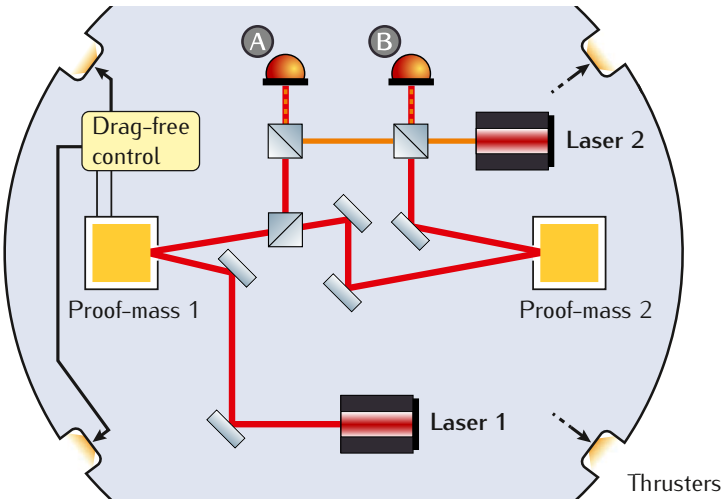


Figure 1.15: Lasers are used to read out the motion of the first proof mass (detector A) and the differential motion between both masses (detector B). While one proof mass is drag-free and the spacecraft follows its position by micro-thrusters, the other one is free floating except for a very gentle electrostatic suspension to prevent runaway. Their differential acceleration reveals the spurious forces at the $1 \times 10^{-14}\,\mathrm{m/s^2/\sqrt{Hz}}$ level.

position with micro-Newton thrusters. Just like in the LISA mission, the second proof mass is kept in position relative to the spacecraft by capacitive actuators low bandwidth suspension controller. In that sense LISA Pathfinder is a highly accurate gravimetric sensor that measures differences in the gravitational force between the two proof masses, i.e., a gravity gradiometer.

Figure 1.16 shows the fully assembled LISA Pathfinder spacecraft with the propulsion module attached during environmental and performance tests inside a space simulator in August 2011. It is to be launched in 2015 and will perform its experimental schedule at the L1 Lagrangian point within three months. Results will be available almost immediately, through real-time data analysis.

Although LISA Pathfinder also uses heterodyne interferometry, the signals are not subject to Doppler shifts and are set to a constant kHz frequency making the phase read-out easier. Hence LISA technology related to inter-spacecraft interferometry is currently being separately developed and tested on ground, in particular in the context of this project:

- Phase measurements for frequencies up to 25 MHz
- Adjustable offset frequency laser locks
- Laser frequency noise suppression
- Optical inter-spacecraft data communication

These items together are at the core of the **LISA Metrology System** (LMS). Within the scope of this project an international team developed a fully functional **TRL 4** compliant prototype making the LISA Metrology System available as European only contribution for the very first time. ■

The **LISA Metrology System** was developed to **Technology Readiness Level 4** specifications (component and/or breadboard validation in laboratory environment).

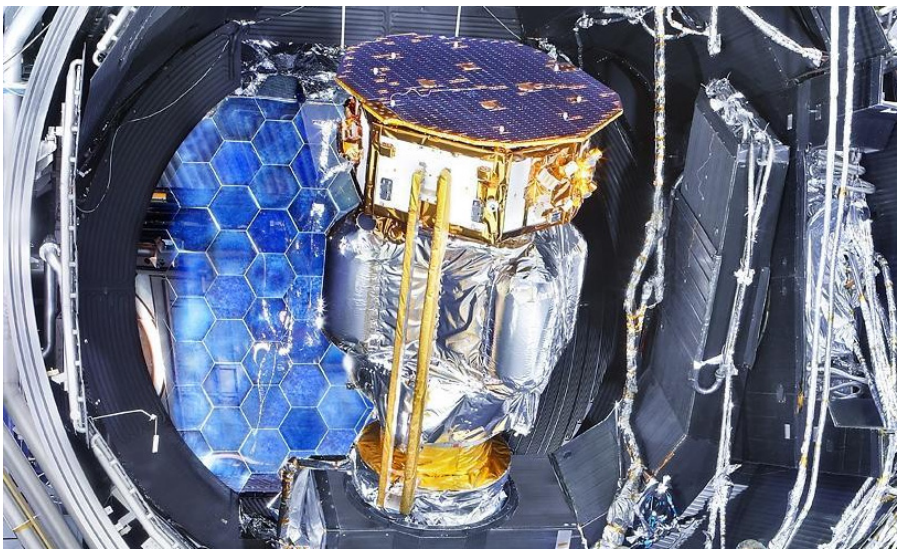


Figure 1.16: The LISA Pathfinder spacecraft with attached propulsion module inside a space condition simulation chamber at IABG (Germany) in August 2011. *© ESA / Airbus / IABG*

2 METROLOGY SYSTEM

The main function of the LISA Metrology System (LMS) is the continuous and simultaneous phase measurement of multiple heterodyne signals at frequencies between 5 and 25 MHz with µcycle precision. In LISA, the phase of the beat note between the incoming laser beam from a distant spacecraft and a local oscillator laser is proportional to distance fluctuations between the three spacecraft and thus carries the gravitational wave information. Beat notes from other laser interferometers measure fluctuations of the proof mass position and auxiliary lengths for noise cancellation in post processing. All measurements have to be performed with extremely low noise and hight stability over thousands of seconds.

As discussed in Section 1.3.4 **we derive all requirements from the more demanding Classic LISA mission concept** with 1064 nm laser interferometry, a maximum heterodyne frequency, f_{het}, of 25 MHz, and a shot-noise limited target sensitivity for the phase read-out of 10 pm/$\sqrt{\text{Hz}}$ equivalent total length measurement noise (single link).

We are working with a maximum noise budget of 1 pm/$\sqrt{\text{Hz}}$ to the phase measurement system. This translates to a phase noise requirement 6 µrad/$\sqrt{\text{Hz}}$ which is relaxed proportional to f^{-2} below 3 mHz due to the dominance of acceleration noise to

$$6 \times \sqrt{1 + \left(\frac{2.8 \times 10^{-3}\,\text{Hz}}{f}\right)^4}\ \mu\text{rad}/\sqrt{\text{Hz}} \quad ,$$

valid for Fourier frequencies, f, between 10^{-4} and 1 Hz. Even if not explicitly mentioned, **this frequency shaping function is present in all requirements derived in this document.**

Additionally, the LMS has to control laser frequency locks, provide inter-spacecraft ranging, and handle optical data communication.

2.1 PHASE MEASUREMENT SYSTEM

As described in detail in Section 3.1, many techniques to measure a signal's phase—like zero-crossing or down-mixing—have been discarded due to significant disadvantages. A phase-locked loop (PLL) operating directly at the signal frequency is currently the preferred

architecture for a LISA Phase Measurement System.

To remove excess noise and reach the required performance, one must apply additional corrections schemes. This is necessary due to limitations in current analogue-to-digital converter and reference oscillator technologies.

2.1.1 ALL-DIGITAL PHASE-LOCKED LOOP

The chosen PLL principle for measuring a signal's phase is shown in Figure 2.1. The input signal is mixed with a sine wave of equal frequency and phase that is generated by an **adjustable oscillator**. This produces products near DC and at twice the signal frequency. A low-pass filter removes the $2f$ component and other spurious signals.

For an analog PLL implementation, this **adjustable oscillator** would be, e.g, a VCO.

A digital phase-locked loop (DPLL) as utilized by the PMS is the digital implementation of the PLL described above. It uses digital multipliers and filters, and a numerical controlled oscillator (NCO) which form one DPLL core as shown in Figure 2.2. Input signals are digitized by an analog-to-digital converter (ADC).

Such a DPLL can track a signal even when its frequency changes due to Doppler shifts. Also the bandwidth can be tuned to allow the **independent tracking** of several beat notes in a single input signal. The key components of a DPLL are:

Independent **simultaneous tracking** is made possible by using several DPLL cores on the same digitized signal.

Q MIXER OUTPUT: A proportional-integral (PI) controller keeps the mixer output (Q) very close to zero by actuating the oscillators frequency. Thus this technique tracks the signal's instantaneous frequency $f(t)$. The purpose is to produce a precisely tracking copy of the incoming sine wave, but in digital form.

PIR VALUE: The NCO consists of a phase increment register (PIR), a phase accumulator (PA), as well as a sine and a cosine look up table (LUT). Its instantaneous output frequency is determined by the cur-

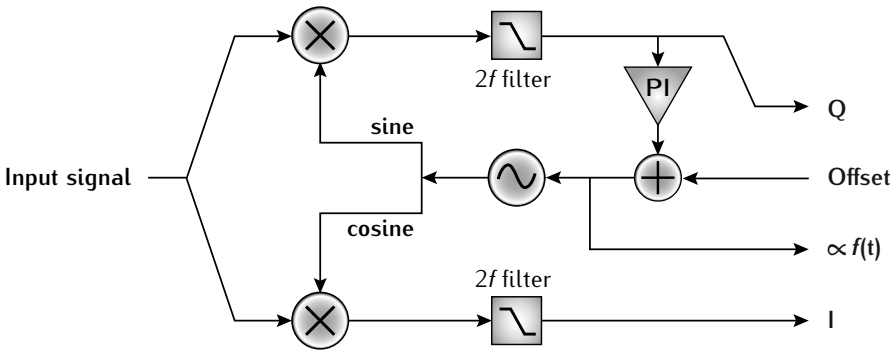


Figure 2.1: In an analogue PLL a signal is mixed with a sine and cosine produced by an adjustable oscillator. A PI controller locks onto the input signal and keeps the sine channel at zero by actuating the oscillator's frequency. This information can be used to reconstruct the signal's phase while the cosine channel represents the signal's amplitude.

rent value in the PIR that is controlled by an initial frequency, f_0, and the current value of the PI controller. This frequency data is used to reconstruct the signal's phase changes over time $\phi(t)$.

For a set of frequencies $\{f_1, f_2, \ldots, f_n\}$ the corresponding phase is described by

$$\phi_n = 2\pi \frac{1}{f_s} \sum_{i=1}^{n} (f_i - f_0) \ , \tag{3}$$

where f_s^{-1} denotes the time between two samples (inverse sampling time) and f_0 could in principle have an arbitrary value but should usefully be the initial frequency or an average of all frequencies.

I MIXER OUTPUT: When mixing the input signal with a sine wave 90° out of phase (cosine) the low-pass filtered mixer output (I) represents the **instantaneous amplitude** of the input signal. This information is beneficial in many ways. For example it can be used to correct for imperfections of the PLL where Q is non-zero and therefore describes the difference between the phase of the actual input signal and that of the oscillator. A correction term $\Delta\phi$ can be computed by

The **instantaneous amplitude** is assumed to be only slowly varying in normal operations.

$$\Delta\phi = \arctan\left(\frac{Q}{I}\right)$$

that is added to the value calculated by Equation 3 to measure the signal's phase with higher fidelity. It also helps in forming weighted combinations of signals and is a diagnostic quantity in lock acquisition.

PA VALUE: Using the PIR, Q and I values, the signal's phase can be reconstructed only with an unknown offset. The **instantaneous phase** is available in the phase accumulator (PA), but not easy to process due to its rapidly ramping form. The difference between two PA

Differential Wavefront Sensing (DWS) utilizes the **instantaneous phase** to recover the differential phase between signals on quadrant photodiodes. It provides very precise spacecraft and proof mass alignment information.

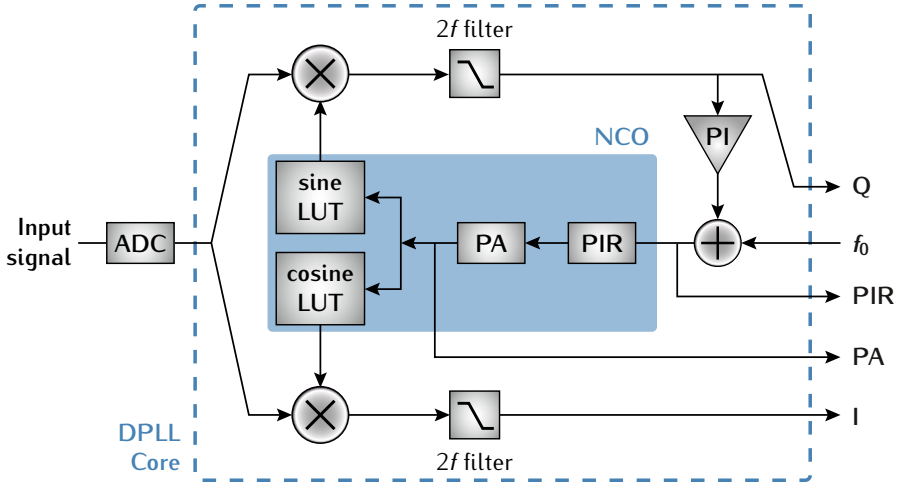


Figure 2.2: In a digital PLL all elements are digital. The oscillator (NCO) is controlled by an initial frequency, f_0, and the current value of the PI controller. Combined they set the value in the phase increment register (PIR) which holds the frequency information for phase reconstruction. The phase accumulator (PA) value is used to obtain the instantaneous phase for Dynamic Wavefront Sensing (DWS).

values of PLLs that track the same frequency can however be used e.g. in DWS.

In combination the 4 quantities (PIR, PA, Q, I) are a complete description and in the digital domain of the input signal's sinusoidal component at the frequency of interest.

In order to reach the required fidelity of $6\,\mu\mathrm{rad}/\sqrt{\mathrm{Hz}}$, **we have to make sure that no component or algorithm in the signal path adds excess phase noise** above this level.

2.1.2 ADC JITTER CORRECTION

One of the very first components in the phase measurement system is the analogue-to-digital converter (ADC) which is triggered by a sampling clock. Intrinsic timing jitter within the ADC leads to a digitization of the input signal at non-equidistant intervals so that the digital replica is distorted. Assuming a perfect external sampling clock and a 25 MHz heterodyne signal a requirement for the ADC timing accuracy arises as

$$\frac{1\,\mathrm{pm}/\sqrt{\mathrm{Hz}}}{1064\,\mathrm{nm}} \times \frac{1}{25\,\mathrm{MHz}} \approx 4 \times 10^{-14}\,\mathrm{s}/\sqrt{\mathrm{Hz}}\,. \tag{4}$$

One cannot distinguish between apparent phase shifts due to ADC timing jitter and a genuine gravitational wave signal. The timing requirement can also be expressed as phase noise limit for the sampling clock. Since the sampling frequency f_s needs to be at least twice the maximum signal frequency, a 80 MHz clock was chosen. The $6\,\mu\mathrm{rad}/\sqrt{\mathrm{Hz}}$ requirement then simply relaxes by the ratio of f_s over f_{het}:

$$2\pi \times \frac{1\,\mathrm{pm}/\sqrt{\mathrm{Hz}}}{1064\,\mathrm{nm}} \times \frac{80\,\mathrm{MHz}}{25\,\mathrm{MHz}} \approx 19\,\mu\mathrm{rad}/\sqrt{\mathrm{Hz}}\,. \tag{5}$$

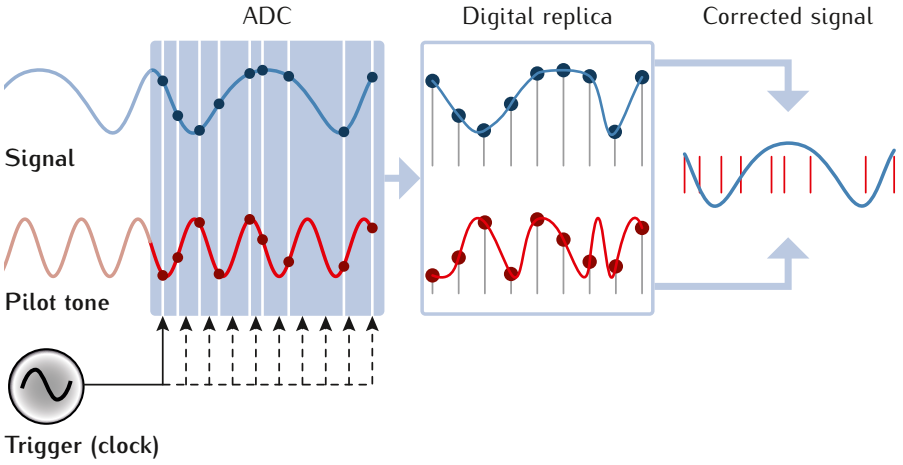


Figure 2.3: Although we assume a perfect clock, the signal is digitized at non-equidistant intervals due to intrinsic noise of the ADC. The digital replica of the signal will deviate from the original. To measure the intrinsic noise and remove it from the measured signal, a reference signal at different frequency (pilot tone) is digitized simultaneously by the same ADC.

Unfortunately, all ADCs under test fail this requirement and spoil the system performance. As illustrated in Figure 2.3, one solution to this problem is the introduction of a system wide clean and stable reference signal ("pilot tone"). This additional signal will be superimposed onto each ADC channel and hence will be affected by the same ADC sampling time jitter. It is tracked by a dedicated DPLL core.

Since the pilot tone is stable at a well known frequency it can be used to measure ADC timing jitter. This information can be used for **correcting** the signal. Phase noise introduced by an unstable sampling clock is indistinguishable from ADC timing jitter and will be removed in the corrected signal by the same principles. Thus the pilot tone in generally removes the extreme stability requirements on the sampling clock itself and becomes a constellation-wide reference which all measurements are compared to.

There are several options for **correcting** the signal (removing ADC timing jitter) all of which can be found in technical note 2-1 [TN21].

All requirements are now carried over to the pilot tone itself, and thus the oscillators producing it on the different spacecraft.

We decided to use a pilot tone frequency, f_p, of 75 MHz. Although it is **under-sampled** by the 80 MHz sampling clock and hence will be aliased down to 5 MHz, the 6 µrad/$\sqrt{\text{Hz}}$ requirement still relaxes at the ratio of f_p over f_{het} to

$$\frac{1\,\text{pm}}{1064\,\text{nm}} \times \frac{75\,\text{MHz}}{25\,\text{MHz}} \approx 18\,\mu\text{rad}/\sqrt{\text{Hz}} \tag{6}$$

which corresponds to the exact same 40 fs/$\sqrt{\text{Hz}}$ timing requirement as described by Equation 5. Unfortunately, an oscillator that stable does not exist. Figure 2.4 demonstrates that even laboratory setups with state of the art cryocooled sapphire oscillators violate the required stability. [20] Space-qualified low-power oscillators that would be applicable for LISA are much worse.

A shift by a certain phase angle in the original **under-sampled** frequency (75 MHz) translates to a phase shift 15 times smaller in the aliased 5 MHz signal. Hence even though the pilot tone will be measured at 5 MHz one can still use to the requirement referred to the original frequency.

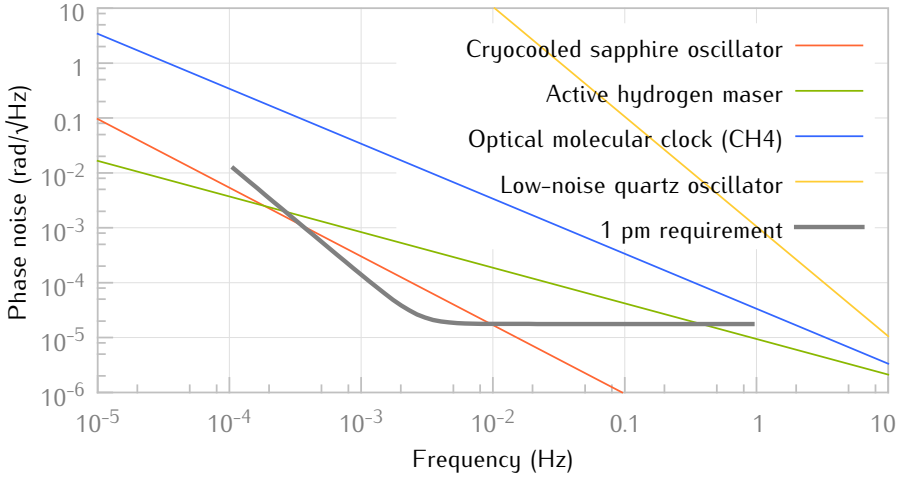
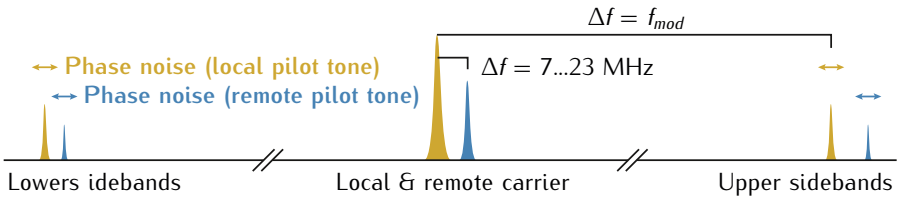


Figure 2.4: Rough trends of the SSB phase noise (linear power spectral density) over Fourier frequency for different reference oscillators. Even cryocooled dielectric-sapphire-resonator oscillators at 6 K (red) violate the 1 pm requirement. A more realistic choice for a LISA reference oscillator would be closer to the yellow trace for low-noise quartz oscillators. All data were scaled for a 75 MHz carrier.

2.1.3 PILOT TONE JITTER CORRECTION

We thus have to deal with the excess phase noise of free-running oscillators that generate the pilot tones. The basic idea is to measure the differential phase noise between the pilot tones of the three different spacecraft and send this information back to Earth. Here it can be used in post processing to subtract the noise contribution.

Such an implementation requires the transmission of the pilot tone's phase noise information between the spacecraft. This can be done easily by using the pilot tone to phase modulate the carrier wave of the outgoing laser beam with an electro-optic modulator (EOM) as sketched in Figure 2.5. The resulting sidebands that hold the **phase noise information** of the respective pilot tones are shown below.



Sideband picture of the local (yellow) and remote (blue) laser beams. The upper and lower sidebands hold the **phase noise information** of the pilot tones.

After interference, the heterodyne signals now contain two additional beat-notes (sideband/sideband beat-notes) which—on top of the gravitational wave signal—yield the differential phase noise between the pilot tones.

The sideband/sideband beat-notes are separated from the carrier/carrier beat-note by the difference in modulation frequency f_{mod}. Hence the frequencies of the phase modulation on the local and the remote spacecraft must differ by at least ≈1 MHz so that DPLL cores can track the three beat-notes individually.

To retain a strong carrier signal for the main science measurement only a small fraction of the laser power is carried in the sidebands. It was proposed to have 7.5 % of the respective carrier power in each single sideband. Thus the **combined readout** of both sideband/sideband beat-notes per heterodyne signal contains an equivalent length measurement noise of $93\,\mathrm{pm}/\sqrt{\mathrm{Hz}} \equiv 546\,\mu\mathrm{rad}/\sqrt{\mathrm{Hz}}$. This excess phase noise due to the lower signal-to-(shot)-noise ratio violates the $18\,\mu\mathrm{rad}/\sqrt{\mathrm{Hz}} \equiv 40\,\mathrm{fs}/\sqrt{\mathrm{Hz}}$ requirement for the pilot tone stability as described in Equation 6.

A detailed calculation of the **combined readout** noise for the sideband/sideband beat-notes can be found in technical note 2-1 [TN21].

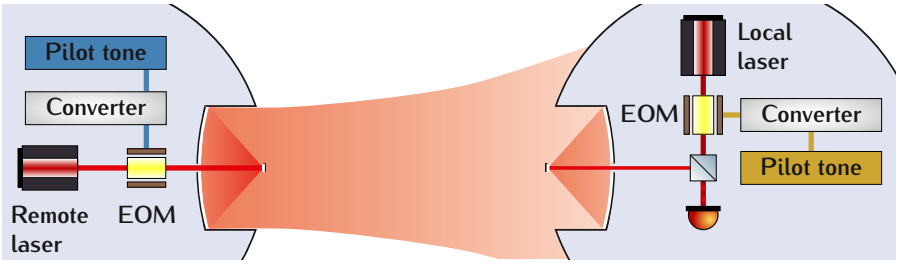
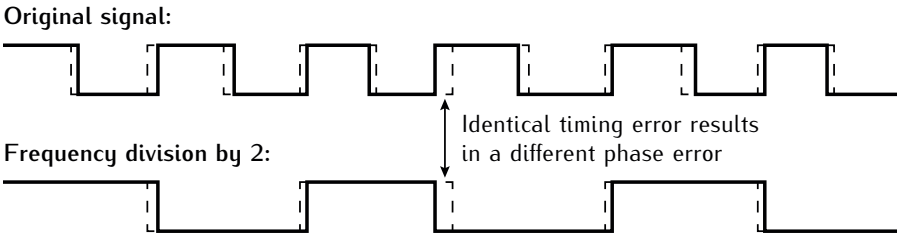


Figure 2.5: Remote and local pilot tones are phase modulated onto the laser beams by electro-optic modulators (EOM). The phase noise needs to be converted to achieve the required readout sensitivity.

As a result one cannot use the pilot tones directly for the phase modulation. Instead, any phase noise in the pilot tones needs to be upscaled by a factor of at least 31 so that a read-out noise of $546\,\mu\text{rad}/\sqrt{\text{Hz}}$ would still be sufficient to measure the pilot tone phase noise with required accuracy.

In contrast to the mixing process in, e.g., heterodyne interferometry or electronic mixers, which maintain phase information, frequency dividers and multipliers do conserve timing jitter. This leads to a **scaling of phase noise** by the respective frequency ratio as illustrated below.



Noisy square wave signal (top, solid) with ideal representation (dashed line) and corresponding signals after frequency division (bottom). Timing errors are conserved which leads to a **scaling of phase noise**.

This conversion of phase shifts makes these devices ideal for scaling the pilot tones' phase noise.

After a long run of pre-experiments as described in Section 3.3 we decided on a reference oscillator frequency of $f_{mod} = 2.4\,\text{GHz}$ for the phase modulation and a frequency devision by 32 to obtain a $f_p = 75\,\text{MHz}$ pilot tone that meets the scaling requirements between f_{mod} and f_p (downconversion of reference oscillators' phase noise by a factor of 32). Modulation frequencies between different laser links will differ by 1 MHz to get sideband/sideband beat-notes at 1 MHz above and below the carrier/carrier beat-note, now using up a heterodyne signal bandwidth of 6 ... 24 MHz as illustrated in Figure 2.6. The 80 MHz sampling clock can be derived from a frequency division by 30 out of the same 2.4 GHz reference oscillator. The 1 MHz difference between the reference oscillator frequencies may shift the pilot tones between Phase Measurement Systems by ≈ 30 kHz. This has no impact on the PMS design or any stability requirements.

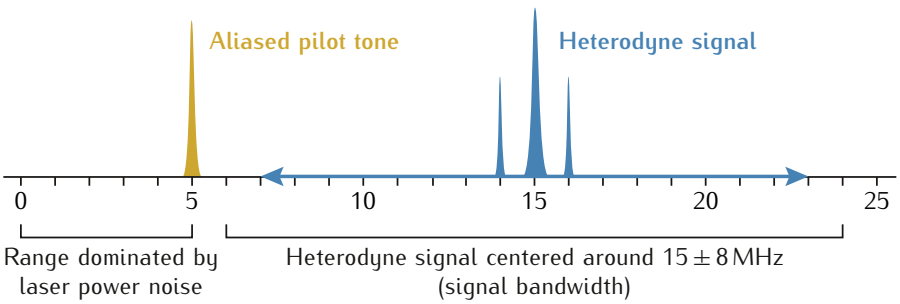


Figure 2.6: Down-aliased pilot tone at 5 MHz and heterodyne signal with sideband/sideband beat-notes 1 MHz above and below the carrier which is centered around 15 MHz and shifted by ±8 MHz due to Doppler shifts resulting in a signal bandwidth of 6 ... 24 MHz.

The final ADC and pilot tone jitter correction scheme for the Phase Measurement System is shown in Figure 2.7. The differential timing noise between the two 2.4 GHz reference oscillators can be measured via the sideband/sideband beat-notes in a local reference interferometer, and by electronically mixing both oscillator signals down to their 1 MHz difference frequency and passing it to the PMS. The phase noise of this signal will be read out via a dedicated DPLL core. With no optical signal present, the frequency range in this channel will not be dominated by laser power noise.

The $40\,\mathrm{fs}/\sqrt{\mathrm{Hz}}$ timing requirement that could not be met with ADCs and reference oscillators alone is now instead imposed upon all components of the pilot tone conversion and transfer chain highlighted in blue. On the one hand this concerns all electrical cables [21], electro-optic modulators [22], optical amplifiers [23–25], and any fibers cables [22] present in the GHz signal lines. Candidates for all of these components that meet the requirements were already identified. On the other hand also all components between the reference oscillators and the actual pilot tone—i.e., cables, dividers, adders, and filters—as well as the mixer that produces the difference frequency between both oscillators are affected by the same timing requirement. These components (highlighted in yellow) are combined in the Fre-

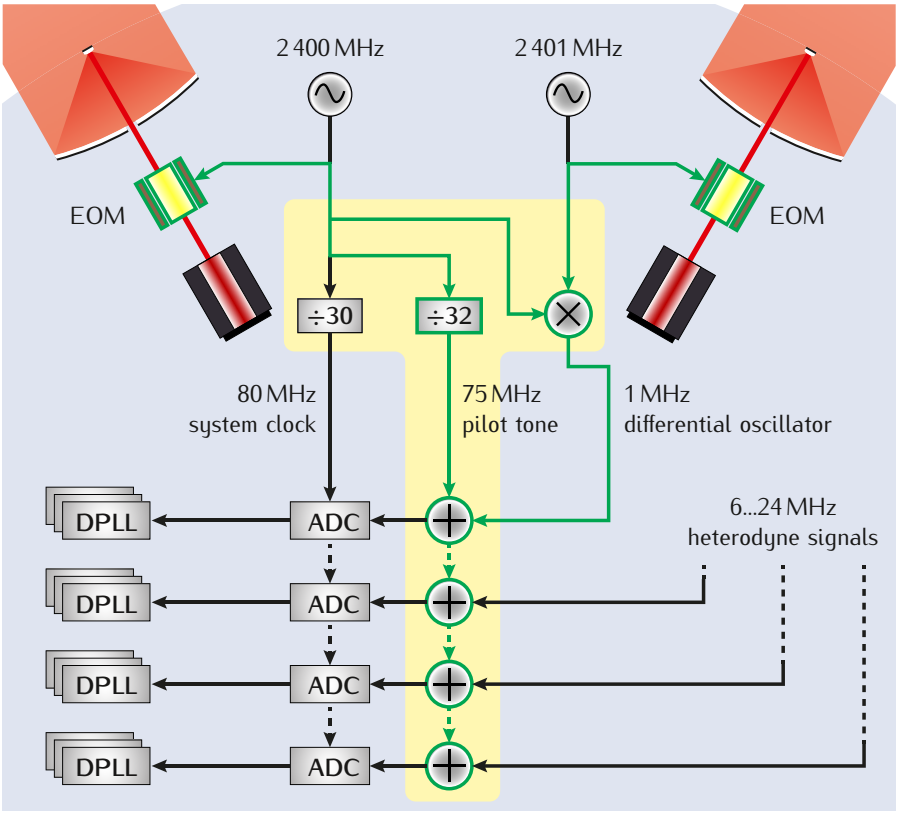


Figure 2.7: Scheme presenting the ADC and pilot tone jitter correction. EOMs modulate the outgoing laser beams by reference oscillator frequencies at 2.4 GHz. This transfers their phase noise in sidebands to the distant spacecraft where it can be compared to the local oscillators' noise. Dividers downconvert the phase noise of the oscillators and produce the sampling clock and a pilot tone. The latter is added to each channel of the Phase Measurement System and will be used to correct for intrinsic ADC timing jitter. Multiple DPLL cores per channel track the different signal frequencies individually. Components and signal lines that must meet the $40\,\mathrm{fs}/\sqrt{\mathrm{Hz}}$ timing requirement are highlighted in green.

quency Generation and Distribution Subsystem (FDS) which was developed as part of the LISA Metrology System.

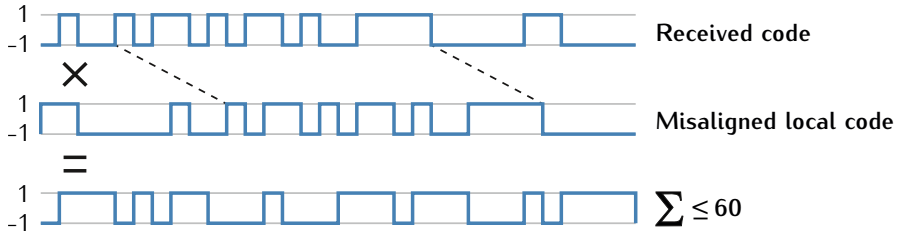
2.2 AUXILIARY FUNCTIONS

In addition to the primary length measurement, the LISA Metrology system has to perform several auxiliary functions. Among those are beat-note acquisition, offset frequency locking of slave lasers, and inter-spacecraft ranging and data transfer.

2.2.1 RANGING

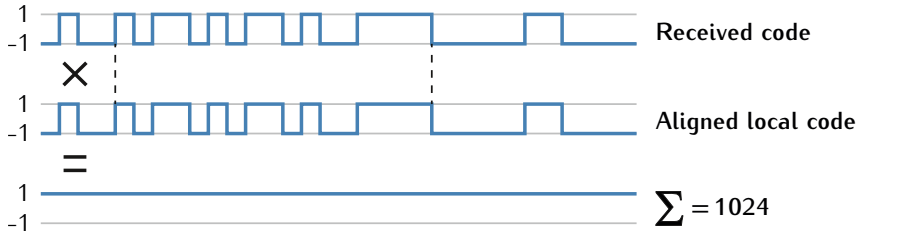
While the laser interferometric phase measurement determines relative distance fluctuations between spacecraft down to some $\mathrm{pm}/\sqrt{\mathrm{Hz}}$, the absolute distance also needs to be measured with sub-meter accuracy. Time Delay Interferometry (TDI) algorithms require this information to calculate correct time delays so that laser frequency noise is removed from the data streams in post processing. [26, 27] The deep-space network (DNS) yields an absolute inter-spacecraft distance with an accuracy of $\approx 25\,\mathrm{km}$ only. Hence an individual absolute distance measurement, ranging, is required.

The ranging mechanism is based on Direct Sequence Spread Spectrum (DS/SS) modulation: A pseudo-random noise (PRN) code with an even length of 1024 chips is transmitted to the distant spacecraft. The Modulation is implemented as low-level binary phase modulation. At the other end, the received code is correlated with a local copy of the same code. The code was designed to have a correlated sum ≤ 60 if **misaligned** by one chip or more.



When the received and the local copy of the PRN code is **misaligned** by one chip or more, the autocorrelated sum is close to zero. It can also be negative, but its absolute value will be ≤ 60.

If both codes are **aligned**, the autocorrelated sum equals 1024.



When the received and the local copy of the PRN code are perfectly **aligned**, the autocorrelated sum = 1024.

This ranging mechanism is implemented by phase modulating the PRN codes onto the optical carrier of each laser using ≈1 % of the

light power. As a result, the PRN code shows up as phase errors in the received heterodyne signal at the DPLLs Q mixer output since they are faster than the PLL loop bandwidth. These phase errors are passed to a delay-locked loop (DLL) within the Phase Measurement System which keeps a local copy of the PRN code aligned to the received code via correlation of both sequences. The code delay necessary to maintain the code alignment yields the ranging information together with the absolute clock offset. This can be disentangled in post processing. Experiments performed under real conditions in preparation for this work (1 pW received light power modulated at a depth of 0.1 rad) could show that this technique provides a ranging accuracy of 42 cm at 3 Hz sampling rate. [28, 29]

2.2.2 DATA TRANSFER

The ranging mechanism is also used to transmit binary data between the spacecraft. The data is encoded on top of the PRN code by bitwise operation (XOR) at lower rates so the code length of 1024 chips is divided into several data periods. At the distant spacecraft this data must be directly decoded from received PRN code within the Phase Measurement System.

The full spectrum of the heterodyne signal is shown in Figure 2.8 including the carrier/carrier beat-note at 15 MHz with upper and lower pilot tone sideband/sideband beat-nones 1 MHz above and below, as well as PRN DS/SS modulation with data encoding. While at a received light power of 10 nW all modulations are clearly visible, the DS/SS modulation is completely buried in the shot noise in a realistic heterodyne signal measured at 1 pW received light power. This is typical for spread spectrum signals, which can only be recovered to a level above the noise by 'unspreading' them with a copy of the modulation code. Experiments performed under real conditions (1 pW received light power modulated at a depth of 0.1 rad) allowed for data

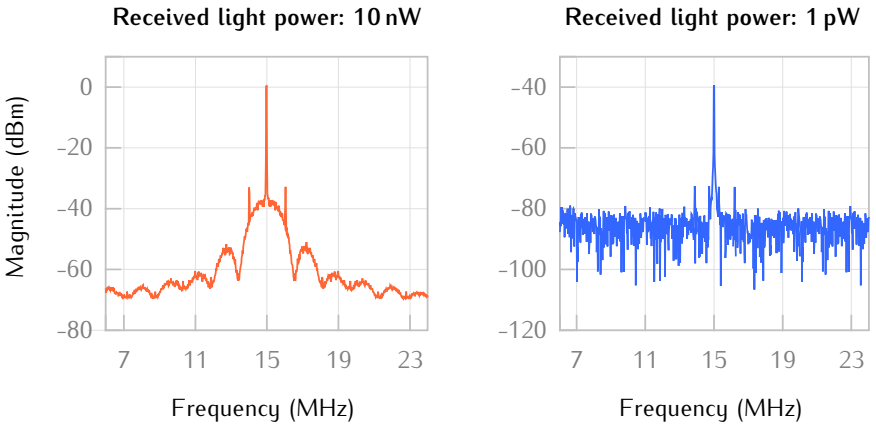


Figure 2.8: Heterodyne spectrum comparison (experimental data) for received light power of 10 nW (red) and 1 pW (blue). Carrier/-carrier beat-note at 15 MHz with upper and lower pilot tone sideband/sideband beat-nones 1 MHz above and below. Shot-noise is covering the DS/SS modulation in the case of weak light.

rates of 24.4 kbit s^{-1} with a bit error rate $< 26 \times 10^{-3}$ that was totally eliminated using Reed-Solomon encoding [30].

2.2.3 BEAT-NOTE ACQUISITION AND LASER FREQUENCY LOCK

While each DPLL can track a different frequency, it needs to know which exact frequency to lock onto. Since at first the beat-note frequency is completely unknown, another auxiliary function of the LISA Metrology System is the initial acquisition of the beat-note. This is accomplished by a Fast Fourier Transform (FFT) in combination with a peak finding algorithm.

The LISA Metrology System furthermore needs to be able to offset frequency lock the different lasers. This means, once the carrier/carrier beat-note was identified, it must be capable to keep the beat-note at a constant value by continuously tuning the frequency of a local laser. A piezoelectric element at the laser crystal allows for a fast control of laser frequency while temperature adjustments on the crystal can compensate for long-term frequency drifts. The LISA Metrology System will be able to control both of these actuators.

A functional overview of the LISA Metrology System for one laser link is shown in Figure 2.9. In reality, all optical components, e.g., mirrors and beam splitters, will be attached to an optical bench utilizing hydroxide catalysis bonding. In the present baseline concept, there

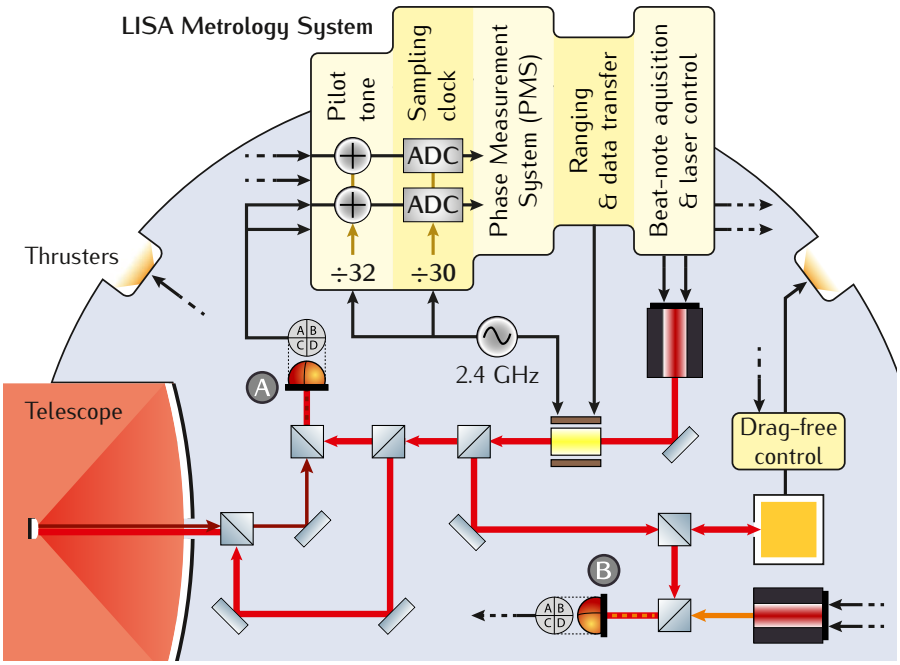


Figure 2.9: Simplified functional overview of the LISA Metrology System for one laser link. Quadrant photodiodes are used to enable Differential Wavefront Sensing (DWS) to get not only the position but also the alignment information for the distant spacecraft (detector A) and the proof mass (detector B). This requires a multitude of phase measurement channels. The alignment information with respect to the incoming beam for both, proof mass and spacecraft, is used in the Drag-free Attitude Control System (DFACS). All interactions between systems are shown as black arrows, where dashed lined arrows also go to the PMS.

will be one of these benches per laser link. Light from the lasers and between benches is transmitted via optical cables.

2.3 REQUIREMENTS OVERVIEW

The project's goal was the design, development, manufacturing, testing and validation of a breadboard model of the LISA Metrology System. This includes a 20 channel phase measurement and 4 channel laser offset frequency locking system, the Frequency Generation and Distribution Subsystem (FDS) as well as a Digital Signal Simulator (DSS) for the generation of signals identical to expected interferometric LISA signals. The following describes the key requirements and our implementation that achieves them.

2.3.1 FREQUENCY GENERATION AND DISTRIBUTION SUBSYSTEM (FDS)

All frequencies that determine the payload timing and phase measurement performance are coherently derived by frequency devision using a 2.400 GHz oscillator as primary reference. The timing fidelity between each pilot tone and the primary reference needs to be at least $4 \times 10^{-14}\,\mathrm{s}/\sqrt{\mathrm{Hz}}$. A second oscillator at 2.401 GHz is compared to the primary reference by measuring the 1 MHz output of a frequency mixer. Since electronic mixers conserve phase shifts, the timing requirement for this signal is still referred to the original 2.4 GHz.

	Signal	Requirement
Sampling clock	80 MHz differential (square)	n/a
Pilot tone	75 MHz single ended (sine) 0.7 V_{p-p} (each)	$18\,\mu\mathrm{rad}/\sqrt{\mathrm{Hz}}$
GHz oscillator differential	1 MHz (sine)	$600\,\mu\mathrm{rad}/\sqrt{\mathrm{Hz}}$

2.3.2 PHASE MEASUREMENT SYSTEM (PMS)

Phase measurements are implemented as DPLLs (see Section 2.1.1) on multiple FPGAs. DSS signals at high and low power to noise densities (PND) were used to evaluate the performance of the Phase Measurement System (PMS). To test the required beat-note sensitivities, the principle of **zero measurements** was used. The following requirements are valid for measurements after application of the ADC jitter corrected.

For **zero measurements** two identical input signals are measured in individual channels. The difference of both measurements yields the system performance. Requirements refer to a single measurement. As mentioned on page 23 all requirements are relaxed proportional to f^{-2} below 3 mHz due to the dominance of acceleration noise.

	Requirement
75 dB Hz **carrier signal**	$12 \times 10^{-6}\,\mathrm{rad}/\sqrt{\mathrm{Hz}}$
95 dB Hz **carrier signal**	$6 \times 10^{-6}\,\mathrm{rad}/\sqrt{\mathrm{Hz}}$
75 dB Hz **sideband beat-note**	$83 \times 10^{-6}\,\mathrm{rad}/\sqrt{\mathrm{Hz}}$
Measurement bandwidth	0.1 mHz . . . 1 Hz
Sampling rate	3.3 Hz, 10 Hz and 100 Hz

2.3.3 BEAT-NOTE ACQUISITION

The beat-note acquisition is performed by means of FFTs of the sampled input data that are implemented on a field programmable gate array (FPGA). Once a signal is detected, the frequency is passed to the Phase Measurement System (PMS).

	Requirement
Signal power (PND)	75 dB Hz
Frequency drift	$> 4\,\mathrm{Hz\,s^{-1}}$
Lock acquisition	At frequency difference < 5 mHz
Maximum time to acquire lock	< 20 s
Accuracy	< 1 fringe

2.3.4 RANGING AND DATA TRANSFER

PRN codes including data are generated by the DSS and modulated onto the carrier beat-note signal. A DLL (see Section 2.2.1) is implemented in an FPGA where the PRN code is tracked and data is read out at 1.7 kHz.

	Requirement
Chip rate	1 . . . 3 MHz
Time delay	< 3 ns
Data rate	$> 15\,\mathrm{kbit\,s^{-1}}$ (averaged over 1 hour)
Bit error rate	$< 1 \times 10^{-6}$

2.3.5 LASER FREQUENCY CONTROL

A frequency control algorithm implemented on an FPGA compares the measured input frequency data with a given reference frequency value. This gives the error signal for a laser frequency control algorithm that keeps the heterodyne frequency at the reference value utilizing a digital proportional integral controller.

	Requirement
Analog outputs	$2 \times -10 \ldots 10\,\mathrm{V}$ (1 kΩ load)
Digital outputs	1 (serial)
Signal bandwidth	$> 100\,\mathrm{kHz}$
Phase measurement error	$< 120 \times 10^{-6}\,\mathrm{rad}/\sqrt{\mathrm{Hz}}$
Accuracy	< 1 fringe

2.3.6 DIGITAL SIGNAL SIMULATOR (DSS)

No tests with optical signals were required in this project. Thus realistic signals had to be electronically simulated that contain the main carrier/carrier beat-note with sideband/sideband beat-notes, PRN modulation, white amplitude noise, additional phase noise and simulated Doppler shifts.

	Signal	Amplitude
Total signal power		$-6 \ldots 3\,\mathrm{dBm}$
Main beat-note	$2 \ldots 25\,\mathrm{MHz}$	89 %
Sideband beat-notes	$\pm 1\,\mathrm{MHz}$	10 %
PRN modulation		1 %
White noise		Adjustable for power to noise densities (PND) of $75 \ldots 95\,\mathrm{dB\,Hz}$
Frequency drift	$4\,\mathrm{Hz\,s^{-1}}$	

This condensed overview of functions and requirements is not intended to be exhaustive. A complete list can be found in technical note 3-2 [TN32].

Chapter 7 on page 87 gives an overview of the testing and validation process where all functions were proven and all requirements have been met. ∎

Part II

DEVELOPMENT

The primary task of the technology development described in this report was to develop a breadboard model of the LISA metrology system (LMS). To do this the abstract functions and performance goals required of the LMS have to be realized in hardware, software and algorithms.

The complexity of the LMS, as well as the overall LISA metrology, required this to be an iterative process, which is advanced by a constant alternation between simulation, analysis, implementation and testing, with gradually increasing complexity. In this process not only the breadboard itself is advanced, but also the understanding of the relevant effects and design choices.

The development reported here therefore reflects these insights not only for one particular breadboard model, but also for the design of the LMS for future experiments and advancements.

3 DESIGN CHOICES

Over the course of many years different research groups world wide evaluated multiple phase measurement techniques. A digital phase-locked loop (DPLL) operating directly at the signal frequency was found to be the preferred architecture for a LISA Phase Measurement System (PMS). We verified these results and extended the research to a wider range of input signals and auxiliary functions.

Extensive preinvestigations on different pilot tone generation and distribution techniques within the scope of this project revealed many components that are not eligible for the Frequency Generation and Distribution Subsystem (FDS). The final design was driven by this findings and our implementation is the only one known to date that meets the rigorous timing requirements.

3.1 PHASE MEASUREMENT TECHNIQUES

A detailed investigation of different methods to measure the phase of a sinusoidal electrical signal has been conducted by the University of Glasgow and the Albert Einstein Institute (AEI) in Hannover in the years 2000 to 2002, prior to this project, in the context of the phase measurement system for LISA Pathfinder, where the frequencies to be measured are nearly fixed at 1.6 kHz.

The LISA Phase Measurement System (PMS) has to handle input frequencies that are much more demanding: Up to three low-level beat-notes (one carrier-carrier and two sideband-sideband) with different amplitudes and variable frequencies between 6 and 24 MHz that drift up to $4\,\mathrm{Hz\,s^{-1}}$ due to Doppler shifts in the constellation—plus a pilot tone set to 5 MHz—in a single input signal.

The following subsections present findings of numerous previous experiments at NASA/JPL, the University of Florida in Gainesville, the Australian National University in Canberra and the AEI in Hannover on different phase measurement techniques and their applicability for LISA.

3.1.1 ZERO-CROSSING TECHNIQUE

The phase of a single sinusoidal signal may be reconstructed by precisely measuring the time of the zero crossings after removing the DC component of the signal (i.e. AC coupling). A zero-crossing oc-

curs twice during each cycle and it is detected by a fast comparator, which can also be considered as a 1 bit analog-to-digital converter (ADC). The timing of the zero-crossings is determined relative to a fast clock that serves as reference. Independent experiments performed at the University of Glasgow [31] have shown that this method can indeed achieve µcycle/$\sqrt{\text{Hz}}$ sensitivities for signal frequencies below 100 kHz with a clock frequency of several 10 MHz. The sensitivity limit of this method is due to quantization noise. It can be shown that for a signal frequency of 20 MHz and a noise budget allocation of 3 µrad/$\sqrt{\text{Hz}}$ the required clock frequency would be 2.7 GHz which is not easy to achieve with space-qualified electronics.

The main problem with this method, however, is that it is not applicable for the case of multiple sinusoidal tones at different frequencies in the same input signal. While this could in principle be mitigated by complex filtering and DSP processing, the effort would in the end be much larger than for the DPLL method that we have selected, with no apparent benefit.

3.1.2 RE-USE OF THE LISA PATHFINDER PHASEMETER

Starting in 2001 the AEI in Hannover developed a phasemeter for the LISA Pathfinder mission. While it shares the main measurement principle of the LISA PMS developed in this project (digital I-Q-demodulation), the main difference is that the LISA Pathfinder heterodyne interferometer operates at a fixed and known frequency in the range between 1 and 2 kHz, as opposed to the drifting MHz signals of LISA.

Due to the success of the LISA Pathfinder phasemeter [32–34] and the fact that a space-qualified version had also been developed, it was briefly studied if it could be adapted for LISA as well. The idea had been to convert the MHz signal to a kHz signal by mixing it with a local oscillator and then operate the phasemeter at the kHz frequency.

Very soon, however, drawbacks of this approach were realized. Mixing the variable input frequency to a constant output frequency requires a tracking local oscillator, which to the required accuracy can only be realized by using a digital PLL, thus making this system more complex than directly using digital PLL as in our present architecture. More importantly, mixing the input signal to any other frequency than DC has a significant noise penalty, since the "mirror image" frequency (in a distance of two times the output kHz frequency from the desired input signal) will equally be converted to the same output frequency. Since at the image frequency there is no signal but the same noise (including shot noise), and filtering is unrealistic, an unacceptable degradation of the SNR by $\sqrt{2}$ results.

We hence conclude that the downmixing of the incoming signals to a smaller heterodyne frequency is unnecessary and has significant disadvantages. It is hence not considered any further.

3.1.3 DOWNMIXING FOLLOWED BY ZERO-CROSSING TIMING

One group in the US has for a short while further pursued a combination of the above two methods (downmixing to $1 \ldots 2\,\mathrm{kHz}$ followed by zero-crossing timing) [35]. Their conclusion was as well that there is a noise penalty of $\sqrt{2}$ for shot noise. Since LISA is designed to be limited in sensitivity mainly by shot-noise, such a degradation is unacceptable if it is avoidable (which it is using the DPLL architecture chosen for this project). Hence any methods based on downmixing to another (non-zero) frequency were not studied further.

3.1.4 DIGITAL PHASE LOCK LOOP (DPLL)

From about 2004, the thinking of three of the most active experimental groups worldwide in this field (NASA/JPL, University of Florida and AEI Hannover) converged to a digital PLL operating directly at the signal frequency (as described in Section 2.1.1) as the preferred architecture for a LISA phasemeter.

Initially the most intensive development took place at NASA/JPL, due to the fact that at the time it was assumed that the phasemeter would be a US contribution to the LISA mission.

Soon it was demonstrated that the required performance could thus be achieved [36, 37]. Early results from AEI in Hannover are described in a publicly available Ph.D. thesis [38].

3.2 LISA PMS BREADBOARDING EXPERIMENTS

The AEI in Hannover performed experiments with the goal to verify the results obtained by other research groups using DPLL as an instrument for phase measurements and to extend research to wider frequency range of input signals and auxiliary functions of the LISA metrology system.

3.2.1 PHASEMETER NOISE PERFORMANCE

Figure 3.1 shows a photograph of the PMS demonstration model developed in 2008 and tested prior to this project at the AEI in Hannover. Its components are located on a 4-layer specially designed Printed Circuit Board (PCB). Signals can be injected via 4 analog inputs that are digitized by 4 ADCs. These digitized data are further processed on

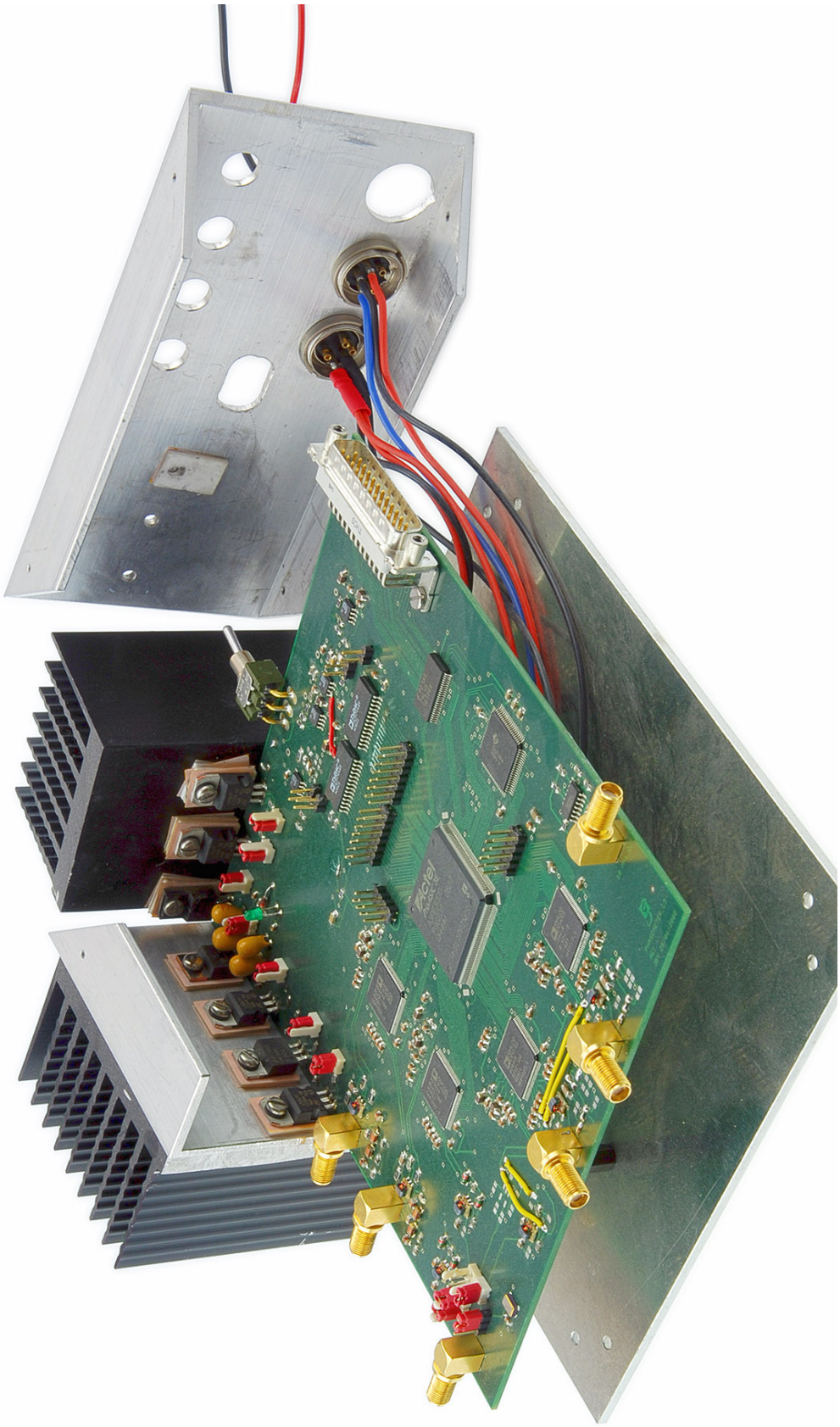


Figure 3.1: Photograph of the PMS demonstration model developed in 2008 at the AEI in Hannover. It features 4 analog inputs that are digitized by 4 individual ADCs. The 4-layer Printed Circuit Board (PCB) was custom designed. Although this early model did not provide all required functionality, LISA performance could be reached at a frequency range between 3 and 20 MHz.

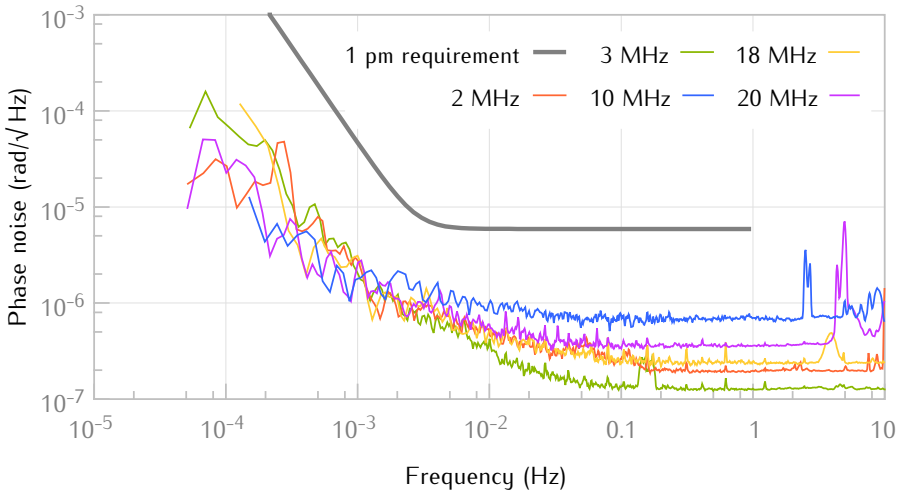


Figure 3.2: For input frequencies between 2 and 20 MHz the requirements are met

an FPGA. The system operates at 50 MHz sampling frequency which is generated by an on board crystal oscillator.

For determining the on-board phase noise of the PMS a zero measurement scheme was used. The most important feature of a this scheme is that noise introduced to the signal by any component before splitting cancels by subtraction, since it is the very same in both readout channels.

The phase difference noise on the output of the setup characterize then the phasemeter noise performance. The output signal of a frequency generator is split before being injected into two PMS channels. In Figure 3.2 the results for measurements with input frequencies between 2 and 20 MHz are shown.

3.2.2 LASER RANGING AND COMMUNICATION

A test-bed based on a Mach-Zehnder interferometer with a low-depth phase modulation scheme was built by the AEI in Hannover to provide a LISA-like signal under a coherent transponder configuration. Due to the stringent requirements of the LISA mission, the ranging scheme requires an experimental verification at picowatt power levels, and a ranging accuracy at sub-meter resolution with a highly reliable inter-satellite laser data communication.

This weak-light conditions combined with precise ranging measurements need to be demonstrated under fast signal dynamics and strong interferences.

The system dynamic performance was verified by tracking an artificial time-varying ranging signal representing the predicted orbital motion. In addition, the interference signals from the advanced laser

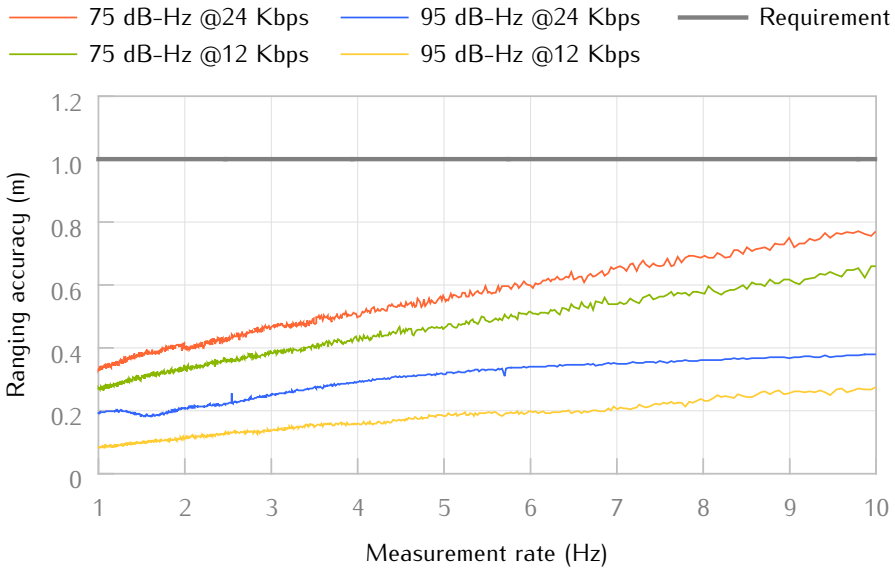


Figure 3.3: Ranging rms noise of the optical ranging measurements for different data rates and in the presence of LISA-like noise sources, including interference with a second PRN and simulated inter-spacecraft velocity.

link capabilities of the inter-satellite interferometry system—i.e., adjacent sidebands to the main beat note for clock noise transfer, and the cross-correlation between different codes in a laser link for bidirectional ranging measurements—were included in the experimental setup through additional phase modulations.

Under these conditions, the designed delay-locked loop (DLL) architecture achieves a sensitivity of $\approx 42\,\mathrm{cm}$ over a bandwidth of $\approx 3\,\mathrm{Hz}$ for data rates at $24.4\,\mathrm{kbit\,s^{-1}}$ (Figure 3.3). Detailed information about this experiment can be found in a paper by Delgado et al. [29] and in his Ph.D. thesis [28].

Although these experiments were initially conducted independently, they were merged with this project after its start. Due to the promising preliminary results, the digital phase-locked loop (DPLL) was selected to be the main instrument for phase measurement and other tasks like ranging for a LISA mission.

3.3 FREQUENCY DISTRIBUTION SUBSYSTEM

Early on experiments performed at the University of Florida and the AEI in Hannover, prior to this project, clearly showed that digital frequency dividers are superior to multipliers (synthesizers) in terms of phase fidelity. Hence a frequency division scheme to convert between the 2.4 GHz modulation frequency and the 75 MHz pilot tone was chosen.

Many components required for signal splitting, division, filtering and distribution were evaluated both before and within this project, and two prototype boards were designed, manufactured and tested. This effort led to the final design for the frequency generation and distribution subsystem (FDS).

3.3.1 FRACTIONAL-N SYNTHESIZER VS. DIGITAL DIVIDERS

At the University of Florida a fractional-N synthesizer (custom-made with due regard to the strict timing requirements of LISA) was tested. The Albert Einstein Institute in Hannover later on evaluated the timing fidelity of a highly accurate programmable integer divider. Both devices are shown in Figure 3.4.

While the divider covered all integer divide ratios between 8 and 511 for maximum input frequencies of 14 GHz at 0 . . . 10 dBm input power, the synthesizer was designed to upconvert a 50 MHz sine or CMOS input signal to 2000 ± 20 MHz at adjustable in 100 kHz steps. 50 MHz was considered to be the pilot tone frequency while 2 GHz was considered to be an adjustable laser carrier phase modulation frequency at that time.

As shown in Figure 3.5, the differential noise between two synthesizers is significantly above the required timing level, while two dividers show much better performance. Considering that the divider measurements were early results and no extraordinary measures for temperature stabilization were implemented, all future design effort for the FDS followed a phase noise downconversion scheme with digital dividers.

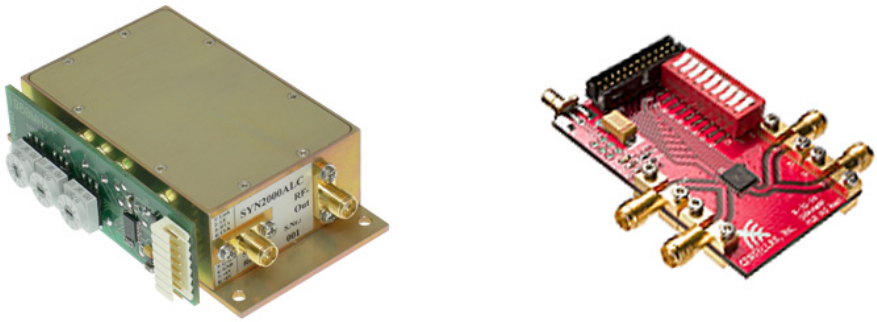


Figure 3.4: Fractional-N synthesizer (left) with BCD switches for output frequency adjustment and programmable integer divider (right) on evaluation board.

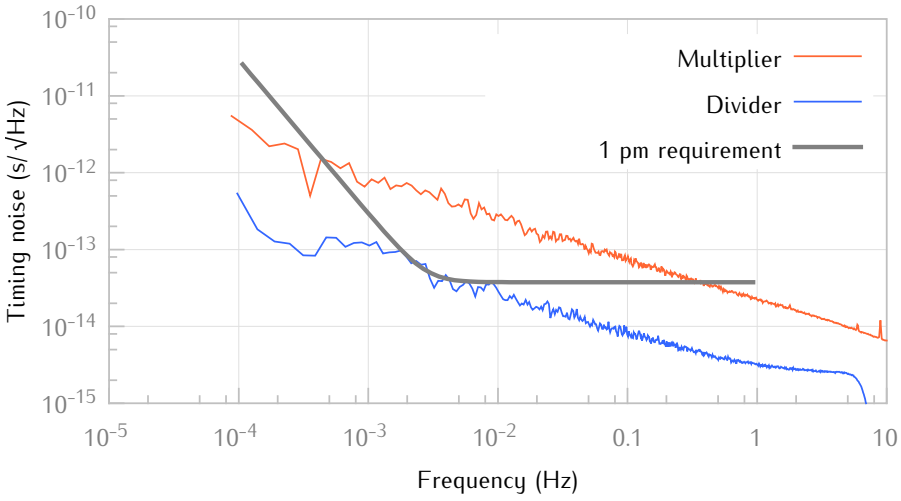


Figure 3.5: Timing fidelity comparison of the fractional-N synthesizer (50 MHz input multiplied by 40) and the programmable integer divider (2016 MHz input divided by 42). Phase measurements converted to timing noise and divided by $\sqrt{2}$ to represent the noise of a single device.

3.3.2 FDS COMPONENT EVALUATION PROTOTYPING BOARD

As most digital dividers, the tested programmable integer divider produces a square wave output which is highly asymmetrical for almost all division ratios. Hence a final divide-by-2 stage is necessary to generate a signal with 50 % duty cycle. While the sampling clock is expected to be a differential square wave signal, the pilot tone has to be a low-distortion sine wave. Thus an additional filter in combination with amplifiers and power splitters for signal distribution is necessary in the implementation of a division scheme for the final FDS.

Early on within the scope of this project, Axcon ApS designed two identical component evaluation boards. Both boards featured prescalers, gain amplifiers, custom-designed 5th order shaping filters and power splitters. Each component could be tested for **phase noise** individually.

While the single sideband (SSB) **phase noise** is given for many off the shelf components at various frequencies, the frequency range of interest for LISA (0.1 mHz ... 1 Hz) is never specified by manufacturers.

The input for the measurements was provided by an evaluation board and split for both boards. This procedure produces realistic signals while the noise of the divider itself is common mode and thus suppressed in the differential phase noise zero measurement. Results are shown in Figure 3.7. The custom shaping filter connected to a chain of power splitters could provide the required timing accuracy, but neither the gain amplifier nor the prescaler met the requirements.

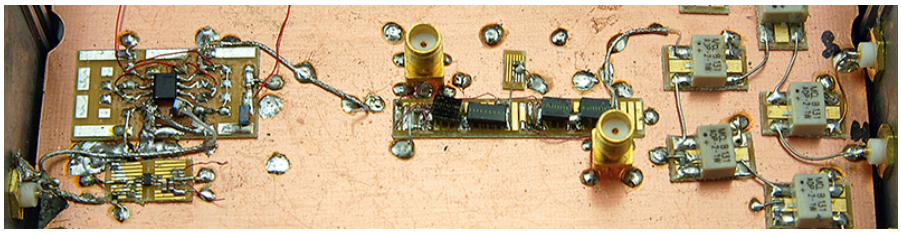


Figure 3.6: One component chain (prescaler, gain amplifier, shaping filter, power splitters) of the FDS evaluation prototyping board.

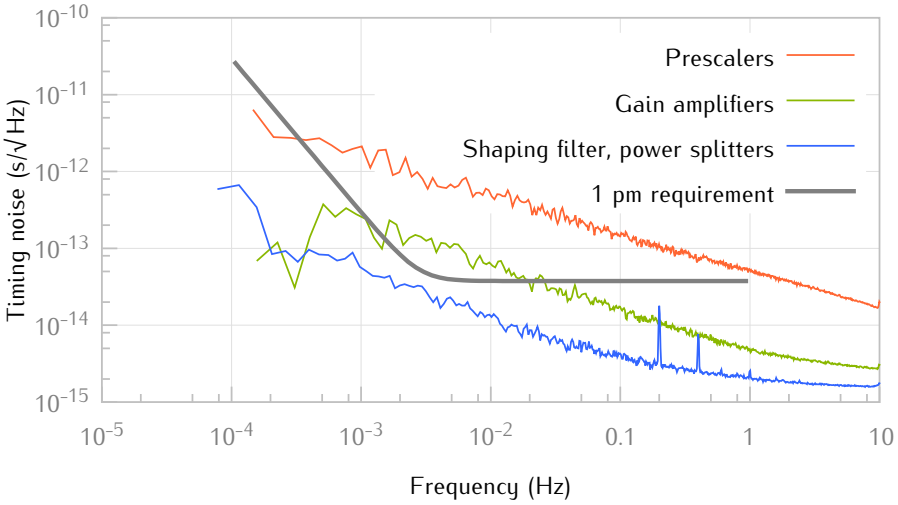


Figure 3.7: Timing fidelity comparison of prescalers, gain amplifiers, custom-designed shaping filters and power splitters. Phase measurements at 76 MHz output frequency converted to timing noise and divided by $\sqrt{2}$ to represent the noise of a single device.

3.3.3 FURTHER DIVIDER EVALUATION

After the initial evaluation with help of the prototyping board, the AEI in Hannover tested different alternative dividers and prescalers. Some replacement devices were tested with 150 MHz input frequency provided by a split signal generated by an evaluation board.

Also a different division approach was investigated. The intention was to replace the divider and prescaler all together with multiple space qualified and radiation hard prescalers. Here the input signal during testing was provided by a 2.4 GHz frequency generator.

While almost all components violate the timing requirements and the space qualified prescalers offer no alternative, one ÷2 divider stood out. As shown in Figure 3.9, alternative divider B performed an order of magnitude better than any other device under test. Further investigation provided evidence that the overall performance was only marginally worse when combined with a ÷16 divider for a full phase noise downconversion (2400 MHz divided by 32) and hence was considered as replacement.

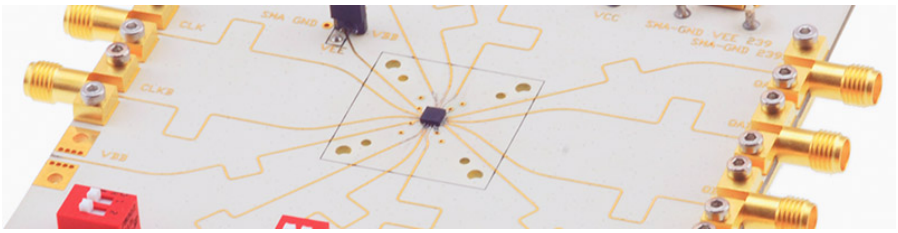


Figure 3.8: One of many dividers evaluated, on an evaluation board.

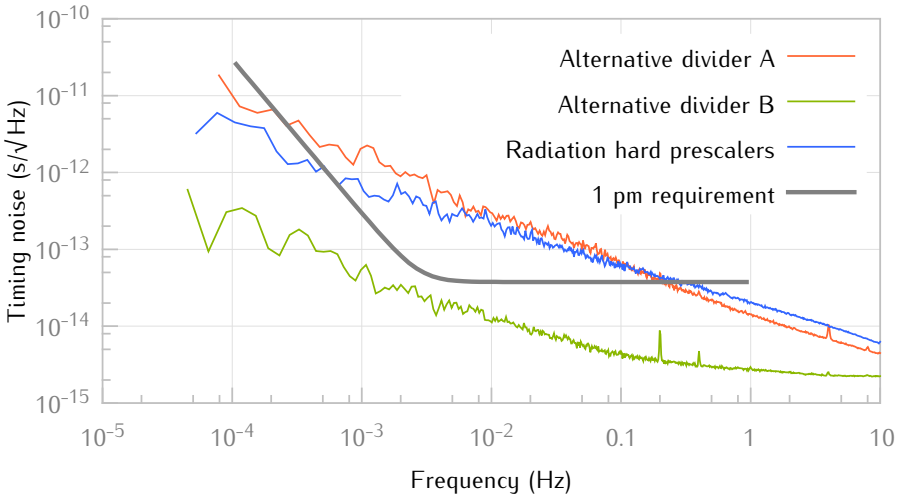


Figure 3.9: Timing fidelity comparison of some dividers (150 MHz input divided by 2) and prescalers (2400 MHz input divided by 8). Phase measurements converted to timing noise and divided by $\sqrt{2}$ to represent the noise of a single device.

3.3.4 PROTOTYPE PILOT TONE MODULE

Within this project and based on previous experiments performed at the AEI in Hannover—that also included GHz power splitters, alternative amplifiers and GHz frequency mixers—a prototype pilot tone module was developed. It was designed and manufactured by Axcon Aps for full integration and evaluation within the LISA Metrology System. The module features all functionality required for the FDS and has an on-board stabilized power supply. Critical components are implemented twice (two independent chains) to allow measurements of their differential phase noise, and multiple test points allow for noise measurements of individual components as shown in the magnified section in Figure 3.10.

The evaluation of the stand alone module showed that the shaping filter and power splitters perform exceptionally well. Their performance is limited by the overall measurement setup sensitivity as visible in Figure 3.11. The divider chain on the other hand as implemented on this module generates an intolerable excess timing noise that demanded a revised version of the pilot tone module.

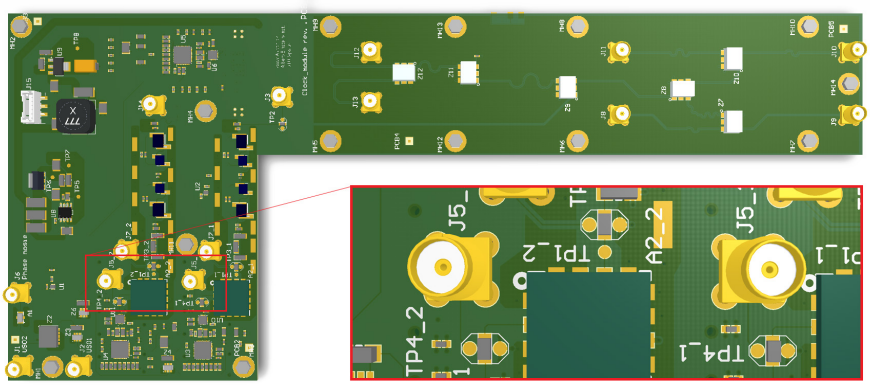


Figure 3.10: Prototype pilot tone generation and distribution module. The magnified section (lower right) shows test points TP1_2, TP4_1, and TP4_2 which were designed to measure the performance of single components individually.

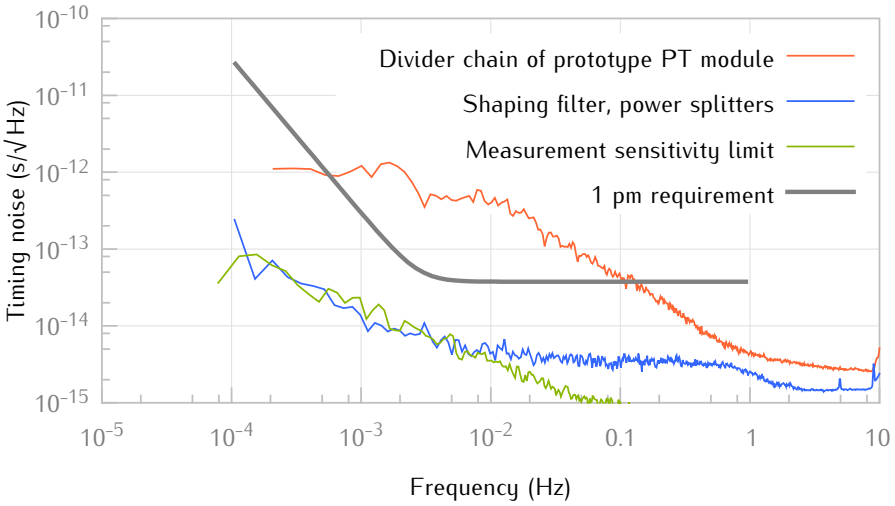


Figure 3.11: Timing fidelity comparison for selected sections of the prototype pilot tone module. While the divider chain (2400 MHz input divided by 32) violates the requirements, the shaping filter and power splitters perform exceptionally well. Phase measurements converted to timing noise and divided by $\sqrt{2}$ to represent the noise of a single device.

3.3.5 TOWARDS A SECOND GENERATION PILOT TONE MODULE

The reason for the excess noise generated by the divider chain implemented on the prototype pilot tone module must be related to the differences between this module and the corresponding divider evaluation boards. For example, the power supply for the ÷16 divider was reversed compared to the evaluation board in order to reduce the number of signal levels shifts in the system from negative to positive logic. Also a different PCB material was used there, which is very hard to come by in Europe. Furthermore the dividers on the prototype module are placed in close proximity to each other and become substantially hotter compared to the evaluation boards.

The entrapment of heat was made visible by a thermographic camera. Figure 3.12 (right) shows high temperatures in the area of the on-board power supply and the dividers. Temperatures peak at over 75 °C. Also a strong temperature gradient is visible across the PCB board, falling off diagonally along the shaping filters.

One more reason for the observed excess noise might be electromagnetic interference between the dividers. Effective shielding was hard to implement on the prototype module so that the PCB layout was revised. As part of this revision process, the ÷2 divider was evaluated again for input signal frequencies up to 2.4 GHz. The AEI in Hannover could show that the projected timing jitter for five dividers at various frequencies – featuring a total division ratio of 32 – surpasses the performance of the ÷16 divider. Hence the ÷16 divider was replaced by a chain of ÷2 dividers.

In the end, the second generation pilot tone module as described in detail in Section 4.1.3 on page 56 was improved substantially. Above all, components that were not essential and might cause excess noise or act as additional heat source were identified and omitted in the final design. ∎

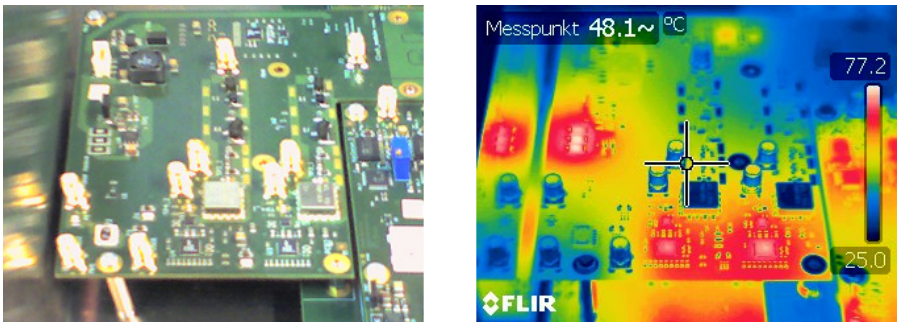


Figure 3.12: Prototype pilot tone module in visible (left) and infrared (right) spectrum. One can clearly see a strong temperature gradient across the shaping filters that originates at the power supply (left hand side) and the dividers (bottom).

4 SYSTEM ARCHITECTURE

The extensive studies performed prior to the design and implementation of the LISA Phase Measurement System (PMS) elegant breadboard model (EBB) clarified the overall technical requirements to the circuitry and calculation algorithms. However, the actual architecture and system split into hardware, software and FPGA computation did not have an obvious link to the technical requirements. Consequently, the system architecture was considered early.

Axcon ApS was driving the EBB architecture work and design in close dialog with the AEI in Hannover. The teams worked closely together while taking the advantage of the comprehensive scientific knowledge of the AEI team with the deep industry experience of Axcon ApS. The resulting architecture comprises several computation units (FPGAs and CPU), advanced high speed interconnect, fast data acquisition, fast control outputs, synchronization signaling, and sophisticated filtering and distribution networks.

The apparent performance requirements called for an advanced platform providing ample processing resources while offering a high flexibility for the later scientific tests done at AEI. A modular configuration was chosen to support future upgrades, thermal experiments, and to facilitate ease of access to measurements. Significant engineering experience and effort was put into securing a solid system performance, including early prototyping of pilot tone circuitry and FPGA connection topology.

The four different modules for the EBB was designed, build, and functionally tested by Axcon ApS. Subsequently the EBB prototype as well as FPGA framework and embedded software was handed to AEI for integration of signal processing algorithms and the extensive performance testing commenced.

4.1 HARDWARE

The driving aspects of the EBB design were the required functionalities and the performance goals. But also considerations for cost, power consumption, flexibility and special aspects of known critical elements (like the analogue front end and thermal influence from surrounding components) were taken into account. Figure 4.2 shows a photograph of the EBB hardware. While for critical components space qualifiable parts were investigated and partly implemented, standard

commercial parts were used for the bulk of the system. A system sampling clock of 80 MHz was chosen, which is higher than in previous prototypes and allowed to simplify some aspects of the design, like the anti-aliasing filters. FPGAs were selected from the Spartan 6 series from Xilinx, since they provided sufficient logical resources, including large margins for future developments and experiments, together with reasonable power consumption and price. Microsemi (Actel) devices were considered but the available devices did not offer adequate fabric complexity and density for the EBB. It is assumed that Microsemi over time will provide devices of performance comparable to the Spartan 6 devices. At the Microsemi Spaceforum in autumn 2013 Microsemi revealed their roadmap of the RT4G showing that relevant devices are scheduled for release in 2015. Additionally Xilinx Virtex 5 devices are available in space qualified variants. DTU Space is currently testing a Virtex 5 device for another mission. The hardware was split into four individual modules, each containing different parts of the functionality. One full EBB consists of one main module, one pilot tone module, one DAC module and five ADC modules. In the following, each module is presented together with its key components and functions. Afterwards two critical aspects of the infrastructure are described in more detail, the signal and data flow between the components and the synchronization subsystem that is required to ensure a common system timing.

4.1.1 ADC MODULE

The analogue signals from the interferometers are digitized and processed on the ADC module. The main components on this module are an analogue front-end circuit, which conditions the input signals and adds the pilot tone, an ADC that performs the digitization, and an FPGA, that houses the readout algorithms and communicates with the other subsystems. The layout of the ADC module is shown in Fig-

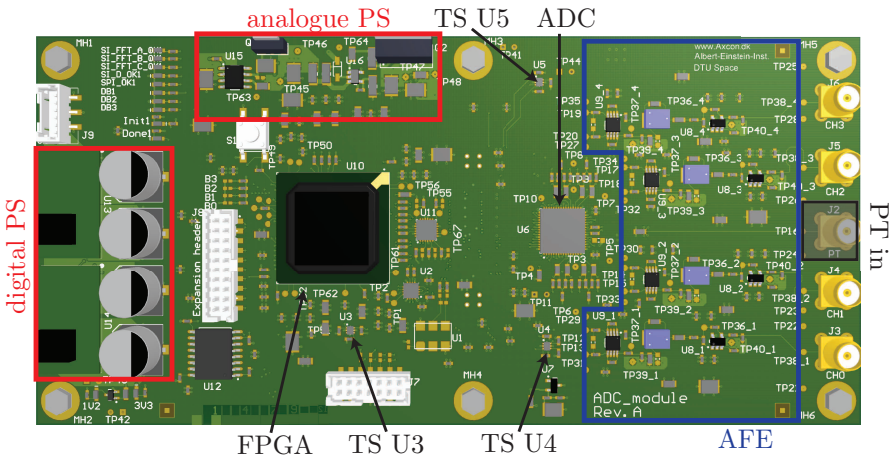


Figure 4.1: Layout of the ADC module. It contains four signal inputs, one pilot tone input (PT in), four analogue front-end circuits, one ADC, one FPGA, three temperature sensors (TS), an analogue and a digital power supply (PS) as well as several other peripheral components and connectors. The connector to the main module is located on the bottom.

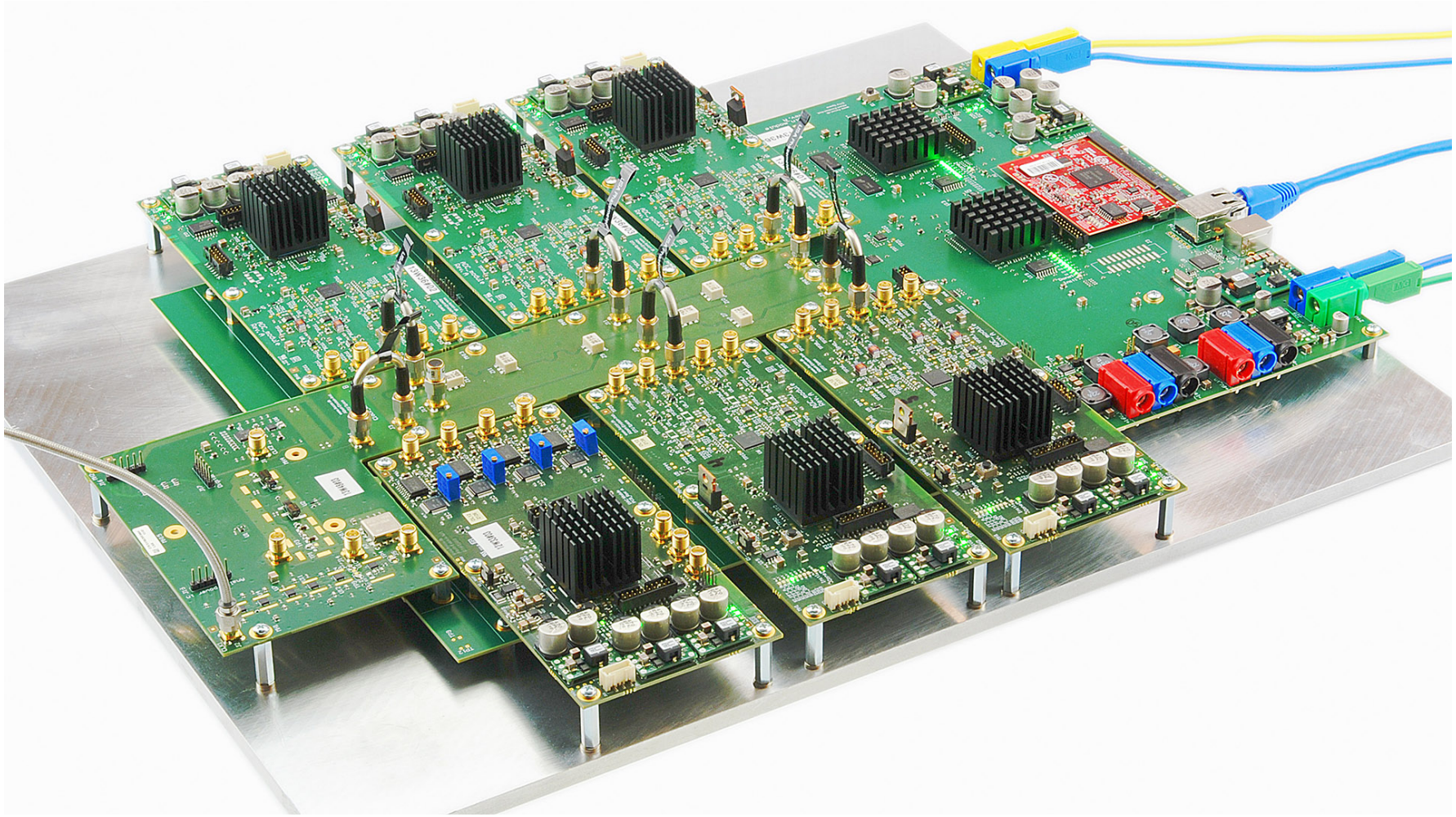


Figure 4.2: Photograph of the assembled EBB. Shown is a main module with one second generation clock, one DAC module and five ADC modules.

ure 4.1. The module can either be connected to the main board or it can be used in stand-alone operation. The latter variant allows to simplify testing, since a single ADC module can be used as an independent phasemeter prototype and does not contain the various additional features of the full system which could potentially cause unwanted disturbances.

An ADC module is plugged via a multi pin connector directly into one of the six slots of a main module. This connector provides the system clock and the supply voltages to the module. It also connects several interfaces, most importantly the main, high bandwidth link between the local FPGA and the FPGAs on the main module. One ADC module was designed to measure four input channels. Therefore it contains four equal analogue front-ends and an ADC with four input channels. The phase measurement performance of the ADC was tested beforehand. The main function of the FPGA on this card is to perform the phase and ranging readout algorithms, to decimate this data to a suitable rate, and to transmit it to the main module.

In stand-alone operation the FPGA can directly be controlled and read out via a USB or generic serial interface, added to the module by using free FPGA pins connected to an expansion header. Another connector allows to provide power and an additional crystal oscillator has to be soldered onto the module to provide a system clock.

ANALOGUE FRONT END The signals are fed into the ADC module via four SMA connectors. A fifth connector is used to feed in the pilot tone signal directly from the pilot tone module. The AFE circuit for one channel includes three main components: a gain and buffer stage for signal conditioning, an anti-aliasing filter, and a differential amplifier, that is used to simultaneously add the pilot tone and to generate a differential signal required for driving the ADC. This architecture was based on the pre-investigations of phasemeter prototypes developed at the AEI in Hannover [39].

The gain stage was implemented using a current-feedback op-amp with a high gain-bandwidth product. The aim of this was to generate a flat amplitude and phase response for various signal gains, in order to reduce temperature induced noise. No final requirements on the gain were available and, since they depend highly on the signal power and the photo receiver (PR) gain, therefore the implementation allow for flexibility by simply changing the feedback resistors and thus the amplification.

The anti-aliasing filter (AAF) is a second order low pass and was included for testing purposes. A detailed study of the required filter suppression and phase linearity was not conducted, since they depend strongly on the PR transfer function and other not yet specified parameters. A full measurement chain design might move the AAF,

as well as all required gain stages, fully into the PR, depending on the available thermal stabilities and power budgets.

The differential amplifier used to drive the ADC and to add the pilot tone has a large bandwidth (> 300 MHz) to reduce thermally induced phase noise. The pilot tone was split without using a resistive splitter and fed into the second input port of the amplifier. To prevent reflections from the impedance mismatch of the split and from the receivers, the signal is terminated at the split. This is considered feasible since the dimensions on the AFE board are small compared to the signal wavelengths.

Since all of these analogue components were known to be critical for the measurement performance, a possibility for exchanging not only the front-end components, but also the layout was included into the design. Several test-points were added, that allow to solder a hook-up board onto the original AFE. Such a board directly connects to the signal inputs and the ADC inputs, and can therefore be used to replace the original AFE circuit, allowing to still use most of the ADC module.

4.1.2 DAC MODULE

The EBB generates up to three digital and four analogue signals with the DAC module. Its main components are an FPGA, four DACs, each with an analogue offset correction and amplifier circuit, and three buffered digital outputs. The FPGA infrastructure of this module is almost an exact copy of the one of the ADC module. This allowed to use some of the same programming code and it made it possible to easily exchange the two module types. Therefore a main board can potentially be used with none, one or even more than one DAC module. The layout is shown in Figure 4.3. The DAC module can also be used in stand-alone operation.

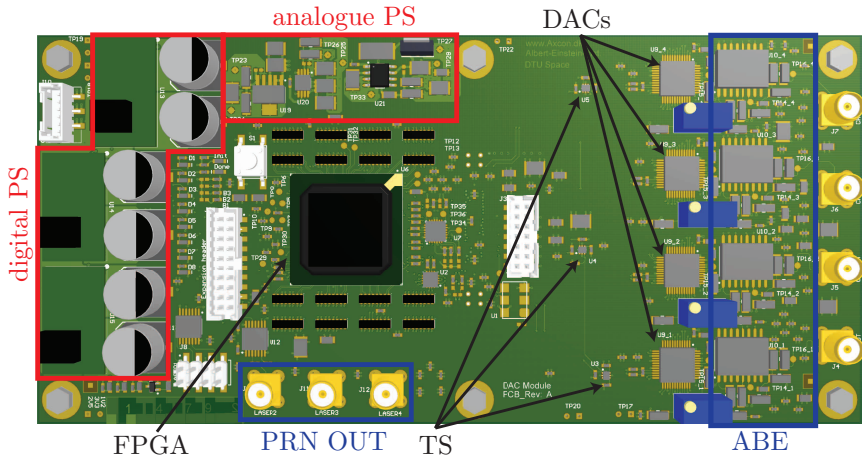


Figure 4.3: Layout of the DAC module. It contains three single-bit digital outputs, four DACs, four analogue back-end (ABE) circuits, one FPGA, three temperature sensors (TS), an analogue and a digital power supply (PS), as well as several other peripheral components and connectors. The connector to the main module is located on the bottom.

The FPGA on this module has two main functions. The first function is to host offset-frequency phase locks [40, 41] or similar algorithms. These algorithms use the frequency information of the beat notes from the ADC modules, communicated via the main board, to generate actuator signals. These signals are then converted into analogue ones by the DACs and their offset and amplitude is further conditioned by analogue back-end circuits, before they are made available at separate SMA connectors. Each output was designed to have a range of $\pm 10\,\mathrm{V}$, which is convenient for laboratory experiments. While the DACs are sampling with 80 MHz, the analogue outputs were low pass filtered with a corner frequency of approximately 10 MHz. This is a more than sufficient bandwidth for laser control and additionally allows to use the DACs for other purposes. The outputs also include a resonant filter at 80 MHz to reduce any residuals of the clock signal in the outputs. The actuator signals can also be made available via a serial interface, if a laser with digital interfaces has to be controlled.

The second function of the FPGA is to generate PRN signals for the phase modulation required to implement ranging and data communication. For three channels, data received from the main board is therefore encoded with individual PRN signals and fed via simple digital buffers to SMA connectors.

4.1.3 PILOT TONE MODULE

The pilot tone module generates the system clock at 80 MHz and pilot tone at 75 MHz out of a 2.4 GHz reference oscillator by frequency division ($\div 30$ and $\div 32$) and distributes the pilot tone. It is plugged into a dedicated connector on the main module which provides the supply voltages and receives the clock signal from the pilot tone module.

While the clock is directly fed to the main module, the pilot tone is further filtered and amplified. Since the initial pilot tone is a rectangular signal (from the digital dividers) a temperature compensated passive filter is used to reduce its content of higher harmonics.

A pilot tone distribution section, where the pilot tone is split via power splitters and made available at six SMA connectors with equal delays ensures a common overall phase. This type of distribution was chosen to ensure a high phase stability and cleanliness of the pilot tone, both of which might have been spoiled by using a distribution via the main board. The distribution part of the pilot tone module is in the middle of the ADC modules (see Figure 4.2), this shortens the signal path and allows to decrease the influence of strong heat dissipation by the FPGAs and power supplies, which are situated on the outside of the EBB.

Figure 4.4 shows the layout of the two pilot tone modules designed for the EBB. In contrast to the prototype pilot tone module as described in Section 3.3.4 on page page 48, this final module has no on-board voltage regulators. Instead it forwards the power supply from the main module to a connector. An external voltage transformation and stabilization board then feeds the required voltages back to the pilot tone module. Each group of components has its dedicated power pin so that single devices can be switched off individually.

This redesign was part of the effort to remove everything from the pilot tone module that was not essential and might cause excess noise or act as additional heat source. In this regard the mixer to generate a correction signal for a second GHz signal together with all GHz power splitters were moved to external shielded components.

Another major change is the replacement of a ÷16 pilot tone divider by a chain of 5 + 1 ÷2 dividers. The additional stage is bypassed and powered off but can be used to produce an alternative 37.5 MHz pilot tone which is not aliased by the 80 MHz sampling frequency.

The shaping filters and the divider chain producing the system clock are identical to the prototype module. Only one pilot tone generation chain is present on the module, differential measurements of the timing fidelity are performed between two equal modules. All components have solder points for electric shielding, and thermal pads are connected through the backside of the board. The primary trace layer is made of a special material which performs very similar to the material used in the evaluation board of the ÷2 divider.

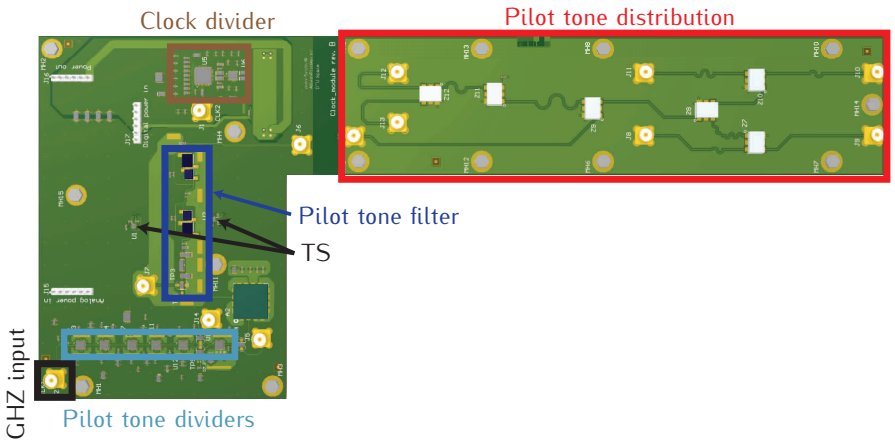


Figure 4.4: Layout of the second generation pilot tone module. The elongated part of the module contains the pilot tone distribution with delay matched signal lines and six power splitters. The other part of the module contains the frequency generation. It consists of the clock dividers and of the pilot tone dividers and filter.

4.1.4 MAIN MODULE

The main module as shown in Figure 4.5 hosts all other sub modules, provides power, distributes the system clock, it hosts an FPGA dedicated to performing fast Fourier transformations (FFT FPGA), it hosts the CPU module that controls the system, and it hosts another FPGA (bridge FPGA) that establishes the interfaces between the FPGAs and the CPU. The main module can also use a crystal oscillator as source for the system clock. This allows to use the system without a pilot tone module or if, for example, no 2.4 GHz source is available. A 12 V supply voltage is passed to all sub modules and used to generate all voltages for digital circuits. A 24 V supply voltage is used to generate the local supply voltages of ±6 V and ±16 V for analogue components, which are also supplied to all sub modules.

BRIDGE FPGA The bridge FPGA works as the central switch for most communications between the FPGAs and the CPU. It multiplexes the various data streams that are sent back and forth in the system and frames them into the required formats. The data streams are discussed in Section 4.2.2. It also handles the FPGA synchronization, which is described in more detail in Section 4.2.3. For simplification this FPGA was chosen to have the same type as the FPGAs on the ADC and DAC modules.

CENTRAL PROCESSING UNIT The EBB required a central processing unit with floating point capabilities and high-level programming options. The LPC3250 OEM Board from Embedded Artists was chosen for this purpose. It houses an NXP ARM926EJ-S LPC3250 processor and includes various peripherals that allow to simply mount

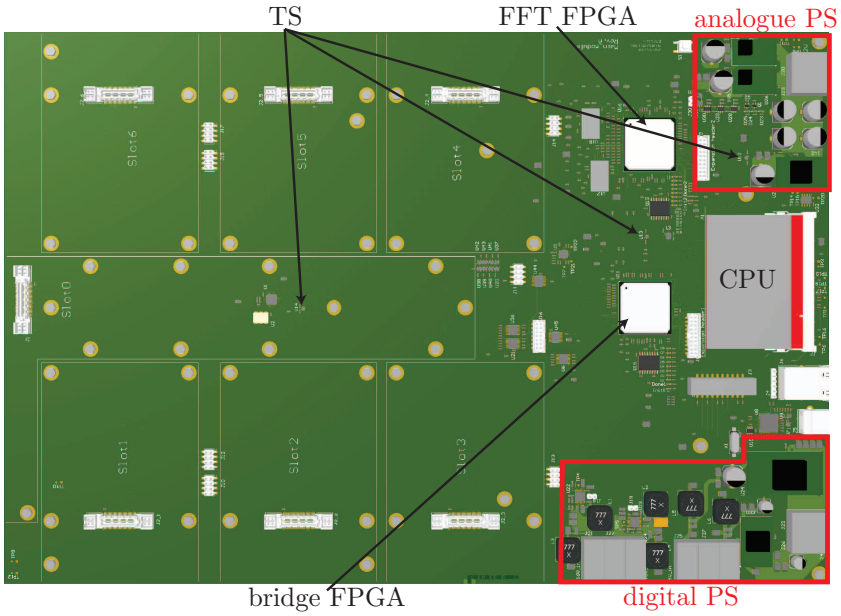


Figure 4.5: Layout of the EBB main module. The left side contains seven connector slots for sub modules. Slot 0 is reserved for the pilot tone module, slots 1 to 6 can be equipped with ADC and DAC modules. The right side of the EBB contains the FFT FPGA, the bridge FPGA, the CPU, the power supplies and various connectors and additional peripherals.

it onto the main board with an expansion connector, which provides power and the required connections. The CPU functions can be divided into two main tasks. The first one is to handle the measurement data. The incoming data packages have to be formatted, filtered and then packed and transmitted via Ethernet to a connected PC. Later on the data might also be sent to a DFACS system in the spacecraft computer, via a not yet defined interface. The filtering of the incoming data is the most demanding task in terms of required processing power. The chosen CPU therefore includes a dedicated vector floating point co-processor, which gives the system a computational overhead that can be utilised during later developments.

The second task of the CPU is to control the system and to perform housekeeping functions. The availability of a general-purpose programming environment allows to implement complex algorithms that can be used to operate the EBB autonomously. This is necessary for using the EBB in experiments that simulate flight-like situations, where the communication to the satellites would be non-permanent and very limited in bandwidth. For example, the autonomous acquisition of the ADPLLs had to be implemented as part of the EBB development.

An important additional feature of the CPU is the readout of temperature sensors spread across all modules. This data is also packed and sent to the PC. The CPU runs the RTEMS (Real-Time Executive for Multiprocessor Systems) operating system. This choice of high-performance CPU was agreed at the beginning of the activity in order to facilitate algorithm development and debugging with ample performance margin. A suitable flight CPU can then be chosen at the time of FM development based on the actual CPU load measured with these prototypes.

FAST FOURIER TRANSFORM (FFT) FPGA To allow for maximum acquisition performance a dedicated FPGA was implemented to perform fast Fourier transformations. This FPGA is connected directly with high bandwidth interfaces to a subset of the ADC modules. The full ADC data sampled at 80 MHz is fed through these interfaces and made available on the FFT FPGA. There it is fed into FFT blocks, that allow to perform full duty-cycle FFTs on four input data streams, for example, on four segments of a QPD. To achieve this amount of computational power the FFT FPGA is a larger Spartan 6 type, with roughly twice the logic resources than the other FPGAs in the system. The FPGA also hosts peak detection algorithms which operate on the FFT outputs and produce the data sent to the CPU.

Additionally the FFT FPGA connects to random access memory (RAM) with a capacity of 256 MB. This allows to store a burst of data at the full sampling rate, which can then be read out via the CPU. The ADC modules providing this data can also be modified to transmit, for example, signals from inside the ADPLL. These types of burst data can be used to perform debugging and signal analysis over a wide range of frequencies, something which is not possible otherwise, due to bandwidth limitations.

4.1.5 THERMAL CONSIDERATIONS

The thermal design and implementation of the EBB have been given special attention by Axcon ApS in the overall design layout of the system and subsystem. The EBB module setup and placement of the different parts on the module have been done with this requirement in mind. This is to keep the PT distribution and the analogue measurement components as stable as possible and not to increase the noise in the chain. The design is implemented with a target of being able to only use passive convection of the components packages and optional heat sinks. Using a forced airflow from fans over the board could influence on the thermal stability if the flow is not uniform over time intervals corresponding to the frequency of interest in the measurement. This can cause unintended modulations of the signal before it is sampled in the ADC and adds to the noise of the signal. Forced airflow was consequently not part of the prerequisite for the EBB construction. However, both active and passive temperature control was added to improve the thermal noise performance even further during the testing.

The components with the highest power dissipation are placed close to the edges of the modules maximizing the distance to the analogue front end and PT distribution circuits. The overall layout is designed to support a thermal insulation block that is covering all the analogue front-end of the ADC modules, PT distribution circuits together with the shaping filter for the PT. The use of such an insulation block is only possible when the power dissipation is limited and without risk of thermal run-away.

Moreover it is necessary to make the PT distribution chain as identical as possible for all channels. This is done through length matching and placing the power-splitters as symmetrically as possible. Another technique applied here is to use only the top layer for routing and to avoid vias. As shown in Figure 4.6, the trace length of the critical traces is also to a large extend matched in x and y direction of the PCB. This accounts for the possibility that the PCB is not necessarily expanding homogeneous in the x,y and z direction.

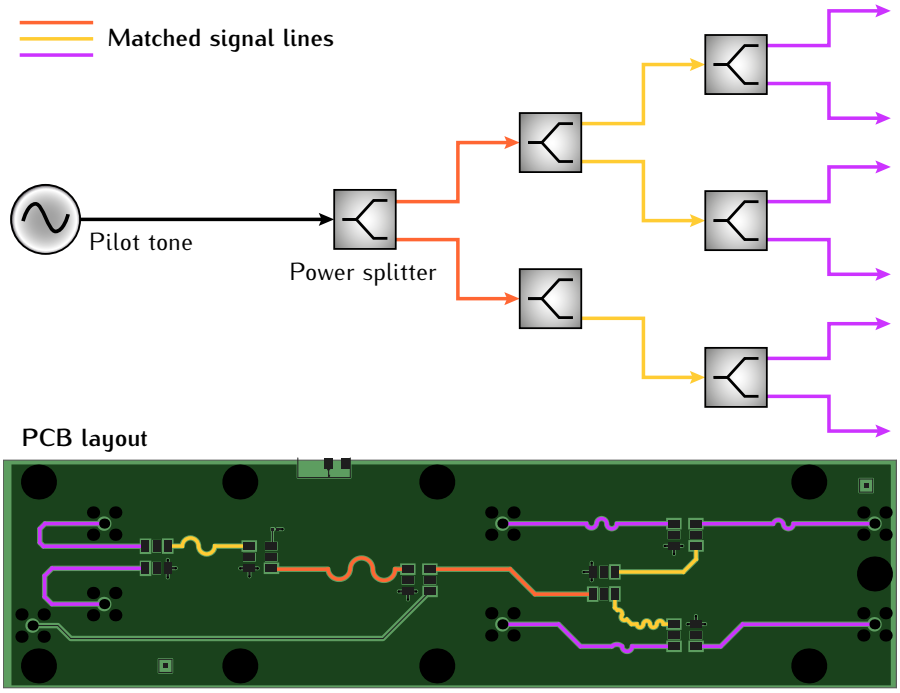


Figure 4.6: Pilot tone distribution. Conceptual drawing (top) and actual PCB trace layer (bottom). Traces of individual colors are matched in length to each other.

4.2 SYSTEM INFRASTRUCTURE

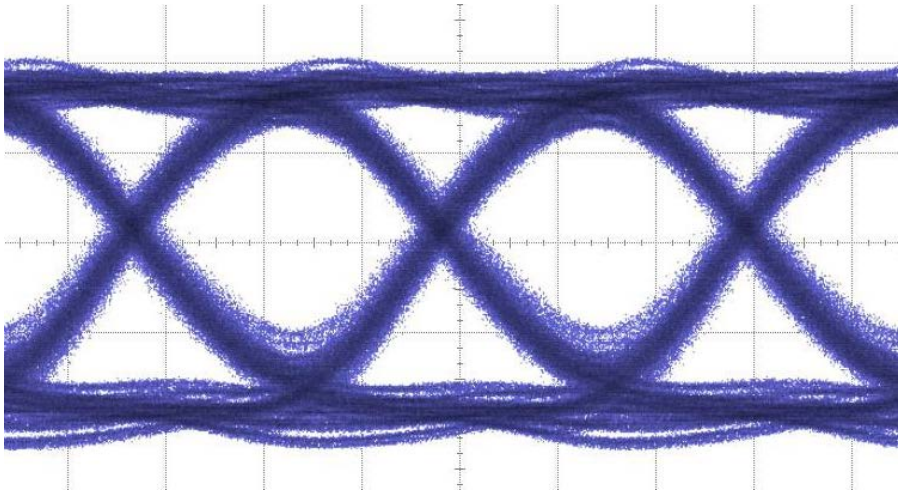
The EBB is composed from the modules described in Section 4.1.1 to Section 4.1.4. However, one significant feature of the modules besides the conversion and processing capabilities is their interconnection. All modules except the pilot tone module have high bandwidth digital interfaces. The modular hardware infrastructure does not only provide flexibility, it also puts challenging requirements on these inter-module connections. The two most relevant aspects are a coherent timing system, which is needed to allow for the TDI algorithms to operate correctly, and the data communication bandwidth and delays, which are essential for the metrology system algorithms to work as desired. How these critical aspects are covered by a dedicated infrastructure is described here.

4.2.1 GIGABIT INTERFACES

As a consequence of the distribution of the FPGA logic across several devices (up to 8) it becomes necessary to have a high performance interconnect. The bandwidth figures are provided in Section 4.2.2, but in addition to these direct calculations the experience is that systems having several FPGAs will benefit from having ample interconnect bandwidth to optimally utilize the FPGAs and to maximize the flexibility. The high speed interfaces will support late partitioning decisions or changes in location of the FPGA processing. Future experiments using the EBB will likewise have a large degree of freedom to

support added or modified FPGA processing. On the EBB the FPGAs are connected using several gigabit serial links providing high bandwidth. In addition the communication protocol is kept simple to limit the latency. The links are connected by board to board connectors and via the main module.

Each of the high speed links is designed to support at least 2.4 Gb/s communication speed and was tested at 3.2 Gb/s as shown in the example below.



Eye diagram at 3.2 Gb/s. Example of the signal quality of the gigabit connections on the EBB as measured during functional testing by Axcon ApS. Example shown is the link from the bridge FPGA to slot 6, 100 ps/div, 50 mV/div.

The topology is selected to ensure that the science data can flow through the system without bottlenecks and to a large extent it allows the FPGAs work as one unit. Combining all the FPGA functionality into one single device would clearly simplify partitioning, but prevents the modular design approach. The FPGA topology has proven to have adequate headroom for the EBB testing and improvements throughout this project.

4.2.2 DATA FLOW

The modular design approach of the EBB required to implement interfaces that have sufficient bandwidth for the different functionalities. The various interfaces can be divided into two types: streamed data, which is sent at regular intervals and contains well defined data frames, and command data, which consists of the register read and write packets that are controlled by the CPU. An overview of these interfaces is shown in Figure 4.7. The register interface uses the bridge FPGA as a switch and connects from there to all other FPGAs.

There are three types of streamed data interfaces implemented into the EBB. The first one is used for the science data, which contains all the various DSP readout signals and additional meta data, like the internal time stamp of each FPGA. This data is sent to the bridge,

where it is re-framed and then sent as one large package to the CPU. The rate of the science data is rather slow ($80\,\mathrm{MHz}/2^{17} \approx 610\,\mathrm{Hz}$), but it is sufficient for providing signals to a DFACS system and it has to be even further decimated for the data storage. More details about the science data and its decimation are described in Section 5.4.

The second streamed type of data is for the laser lock implementation. For these locks the EBB implements the core functions of a fast control loop, with a requirement of an absolute delay of less then $\approx 3\,\mu\mathrm{s}$. To implement these locks the frequency/phase information of the beat notes, measured in the ADC FPGAs, has to be sent to the DAC FPGAs without causing excess delays. A rate of 10 MHz was chosen for this interface, which allowed to keep the delays caused by the interface low enough. Only two of the laser lock signals sent from the five ADC cards can be sent through to the DAC FPGA, therefore a multiplexer in the bridge allows to choose which ones are required. The physical interface between the bridge and the other FPGAs is based on a single serial link with a bandwidth of several Gbits/s.

The last type of streamed data interface is the delivery of all the ADC sampling data from three ADC modules to the FFT FPGA. The large required bandwidth ($4\,\mathrm{ADCs} \times 14\,\mathrm{bit} \times 80\,\mathrm{MHz} \approx 4.5\,\mathrm{Gbit\,s^{-1}}$) was achieved by adding three physical serial interfaces to two of the ADC slots. A single additional link was implemented for a third ADC slot, with the reasoning, that a reduced amount of data is sufficient for acquiring lock of the local reference interferometers on the optical bench since these are rigid and have constant high contrast and

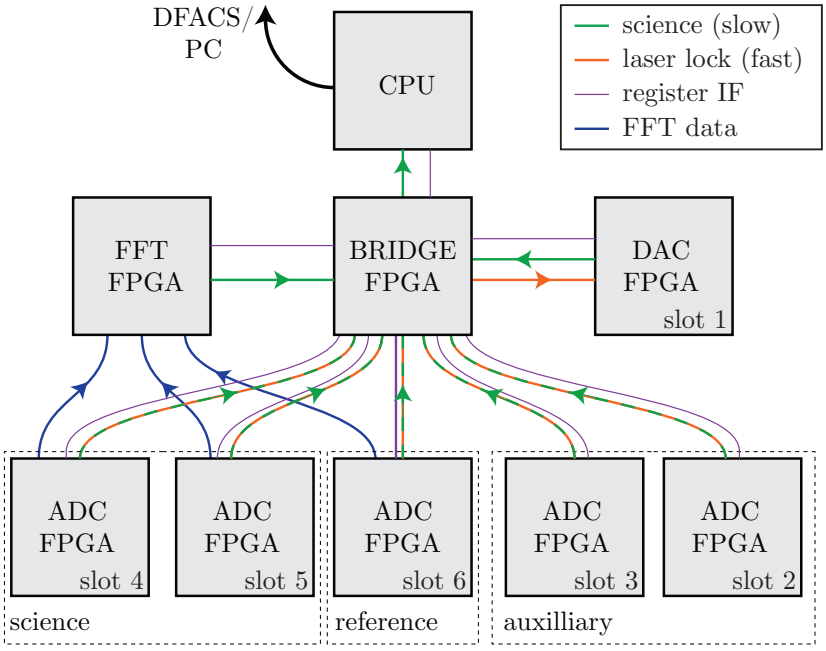


Figure 4.7: Sketch of the data flow between the FPGAs and the CPU on the EBB. The streamed data interfaces (science, laser lock, FFT data) are all unidirectional and they send predefined data frames at fixed intervals. The register interface is bi-directional and allows to send and read data. It is not synchronized, since it is controlled by the CPU. The data to be encoded with PRN codes on the DAC card for inter-satellite communication is communicated also via the register interface, since it only has a low bandwidth requirement.

SNR, thus requiring only a single photodiode channel instead of four channels from a quadrant photodiode.

4.2.3 SYNCHRONIZATION

A dedicated synchronization scheme was implemented to allow system-wide coherent timing. This is necessary to ensure that all sampling and decimation, as well as the PRN generation, start predictably at the same edge of the system clock. The scheme is based on a synchronization signal, the so called tick, that is generated by the bridge FPGA and fed to all FPGAs (also back to the bridge) via matched delay lines (see Figure 4.8). Each FPGA contains a state machine that controls a counter that is triggered by the received tick. After a successful synchronization each FPGA maintains an identical local copy of this counter that is used for all timing operations. This counter is, for example, used to generate the decimation clocks and the PRN codes. The state machine controlling the counter is armed (it waits for the tick), by a simple command from the CPU. The tick generation produces a tick at regular intervals, but it can be switched on and off via a CPU command. Therefore triggered state machines can also be used to time other algorithms or changes in the FPGAs, allowing to exert full control of timing in the system, if necessary. All data packages sent to the CPU contain this counter value from the time of transmission. The value can be compared to a software package counter in the CPU to detect missing packages. The CPU also contains an internal hardware counter (INT in Figure 4.8), driven by an independent clock, which is also read out for debugging purposes.

Once the synchronization works, only deterministic, constant time offsets remain which can be taken into account in the post-processing. One should note, that the full timing in the EBB has three components, the 80 MHz clock, which defines the timing intervals, the tick synchronization, that sets the absolute system time i.e the counters, and the pilot tone, which allows to correct the timing jitter of each ADC channel relative to the timing reference which, in this case, is the 2.4 GHz side band tone.

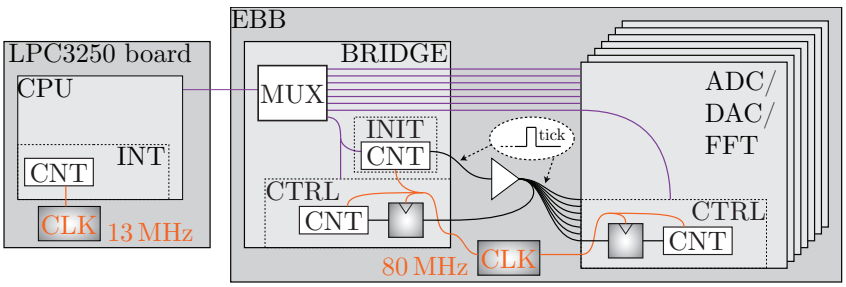


Figure 4.8: Shown is a sketch of the EBB synchronization scheme. A counter (CNT) in the bridge FPGA, with a dedicated state machine (INIT), is triggered by a CPU command to send ticks to each FPGA control block (CTRL).

4.3 PROGRAMMING

Six devices on the EBB required individual programming: the four types of FPGAs were all programmed using VHDL, the CPU and the PC interface programs were written in C. The hardware interfaces on all devices were implemented by Axcon ApS, together with additional abstraction layers, most of the infrastructure for the register interface and the operating system and drivers for the CPU. The digital signal processing, control, framing and data streaming was then implemented on top by AEI. In the following the system control is explained in more detail.

The EBB is initialized via a PC program. The program establishes a TCP/IP link via Ethernet to the CPU and provides it with various parameters, depending on the chosen mode of operation. The CPU then performs the FPGA counter synchronization and initializes the DSP blocks in the system by writing various parameter into the corresponding register, like the gains and initial frequencies for the ADPLLs. After this, the CPU activates the streamed data interface on the bridge and it begins the data readout loop. During this loop it waits for packages to arrive, decodes and filters them, and sends the resulting packages to the PC, where they are stored for display and analysis.

The system is controlled via a register based interface handled by the CPU. Each register in the EBB has a unique address and can be written via a simple CPU command. Registers can also be read out by the CPU if they are configured for that in the VHDL code (readable registers require significantly more resources and therefore they have to be instantiated specifically). For debugging purposes a notification for each register write and read is also sent to the PC. It contains the data and address of the register, as well as the CPU internal counter value for timing. This allows to reconstruct the detailed behavior of the CPU, including reaction times, which is especially important if the EBB works partly autonomously. ∎

5 ALGORITHMS

The core functionalities of the LISA metrology system are provided by digital signal processing algorithms implemented in the FPGAs and the CPU. These algorithms operate on the digitized optical interference signals and they extract the science information, as well as various additional data that is required for the real-time control of the LISA satellites and their subsystems.

This chapter gives an introduction to the most critical algorithms. Large parts of these algorithms are also documented in detail in the Ph.D. theses of J. Kullmann, J. J. E. Delgado and O. Gerberding [28, 39, 42].

5.1 SCIENCE READOUT

The readout algorithms implemented on the FPGA of each ADC module are described here. The presented specific scheme is designed for detecting the four beat notes generated on a QPD for the LISA inter-satellite link ("science interferometer"). This scheme was implemented during the development, since it is the most complex and demanding one. It can be modified and simplified for the readout of, for example, the auxiliary interferometers. The scheme is sketched in Figure 5.1.

SCIENCE TONE PLL The interferometric beat notes are read out in the so called main ADPLLs. Their internal design is based on the model presented in Section 5.2. Read out from these PLLs are the individual frequencies, I and Q values as well as the direct phase differences for DWS. In addition the sum of the four frequency values is computed and read out. This value is also decimated to a rate of 10 MHz and used for the laser locks.

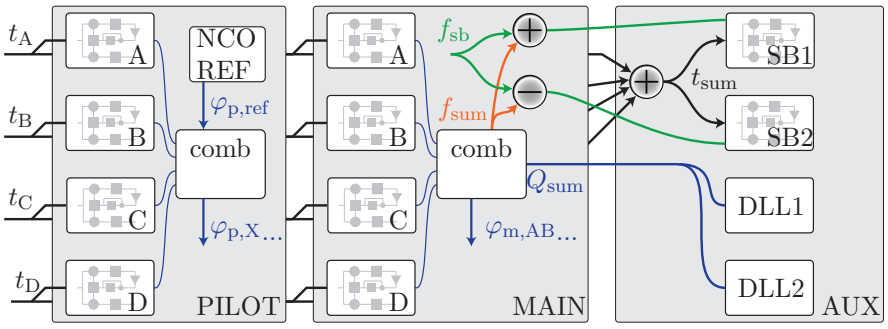


Figure 5.1: Shown is an overview of the DSP implemented in an ADC FPGA for the science readout.

SIDE BAND PLL The added ADC signals are fed into two separate ADPLLs for tracking the upper and lower clock noise transfer side bands. Since the side bands only use a small amount of the signal power their effective SNR is even lower than the one of the main beat notes. At the same time the side band PLLs have to track the same laser frequency noise dominated signal as the main beat notes, in addition to the clock noise and the Doppler shifts. The side bands are 2.4 GHz away from the carrier and their effective Doppler shifts are thus also slightly different. Since the largest part of the phase signal is already tracked by the main beat notes this information can be used to reduce the required bandwidth of the side band PLLs. Therefore the summed frequency of the four main PLLs is used, after adding/-subtracting the corresponding offset, as offset frequencies in the SB PLLs (see Figure 5.1). Thereby the frequency noise and Doppler shift information is transferred in a feed forward scheme and the SB PLLs only need to track the clock noise and the slight Doppler variations. Individual frequencies and the I and Q values are read out from these PLLs.

PILOT TONE PLL The pilot tone is measured for each channel by a dedicated ADPLL with a **design** very similar to the PLLs described before. The values that are read out from these ADPLLs are the frequency values, used to reconstruct the pilot tone phase changes, and the in-phase (I) value, to monitor the signal strength. A readout of the out-of-phase (Q) value is not necessary due to the high bandwidth compared to the absolute signal. The readout of the frequency has a large dynamic range which is not required for the pilot tone. A simplified readout mechanism was therefore included additionally. Since the phase of each PLL contains a ramp at the signal frequency, a constant ramp from an internal NCO (synchronized to the system counter) is subtracted from each of them. The so generated phase values are directly proportional to the sampling jitter in each channel, and they use less then half the amount of bits and therefore bandwidth as the frequency values.

The current implementation used almost the same **design** as developed for the interferometric beat notes. A more specific design might utilize a very low bandwidth, since the absolute pilot tone phase changes are very small. The frequency of such a dedicated pilot tone PLL might even be constrained to a very narrow range around the nominal frequency by additional logic.

DELAY-LOCKED LOOP The inter-satellite ranging function conceptually works by continuously sending time semaphores in both directions along the link. By recording the transmit and receive time in the local clock of the transmitting and receiving spacecraft, respectively, both the distance ("range") as well as the clock offset can be measured. In this implementation, instead of discrete pulse-like timestamps a pseudo-random noise code is continuously transmitted. It is generated from the transmit clock, with the starting time of the code coincident with a bit transition in a certain high-value bit. The receive function is performed in the phasemeter in two delay-locked loops (DLL), which are tracking the local and remote pseudo-random

noise (PRN) codes. They use the combined sum of the main PLL mixer outputs (Q_{sum}) as inputs. These DLLs also read out the raw data from the PRN stream. This implementation is based on earlier work at the AEI [28] and was further extended and ported to the new hardware within this project. The readout signal of the DLLs are the correlation values, the measured delay and the raw data. The raw data normally contains additional bits for data correction algorithms like Reed-Solomon encoding [30], to detect and correct bit errors.

5.2 ALL DIGITAL PHASE LOCKED LOOP

The phase readout of the interferometric beat notes happens in all digital phase locked loops, as described in Section 2.1.1. The performance and stability of the ADPLLs is critical for the system functionality and was investigated extensively. A linearized model of the ADPLL was developed and extended to account for the non-linear behaviors inherent to the algorithm. The model and its predictions were tested by performing digital performance tests to verify the phase noise levels and the ADPLL stability.

This work was also published in a paper [43] and it is included in the PhD thesis of O. Gerberding [42]

5.2.1 LINEAR MODEL AND NON-LINEAR EXTENSIONS

The linearizion of the ADPLL algorithm allows using standard control theory to find stable loop gains and to predict the propagation of noise sources through the system. Truncation noise sources in the ADPLL are inherently non-linear, and may produce irregular spurious signals. Therefore dithering and rounding algorithms were introduced in the VHDL implementations to reduce these noise sources and make their behavior stationary and predictable. The linear loop and its various components, noise entry points and readout points are shown in Figure 5.2.

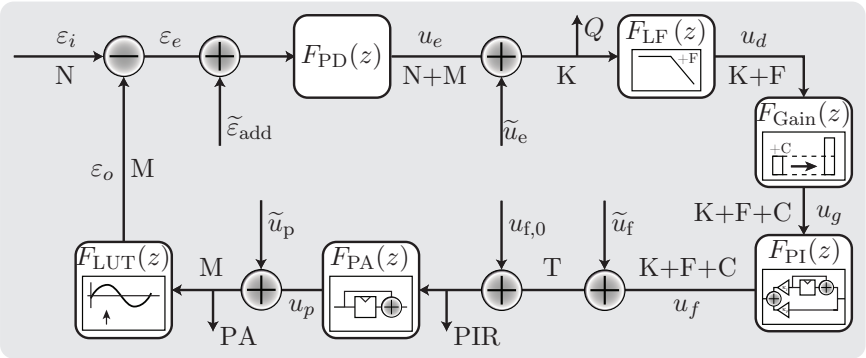
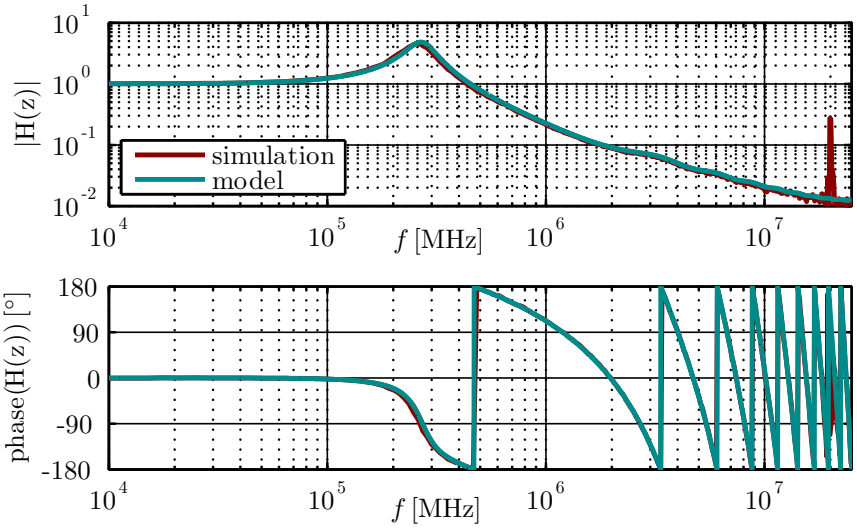


Figure 5.2: Block diagram of the linearized PLL model. Included are bit length indicators (N,M,K,F,C,T), possible truncation noise additions ($\widetilde{u}_e$, $\widetilde{u}_f$, $\widetilde{u}_p$), input additive noise $\widetilde{\varepsilon}_{\text{add}}$ and markers for signal readout points (Q, PA, PIR). Not shown here are the amplitude readout and the additional computation delay transfer function.

Simulations using the actual VHDL code of the ADPLLs were used to compare the expected closed loop transfer functions with the predicted one from the linear model. Except for the second harmonic, one of the well known non-linear effects inside phase locked loops that was treated separately, the model allows very good predictions.



Example of a closed-loop PLL transfer function $H(z)$ from a simulation and the linear model. Both curves are in very good agreement, save for the second harmonic at 20 MHz.

5.2.2 DIGITAL NON-LINEARITY TEST

Using digitally generated LISA-like signals the ADPLL was also tested for non-linear effects and stability. Three extremely different signals were generated such that their combined phase value combines to zero (see Figure 5.3). Measuring the residual noise gives insight into noise sources and non-linear effects, making this type of test the optimal set-up for future experiments with the full metrology system.

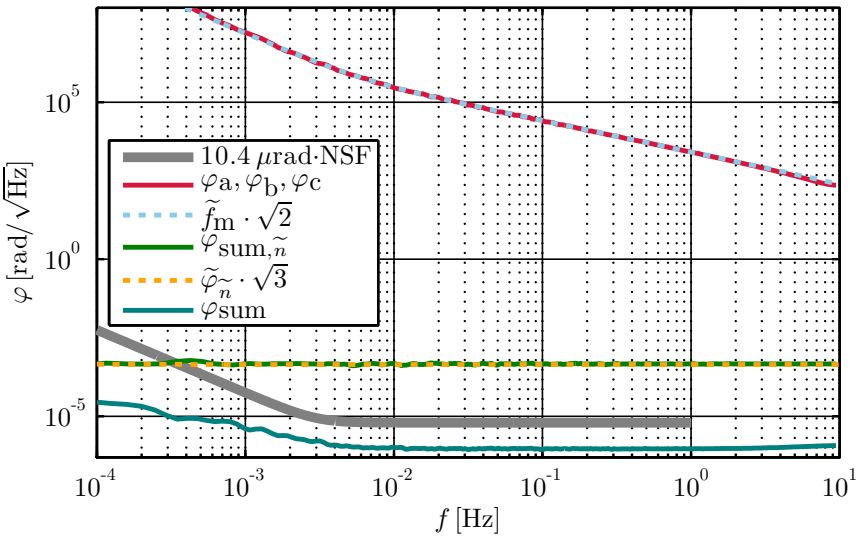


Figure 5.3: Shown are two measurements results of the non-linearity test, with additive noise (green), limited to the expected performance (yellow), and without additive noise (turquoise), demonstrating a dynamic range of 12 orders of magnitude at 1 mHz.

5.3 RANGING AND DATA TRANSFER

The ranging and data transfer functionality of the phase meter system is implemented by means of a delay locked loop (DLL). After initial development before this project [28], further development, optimizations, extensions and transfer to the new hardware was done within this project to increase its reliability and performance to fulfill the requirements of eLISA.

5.3.1 OPERATIONAL PRINCIPLE

To make ranging possible, a pseudo random noise (PRN) code is phase modulated onto the beatnote signal, generating multiple side bands, whose collective power does not exceed more than 1 % of the carrier power. The PRN code has a length of 1024 so called chips, each with a value of ± 1. Each chip is 32 clock cycles in length, which means the chip rate is 2.5 MHz. Since the bandwidth of the PLL is well below 1 MHz, these signals are not tracked by the loop and thus appear in the error point (Q output of the PLL), where they can be demodulated. On the receiving side, the remote PRN code will then be correlated with a locally generated copy. The code delay in the receiver that maximizes the correlation thus represents the signal travel time (and clock offsets). A spectrum of an PRN code modulated signal can be seen in Figure 5.4 which was published by Delgado et al. [28]. In addition to ranging, the DLL is also used to transfer 32 bits of data per PRN sequence. The data to be transmitted is attached to the PRN code by using a simple multiplication with ± 1. The resulting data modulated PRN code will then be phase modulated into the beatnote signal. On the receiving side, a simple multiplication of the local PRN code and the remote PRN code recovers the transmitted data.

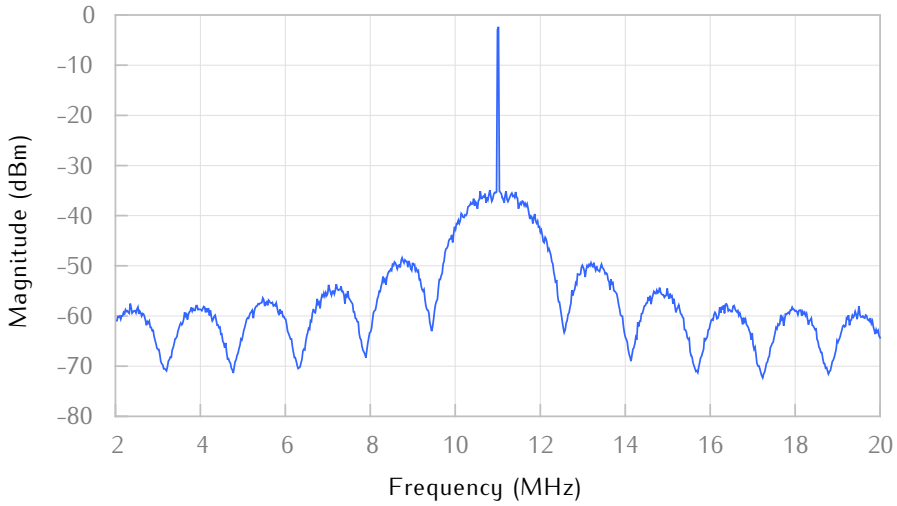


Figure 5.4: Spectrum of an 11 MHz carrier signal, which has been BPSK modulated with PRN code, published by Delgado et al. [28].

5.3.2 STRUCTURAL OVERVIEW

A standard DLL consists of four basic parts:

- The local PRN code generators
- The PRN code correlators
- The servo loop controller
- The control finite state machine

The generation of the local PRN code starts in a counter that is continuously counting. To this value a static start offset determined during the acquisition phase as well the actuator offset from the servo loop controller described below are added. The result is then used as an address for a look up table (LUT) that contains six different PRN codes (one each for the six one-way links). One of these codes is selected by the user and fed into the correlators.

The PRN correlator is used to correlate the input signal with the local PRN code and to recover the embedded data. To accomplish that, the input signal is multiplied with the locally generated PRN code and its result is then sent through a series of filters to calculate the correlation and recover the data. The first filter is an integrate-and-dump (IAD) filter, which dumps every data period (12.8 µs). The transmitted data bit is recovered from the sign bit of the output of this first IAD filter. After the first IAD filter, the absolute value of the output is calculated and sent to a second IAD filter, which dumps every PRN period (0.4 ms). Since the absolute filter eliminated the sign, the output of the second IAD filter is always positive and corresponds to the amplitude of the correlation between the input signal and the locally generated PRN code. A schematic block diagram of the correlator can be seen in Figure 5.5.

There are three of these correlators inside the DLL. One is the punctual correlator, which functions as describes above, and the other two are the early and late correlators. The difference between the early and late correlators and the punctual correlator is that the former use a local PRN code shifted by half a chip in negative or positive di-

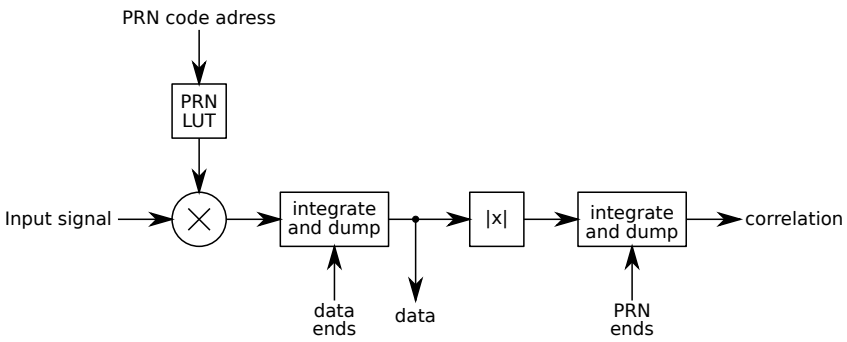


Figure 5.5: Schematic block diagram of a PRN correlator. The input signal is multiplied with the local PRN code and travels through a series of integrate-and-dump filters to extract the transmitted data and calculate the correlation.

rection. In case the punctual correlator has maximal correlation, the early and the late correlator detect a smaller but equal correlation. If the offset of the punctual correlator is slightly off-center, one of the other correlators has a slightly higher correlation than the other one. Therefore the difference of the early and late correlator can be used as an error signal for the loop controller.

The loop controller consists of a single integral controller, which takes the aforementioned difference of the early and late correlator as its input. An integral controller accumulates its input and multiplies the result with an user-configurable constant gain factor. The output of the integral controller is used as actuator signal and added as an offset to the PRN code address counter.

The control finite state machine (FSM) controls the handover process between acquisition mode and tracking mode and generates the timing signals for the IAD filters in the correlators. Special care must be take to achieve correct synchronization of the data bit boundaries. This required modifications to the classic DLL algorithm are described in [28, 44]. When the DLL starts, the FSM is in acquisition mode. In this mode all possible PRN code offsets are scanned until an offset with a correlation above a user supplied threshold is found. After that, the FSM switches to tracking mode where the aforementioned offset is not modified any more. In tracking mode, the loop controller as well as the early and late correlators are switched on to form a closed loop. It is possible to leave the tracking mode and switch back to acquisition mode, when the measured correlation falls below a second user supplied threshold. This is, however, only expected to happen when the PLL unlocks.

A complete block diagram of the DLL can be seen in Figure 5.6.

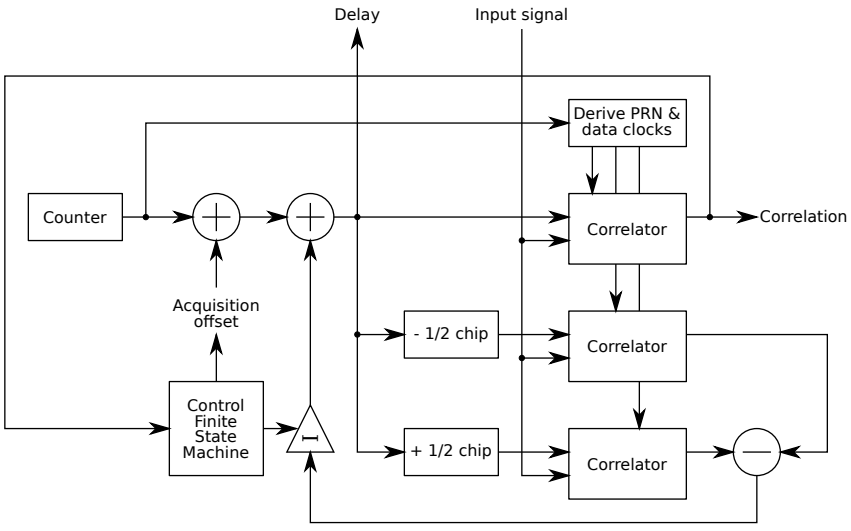


Figure 5.6: Schematic block diagram of a DLL. This includes the counters for the local PRN code address, the early, punctual and late correlators and the loop filter. All this is controlled via a finite state machine.

5.4 DECIMATION CHAIN FOR SCIENCE DATA

For the science data the decimation is implemented in three steps, shown in Figure 5.7. The initial data inside the FPGAs, available at the sampling speed of 80 MHz, is down-sampled by CIC filters to a much lower rate of ≈ 610 Hz and packed into data packets called frames. These frames are transmitted to the bridge, where they are combined and sent to the CPU. There the data is split into the original signals which are first mapped onto floating point numbers and then decimated in three consecutive steps by FIR filters. The final rate of 3.4 Hz is then used to store the data on a PC. The intermediate higher sampling rates of ≈ 102 Hz and ≈ 10 Hz are required for feeding data to a DFACS system. The multi-stop filtering also simplifies the design of the three FIR filters. Signals like counters and received DLL data are not filtered and are directly available in the CPU as integer values.

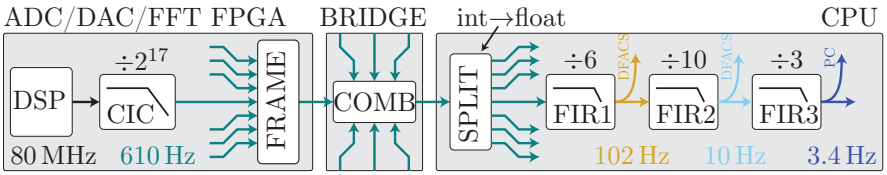


Figure 5.7: Shown is the decimation chain of science data in the EBB.

The most challenging signal, in terms of filtering, is the frequency information of the main PLLs, since it contains both the large inter satellite distance variations as well as the tiny gravitational wave signals. It has the widest dynamic range and spectrum, making its artifact-free decimation the most demanding. The other signals can potentially use much simpler filters that, for example, cause less signal delays, as required for DWS. Due to time constraints only the strong frequency decimation filters were implemented and they were

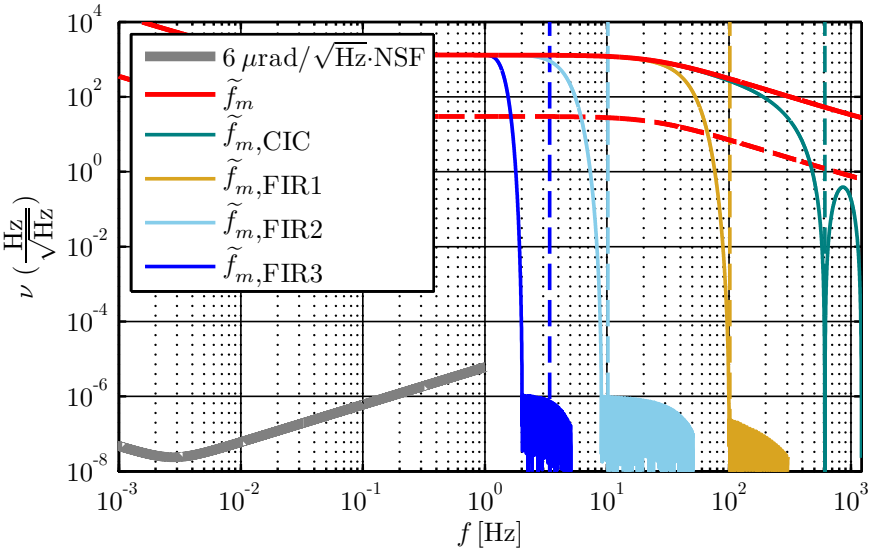


Figure 5.8: Shown is the effective laser frequency noise model used in the signal simulation and its attenuation in the different decimation steps. The dashed vertical lines mark the sampling frequencies, which are also the lowest frequencies that will be aliased into the signal band (> 1 Hz) during each decimation.

used for all signals. The frequency signals are fully dominated by laser noise, therefore the filter suppression can be computed by comparing the expected noise with the filter transfer functions.

Figure 5.8 shows the effective laser frequency noise model and its attenuation via the implemented down-sampling filters. The first stage is a third order CIC filter which has notches of suppression at all critical frequencies (only the first two are shown). The second, third and fourth stages are 54, 104 and 77 tap FIR filters respectively.

One should note that decimated variable is a frequency and not the phase, which implies a time derivative leading to frequency-dependent requirements. Future implementations might also include compensation ("whitening") filters to restore the signal flatness that is required for DWS, post processing and TDI. However, these filters might be computationally very expensive due to the strong constraints on the signal flatness required for the TDI algorithms that suppress noise by more than nine orders of magnitude. Therefore these filters might better be implemented in the on-ground data processing.

5.5 BEATNOTE ACQUISITION

The beat note acquisition (BNA) functionality of the phase meter system is used to find the frequency of an unknown beatnote signal in order to initialize the PLL tracking loop. The heart of the BNA system consists of a Fast Fourier Transform (FFT) and a simple peak finding algorithm. An important feature of the BNA is also the ability to exclude certain frequencies like the pilot tone, multiples of 10 MHz, which are commonly found in a lab environment or other fixed frequency interferers.

5.5.1 FAST FOURIER TRANSFORM

The FFT is a very fast algorithm that is used to calculate the frequency spectrum of an equidistantly sampled digitized signal. Its most popular variant has been developed by James Cooley and John W. Tukey in 1965[45]. This particular algorithm has been chosen, because it can very easily be parallelized, which is a huge benefit on an FPGA.

THEORY OF OPERATION The general FFT algorithm takes N complex numbers representing discrete amplitudes in the time domain and transforms them in such a way that the result also yields N numbers that represent discrete amplitudes in the frequency domain. In our case, the input to the FFT is the digitized AC photo current that comes from the ADCs and therefore is completely real data. When feeding a FFT with real data, the results are still com-

plex numbers. However, the output data X_k is symmetrical around the Nyquist-Frequency, which means that

$$X_{N-k} = X_k^*. \tag{7}$$

Due to this symmetry, a real FFT doesn't magically produce more data than it has been fed with and the number of resulting frequency bins is only $\frac{N}{2}$. However, the more important frequency resolution is not affected by this condition. For example, a FFT with $N = 1024$ points and a sampling frequency of $f_s = 80\,\text{MHz}$ results in a frequency resolution of

$$\Delta f = \frac{f_0}{N} = \frac{80\,\text{MHz}}{1024} = 78.125\,\text{kHz} \tag{8}$$

with a frequency span of 0 Hz to 40 MHz. To then get a real spectrum out of an FFT, the absolute value of the complex output has to be taken by multiplying it with its complex conjugate and then taking the square root. This however has the side effect of the loss of the phase information of the input signal, since there are now less output numbers then input numbers. Fortunately, the phase information is not relevant for BNA.

The FFT algorithm works by recursively dividing the computation of the $N = N_1 N_2$ input data points into smaller FFT of size N_1 respectively N_2 until N_1 and N_2 are prime numbers. The FFT algorithm from James Cooley and John W. Tukey only works for $N_1 = N_2 = 2$, which means that N has to be a power of 2. There are other algorithms that work for $N_1 \neq N_2 \neq 2$, but they are not as fast.

The final $N = 2$ FFT are simple 2 point discrete Fourier transformations (DFT) and are called "butterflies" in the context of FFTs. A FFT of the length N consists of

$$n = \frac{N}{2} \log_2 (N) \tag{9}$$

such butterflies and thus has a complexity of $\mathcal{O}(N \log N)$. As a comparison, a DFT that directly implements the defining formula has a complexity of $\mathcal{O}(N^2)$.

IMPLEMENTATION As actual FFT implementation, the proprietary FFT intellectual property block from Xilinx Inc. was chosen. Since the FPGAs we are using are also from Xilinx Inc., this particular implementation is very well optimized for our FPGAs. This results in high speed operation with low chip area usage.
The FFT also needs some surrounding logic to function properly. After the processing by the FFT, the absolute value of the output signal has to be calculated. In this case however, the square root operation is

omitted and the output is only multiplied with its complex conjugate. The reason is that the square root cannot be easily implemented in a FPGA. Also, we are only interested in the relative height of the amplitudes in comparison to others, for which the squared magnitude is just as good as the magnitude.

5.5.2 PEAK FINDER

The peak finder receives a serial stream of frequency/amplitude pairs and produces as result the frequency/amplitude pair with the highest amplitude. It further evaluates the user-defined list of frequencies to be ignored. The peak finder works by initializing an internal frequency/amplitude pair with 0/0 and replacing it with a new pair, whenever its amplitude is greater, ignoring all frequencies from the list. The internal frequency/amplitude pair is reset, whenever a frequency/amplitude pair with a frequency of 0 arrives. At that time the best frequency/amplitude pair found so far is forwarded as result and can be used as starting frequency for a PLL.

5.6 LASER CONTROL

A laser frequency offset phase lock has been implemented as one of the required auxiliary functions. The used algorithms are digital versions similar to analog servo controllers that have been used and studied before [40, 46].

The active laser control, performed by the phasemeter, uses the frequency information of the beat notes, determined in the ADC FPGAs, as shown in Figure 5.9. From these frequencies the desired offset frequency is subtracted to generate an error signal, which is then passed to a PI controller to generate a fast actuation signal that is sent to one of the DACs. The fast actuator signals is also fed into a another PI controller that generates a second slow actuation signal. Both of these signals are then used to drive the frequency of an NRPO laser

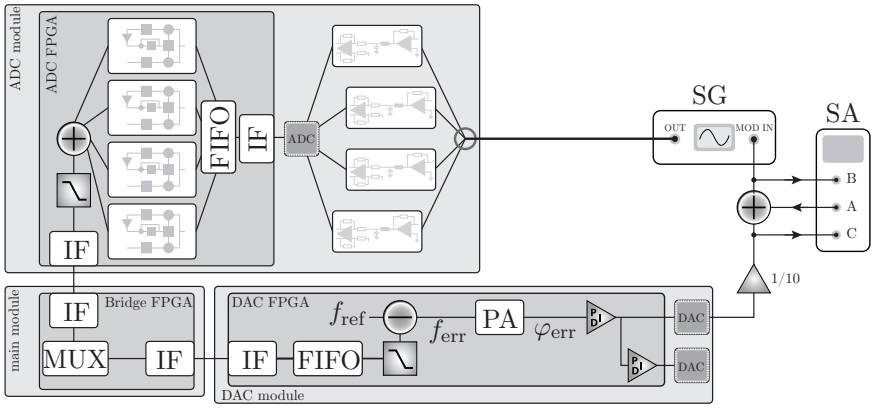


Figure 5.9: Schematic overview of the frequency offset phase lock inside the test set-up. The tests utilized a signal generator (SG) to simulate a laser source and an interferometer. A spectrum analyzer (SA) was used to measure the transfer function. The loop contains several interfaces (IF) designed for high bandwidth.

by actuating on the laser crystal with a piezo (fast) and with temperature (slow). This algorithm was tested successfully and the results are summarized in Section 7.2.4.

The system infrastructure also allows to implement more complex control algorithms inside the DAC FPGA, like arm-Locking [47] and alternative laser stabilization schemes [48]. These have, however, not yet been tested. ∎

Part III

TESTING

Testing the developed LISA metrology system (LMS) is a crucial part of the presented work. Testing all the required functionalities is conceptually straightforward and was in part implicitly covered during performance measurements. The required µcycle noise performance, however, is very hard to verify. The reason is that our aim is to build the best available phasemeter, including lab devices, such that no reference measurement equipment exists against which our results could be compared.

Hence the only remaining possibility is to test the PMS against itself. In the scope of this project we compared the output of two channels that process the same input signal against each other. Realistic (LISA like) input signals were produced electronically by a custom designed signal generator and measures were taken to reduce temperature fluctuations which had initially turned out to limit the performance of the LMS. Parts of the frequency distribution subsystem were also tested electro-optically extending the initial scope of this project.

Conducting more significant but also more difficult "3 signal tests" will represent a milestone in future testing of the developed LMS. Such a test is described in Section 5.2.2 in the digital domain but will also have to be performed with optical signals including timing jitter correction of independent reference oscillators.

6 TEST ENVIRONMENT

During this development activity the LISA metrology system was tested using only electronic signals and equipment; no optical systems were involved. However, since the system behavior depends strongly on the input signal dynamics and spectrum, a dedicated signal simulator was designed and used for the tests. The coupling of temperature fluctuations into phase noise also required to perform some of the test in with actively stabilized temperature environments.

6.1 SIGNAL SIMULATOR

The LISA Metrology System was to be tested with realistic signals that share the same characteristics as the photodetector outputs in the LISA interferometry system. This requires:

- Three sinusoidal **tones** with adjustable but fixed frequency difference in each channel.
- Simultaneous frequency shift of all three tones to simulate Doppler shifts, laser frequency noise and laser frequency sweeps.
- Simulation of laser frequency noise from mHz to MHz Fourier frequencies.
- DS/SS phase modulation of the central tone with small modulation index, using **PRN codes**.
- White amplitude noise of well-controlled spectrum and level.
- Variable output level.

The central **tone** (carrier/carrier note) has a higher amplitude. The others represent the sideband/sideband beat notes.

Data must be modulated on top of the **PRN code** with variable rate and well-known contents.

There are multiple options to generate phase modulated sinusoidal signals, three of which we considered in particular.

1) COMMERCIAL SIGNAL GENERATORS which, however, are limited to sinusoidal tones with at most a sinusoidal frequency modulation, and hence fulfill only a subset of the above requirements.

2) REAL OPTICAL INTERFEROMETERS which provide the most realistic signals, but are not transportable, much less reliable and may contain other noise sources making debugging very difficult.

3) DEDICATED SIGNAL GENERATOR custom designed to fulfill the above requirements.

In the end, we chose to develop a custom digital signal simulator (DSS). It was used to test the functionality and performance of the LISA Metrology System during development and in the final testing phase. Several copies of the signal generator can be used simultaneously in different experiments.

6.1.1 ARCHITECTURE AND IMPLEMENTATION

The hardware of the developed DSS and its architecture are shown in Figure 6.1 and Figure 6.2. A signal synthesis core is implemented in an FPGA and connected to four DAC-channels. Each DAC-channel consists of an digital-to-analog converter, low-pass filter and a number of operational amplifiers used for signal conditioning. The signal simulator is controlled by the user via three USB-interfaces. A set of expansion connectors can be used for connecting different boards like

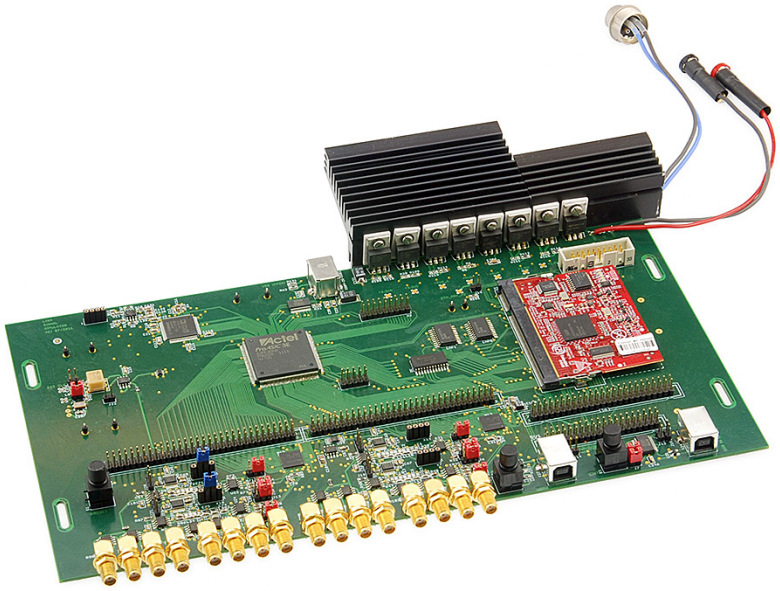


Figure 6.1: Digital signal simulator PCB featuring a field-programmable gate arrray (FPGA) in the center, a microcontroller board (right), digital-to-analog converters (bottom), multiple slots for analog noise generator and expansion connectors and USB ports.

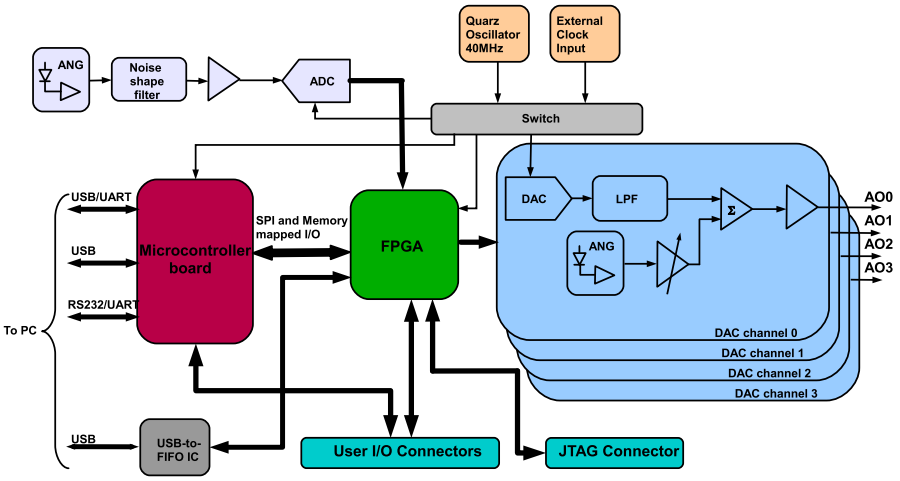


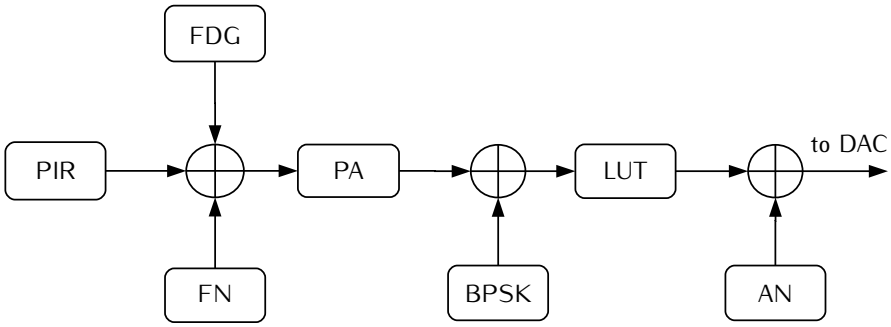
Figure 6.2: Signal simulator architecture. The signal synthesis core is implemented in FPGA and connected to four DAC-channels. Each DAC-channel consists of a digital-to-analog converter, low-pass filter and of operational amplifiers for signal conditioning.

user-made DAC and ADC cards, noise generators, memory devices and interface modules.

Signal parameters needed for a certain PMS test are specified in a configuration file which is stored on a PC. Software that communicates with the signal simulator via one of the USB-ports sends these parameters and starts the DSS.

6.1.2 DIRECT DIGITAL SYNTHESIS

In our signal simulator we used the well-known and widely used direct digital synthesis (DDS) concept. [49] All functional blocks of each DDS signal channel as shown below are implemented in the FPGA using VHDL.



DDS single channel structure. PIR: phase increment register; PA: phase accumulator; LUT: look-up table with digitized sine wave; FDG: frequency drift generator; FN: frequency noise generator; BPSK: binary phase-shift keying; AN: amplitude noise generator

In order to generate all signals that are needed for PMS testing, outputs of several (three in our case) such channels are added and passed to a digital-to-analog converter.

SIGNAL SPECTRUM A typical signal spectrum produced by the signal simulator is shown in Figure 6.3 (green trace). It includes the carrier/carrier tone at 23 MHz, two sideband/sideband tones at 22 MHz and 24 MHz and the DS/SS PRN modulation for inter-spacecraft ranging and data transfer which can be adjusted in modulation depth.

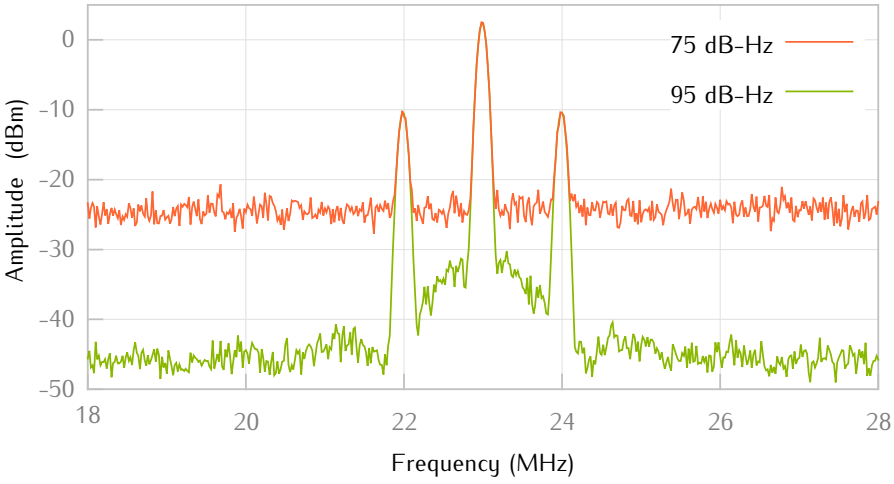


Figure 6.3: Full output signal spectra of the digital signal simulator (DSS) with different amplitude noise levels to simulate the expected signal-to-noise ratios.

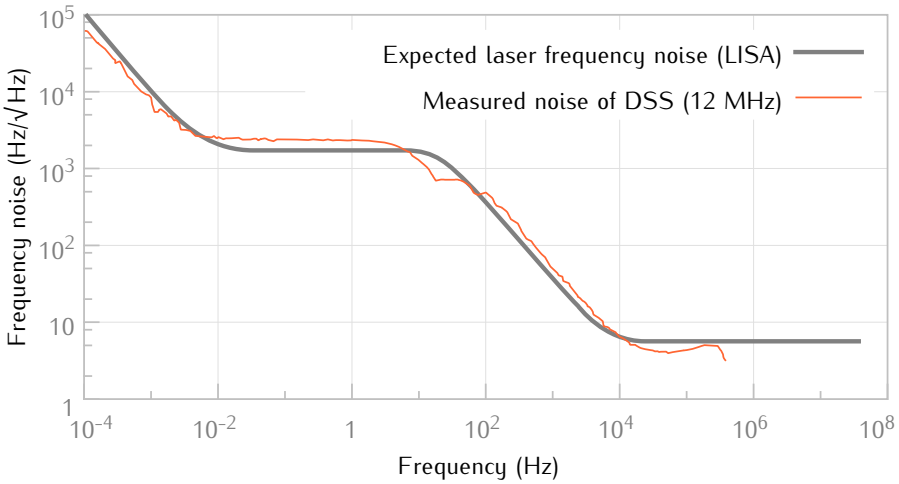


Figure 6.4: Laser frequency noise generation. The measured frequency noise linear power spectral density (red curve) meets the requirements (expected laser frequency noise of LISA plotted in gray).

NOISE GENERATION A white noise floor was added by the DSS using either an analog noise generation device or a digital white amplitude noise generator, implemented in the FPGA. Both noise sources are functionally equivalent and simulate the expected signal-to-noise ratios. The red trace in Figure 6.3 corresponds to 75 dB Hz PND, and the green trace to 95 dB Hz. The total signal power is 3 dBm.

On top of this there is a frequency noise simulation function of the DSS that was implemented in the FPGA. It contains three main blocks: a generator of white Gaussian noise, an integrator and a low-pass filter. The combination of these three units allows to generate the desired frequency noise spectral density (Figure 6.4).

A drift of up to $11\,\mathrm{Hz\,s^{-1}}$ can be added to the signals' frequency to simulate spacecrafts movement. The range of the frequencies for the carrier/carrier tone is $2 \ldots 25\,\mathrm{MHz}$ and hence even wider than required.

6.2 TEMPERATURE CONTROL

The excess noise of phase performance measurements due to temperature fluctuations is often the limiting effect for sensitive measurements at mHz frequencies. Reducing these fluctuations was done in two steps.

The first measure was to use a temperature stable laboratory for such measurements. That room at the AEI in Hannover is deep within a larger building, it is not connected to the outside via walls or windows and it has no other sources of heat other than the measurement equipment itself. The room is also not actively cooled, allowing any constant heat generating system to reach a very stable thermal equilibrium. Additional passive isolation can further improve this.

However, the thermal equilibrium in a well isolated system will always be accompanied by a high average temperature, which is only feasible for some parts of the breadboard.

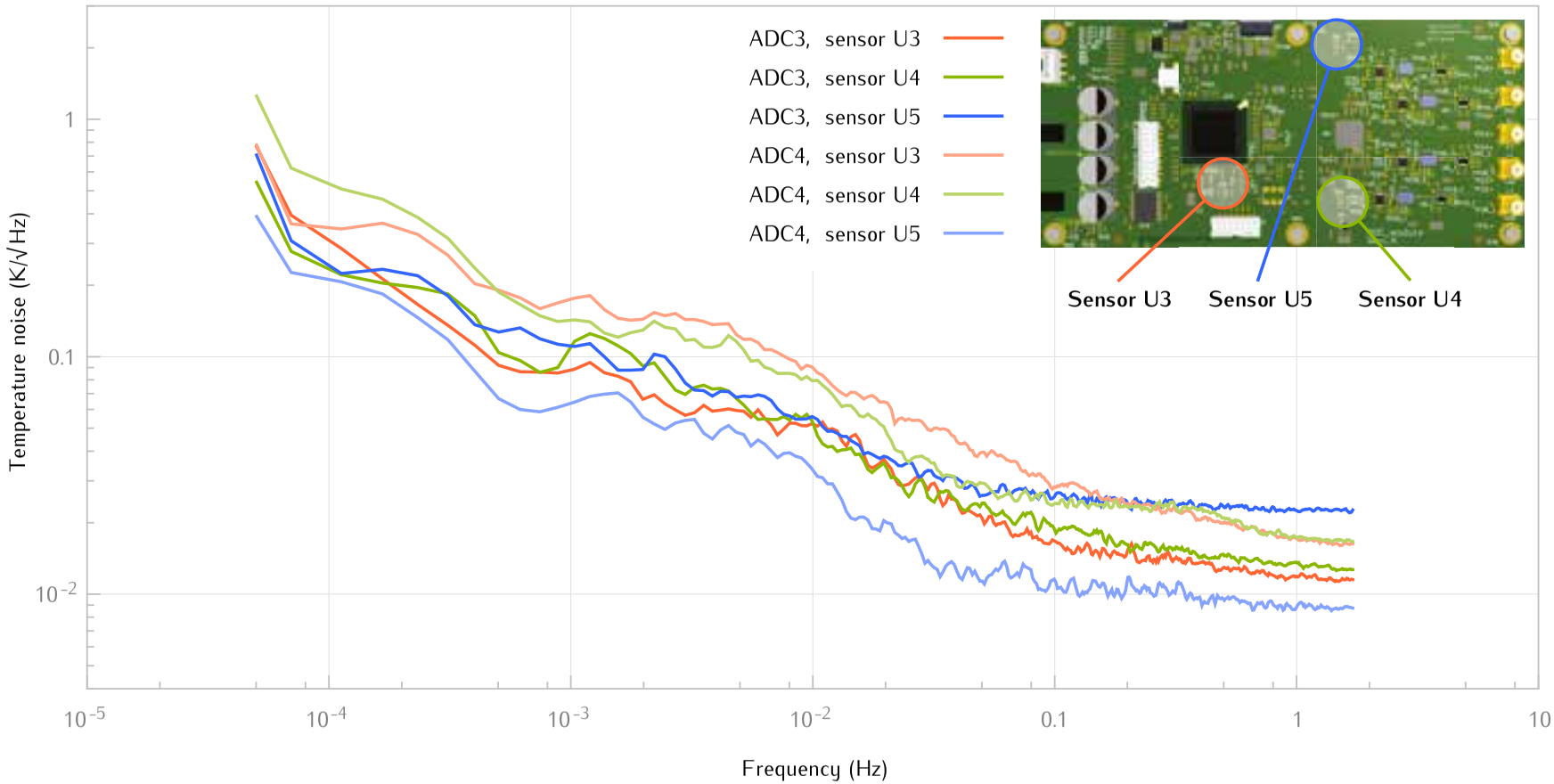


Figure 6.5: Spectrum of the thermal noise with active temperature control. The data is taken from the temperature sensors on the ADC modules in slots 3 and 4 of the EBB during the measurement campaign. The location of theses sensors is indicated on the top right.

Performance tests with the full system did not allow to use such strong passive isolation due to two reasons. The heat generated by the breadboard would raise the temperature to levels far above the operating limits of individual components, risking emergency shut downs or even damage to the system. The second reason concerns the fluctuating heat dissipation of the breadboard itself. The tests revealed that the thermal noise generated by the system itself can spoil its phase measurement performance. Both of these issues could only be addressed by introducing means to actively control the breadboard temperature.

6.2.1 ACTIVE TEMPERATURE CONTROL

The thermal stability of the analogue front-end had to be actively stabilized to reach the required accuracies. For this purpose a temperature controlled housing was built for the breadboard model that utilized a commercial thermal control unit to realize a constant temperature within the box. Fans on both side of the control unit coupled the respective air volume to the two heat exchangers, one mounted on the outside of the box and one on the inside which can be seen in Figure 6.6. The temperature gradient between these heat exchangers was then actively regulated by a Peltier element between them, which used temperature data from an independent thermal resistor inside the box as sensor for the control loop. The loop parameters and air flow had to be optimized to achieve the required thermal stability of the analogue components. The temperature sensors on the breadboard were used for out-of-loop measurements to monitor the effect of the active control. The best stability achieved during testing was just sufficient to achieve all performance levels during the measurement campaign. A corresponding temperature spectrum is shown in Figure 6.5. More details on the implementation and development of the stabilization can be found in the Test Report [TN41]. ∎

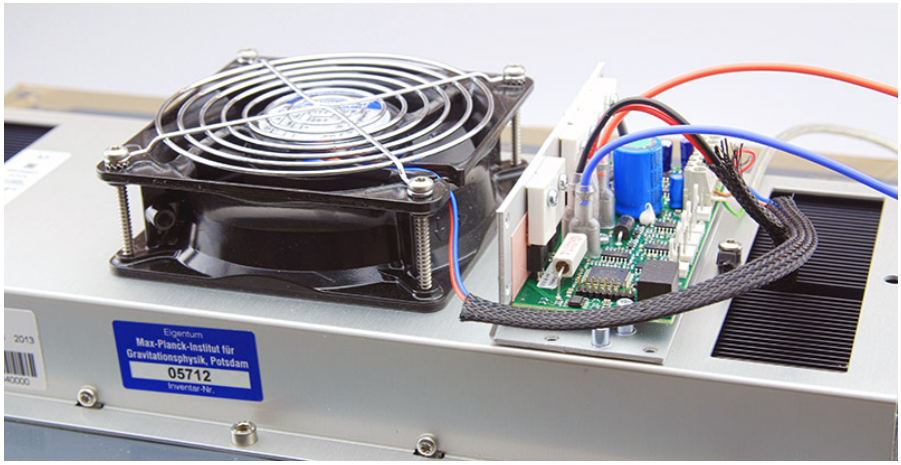


Figure 6.6: Cooling unit for active temperature stabilization.

7 TEST RESULTS

An extensive measurement campaign of the breadboard model has been conducted to investigate critical performance levels and to demonstrate various functionalities.

Initial tests were performed on single modules and simplified input signals that revealed complications early on in the campaign. After minor system modifications the full LISA metrology system as developed within the scope of this project and the implemented algorithms were able to meet all requirements.

In the following the most relevant results are summarized. The full test results are documented in technical note 4-1 [TN41].

7.1 ADC MODULE

We built a stand-alone phase measurement system based a single ADC module with a separate dedicated USB readout module for communication with a dedicated computer. This excludes the additional complexity of the main processing board.

We were able to reproduce all results on phase noise performance (DPLL) as well as ranging and data transfer (DLL) obtained with the first generation phasemeter described in Section 3.2.

7.1.1 DELAY LOCK LOOP (DLL)

The Delay Locked Loop proved to be capable of tracking a PRN modulated signal with a very low SNR of 75 dB Hz.

While maintaining a data rate of more than 15 kbit s^{-1}, a bit error rate (BER) of less than 10^{-6} could be achieved using using the Bose-Chaudhuri-Hocquenghem coding for bit error detection and correction. Additionally the timing delay was measured and found to differ less than 3 ns from the expected values.

All this has been successfully tested for a total of five different PRN codes, each at two different frequencies and over a measurement period of one hour.

7.1.2 DIGITAL PHASE LOCK LOOP (DPLL)

A zero measurement scheme as presented in Figure 7.1 with frequency generators producing input signal and pilot tone was used for initial evaluation of the signal tracking and phase measurement sensitivity of the ADC module.

During these tests a better ADC driver compared to the previously implemented one was found. It was used in all further measurements for both stand alone and full systems.

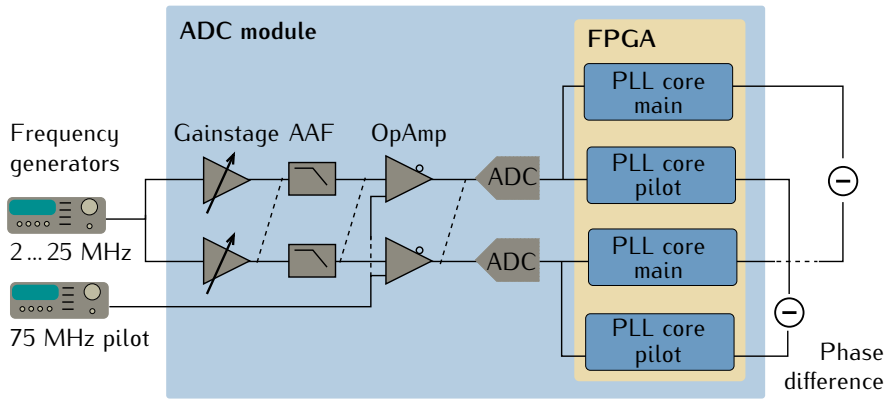


Figure 7.1: Setup for the functionality and noise performance testing. Dashed lines in the analog front-end chain show places of possible short circuits which can be used for excluding certain parts of the analog front-end from the experiment.

Final performance measurements presented in Figure 7.2 were done using the signal simulator with full signal spectra, including carrier and sideband tones, PRN-modulation, and amplitude and frequency noise. All requirements were met over the whole frequency range 2 . . . 25 MHz. The performance strongly depends on the temperature stability though and requirements can only be met using passive or active temperature control.

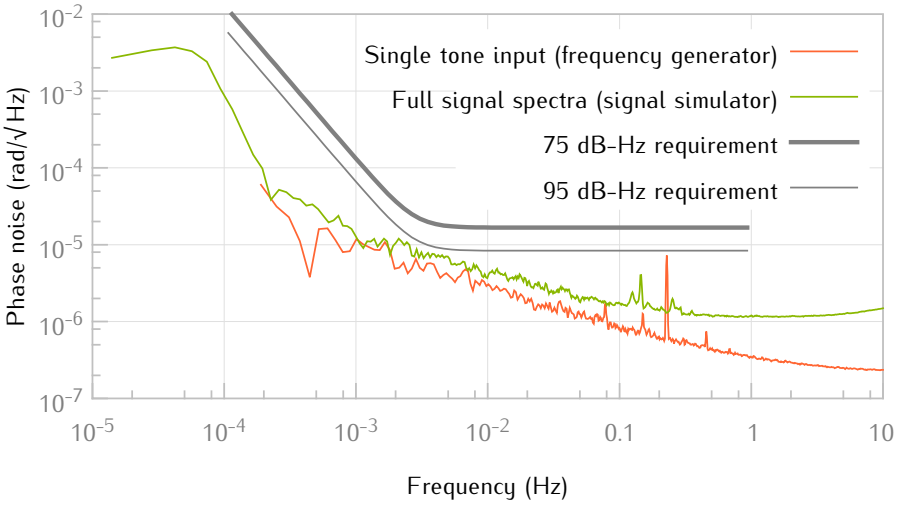


Figure 7.2: Stand-alone ADC module DPLL performance with single tone input (red) and full signal spectra (green) performed with passive thermal isolation for 24 MHz signals and ADC jitter correction by a 75 MHz pilot tone.

7.2 AUXILIARY FUNCTIONS

Further evaluation of functionality and performance required the full LISA Metrology system as developed in the scope of this project. The following tests describe the beat note acquisition for initial lock of the phase measurement system, the support functions for the drag-free and attitude control system (DFACS) with differential wavefront sensing readout as well as PRN code generation for ranging and data transfer and laser frequency control for offset locking.

7.2.1 BEAT NOTE ACQUISITION

The Beat Note Acquisition System was able to detect five different beat note frequencies and successfully locked a PLL on this frequency. This yielded a frequency difference of less than 5 mHz compared to the expected value, measured by a reference PLL. Such a lock takes only a few seconds and a sample graph showing both the reference PLL frequency and the acquisition PLL frequency is shown in Figure 7.3.

The PMS was designed to easily cope with the maximum expected sweep rate of the beat note signal. Since the DSS supports a maximum sweep rate of 11.322 Hz s^{-1}, sweep rates up to this value have successfully been tested.

Using a previously developed phase meter with the same beat-note acquisition system, even beat-note signals with much higher sweep rates could be acquired. This was achieved by using a free-running heterodyne laser system. Therefore sweep rates in the range of several kHz/s would also be possible with the current PMS.

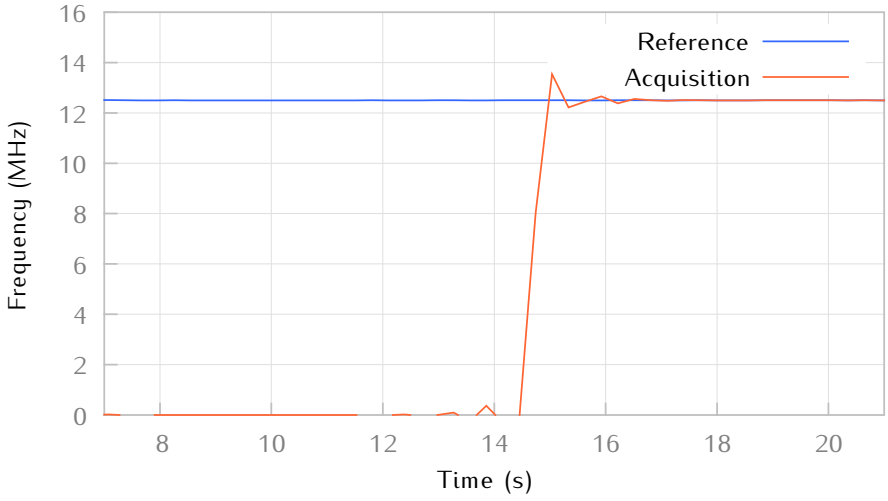


Figure 7.3: Sample acquisition sequence for a frequency of 12.5 MHz, showing reference and acquisition PLL frequencies over time.

7.2.2 DFACS SUPPORT

The LISA metrology system performs the readout of differential wavefront sensing (DWS) signals, which are used to measure the tilt of the test mass relative to the satellite and the attitude between the satellites. This information has to be communicated in real time to the drag-free and attitude control system (DFACS), where it is used to actuate the orientation of the satellite and the test mass. This functionality was verified in a two step process. The availability of the data at sampling rates around 10 Hz 100 Hz was achieved by design, as described in Section 5.4.

The performance of the DC phase readout, which is essential for DWS, was tested by performing a measurement of a signal and a delayed version of it, generated by additional cable length. By using the knowledge of the cable length the earlier signal was then artificially delayed with an interpolation filter. This computed signal was then subtracted from the later received one to determine that the performance was below the requirement of $120\,\mu\text{rad}/\sqrt{\text{Hz}}$ electrical phase difference. Due to the optical gain of the DWS readout, this corresponds to $\approx 10^4$ times smaller physical angels. This also showed that the measured phase difference of the non-delayed signal to the later received one was correct, proving the capability to perform DC phase readouts.

7.2.3 PRN CODE GENERATION

The LISA metrology system also requires to be able to generate pseudo-random noise (PRN) including decoded data for the inter satellite ranging and communication. Therefore the PRN generation on the breadboard, implemented in the DAC FPGA, was tested by monitoring and recording the generated signals with an oscilloscope. The PRN codes were then analyzed to verify the correct repetition rates, the desired cross-correlation properties and no artifacts. Possible data encoding and time stamping were implemented as well, however these functions could not be tested without additional, more complex set-ups.

The communication between two or more breadboards connected via optical links is the most promising and realistic set-up for performing integrated tests of the PRN generation and readout in the future.

7.2.4 LASER FREQUENCY CONTROL

The ability to perform an active laser lock with a closed loop bandwidth of 10 kHz or more is one of the most critical aspects for the modular design of the metrology system. The lock (an overview is shown in Section 5.6) utilized several FPGAs and components, and to achieve the desired bandwidth the total delay of all the interfaces, the algorithms and the converters was required to be below 3 µs. Even though the system design accounted for this, a closed loop test was conceived to measure the actual delay of the system and to demonstrate the phase locking capabilities.

The laser lock capability was tested by locking a commercial signal generator to the LISA metrology system. The actuation signal generated from the DAC module was therefore fed into the analogue frequency actuation input of the signal generator, mimicking the set-up for a real laser lock. The signal generator output signal was fed into one ADC module in the breadboard, thereby closing the control loop.

Several of these locks were performed for more than 1 hour at various signal frequencies. The analogue actuation signal was also fed through an adder circuit, allowing to measure the closed loop response with a commercial network analyser. The comparison between the measured loop gain and a linear model (shown in Figure 7.4) was used to determine the delay caused by the breadboard infrastructure. Excluding some initially unknown but now resolved delays in the set-up it was possible to demonstrate a delay of less than 3 µs.

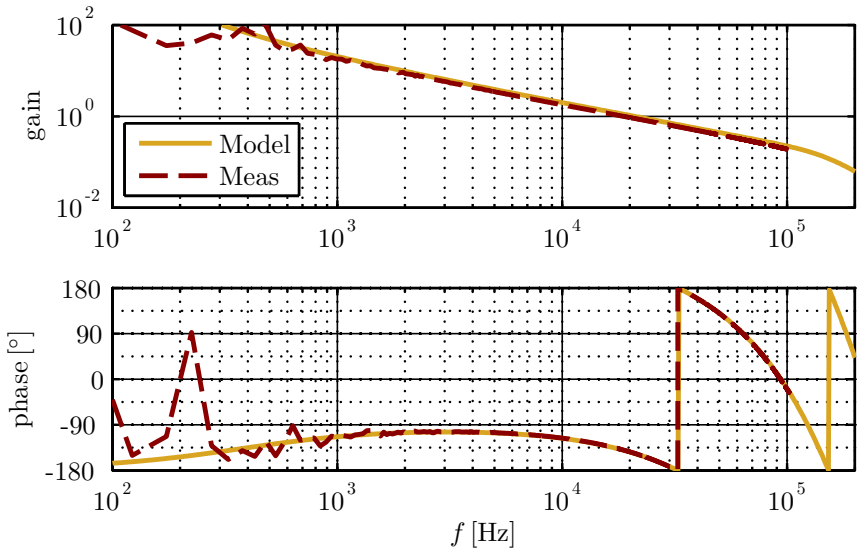


Figure 7.4: Shown is a comparison of the modeled and measured transfer function of the offset frequency phase lock. Unity gain is at ≈ 20 kHz with a phase margin of more than 30°.

7.3 FREQUENCY DISTRIBUTION SUBSYSTEM

To guarantee a stable pilot tone generation and distribution, it was decided to remove some components of the FDS from the second generation pilot tone board as described in Section 4.1.3. To provide full functionality, we evaluated replacement stand alone components. These components (like reference oscillator mixers, modulation power combiners and electro-optic modulators) are only necessary for optical measurements that include inter-spacecraft pilot tone transfer and ranging, which were not part of this project.

7.3.1 PILOT TONE MODULE

The pilot tone module itself produces a differential 80 MHz square wave signal (the system clock) and one single-ended 75 MHz sinusoidal signal (the pilot tone).

PILOT TONE GENERATION The pilot tone is used to correct for ADC timing jitter in the phase measurement system. For a stand alone system no specific stability of the pilot tone is required. This is different when multiple systems are used with individual reference oscillators. Here, the oscillators phase noise is modulated onto laser beams and transmitted to the other phase measurement systems for constellation wide pilot tone jitter correction as described in Section 2.1.3. In this scheme, timing noise between any two pilot tone generation chains shows up. Since optical testing was not part of this project, the performance of two pilot tone modules was tested against each other. The required timing stability was reached as shown in Figure 7.5.

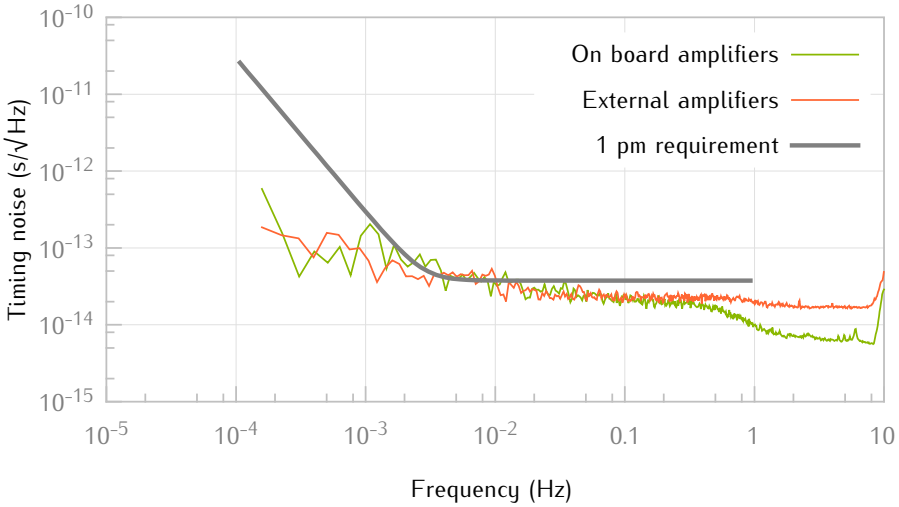


Figure 7.5: Timing fidelity measurement of the pilot tone generation chain with the on board amplifier (green) and the amplifier replaced by a stand alone alternative (red). Phase measurements were performed differentially at 75 MHz, converted to timing noise and divided by $\sqrt{2}$ to represent the noise of a single device.

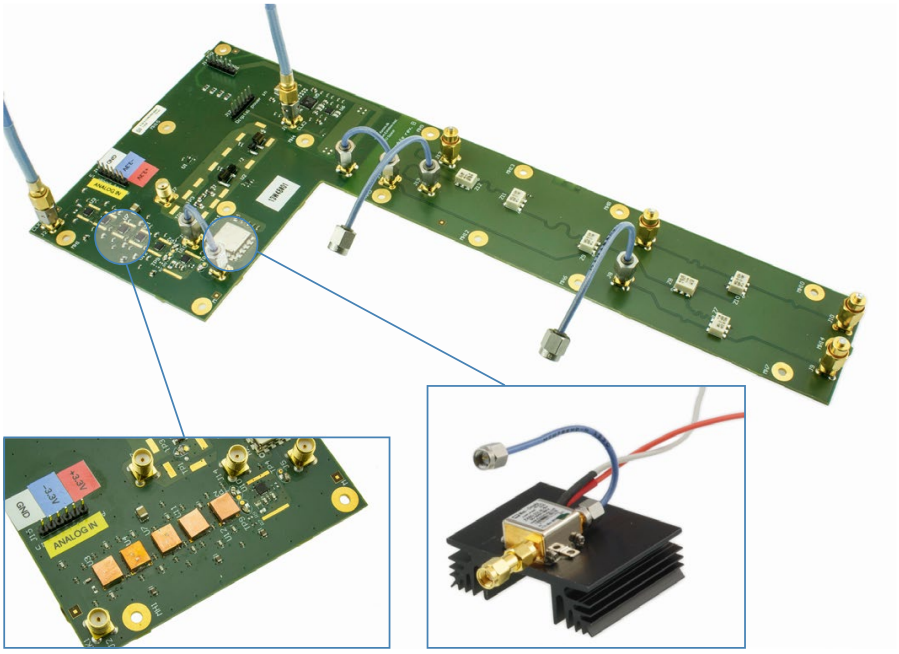


Figure 7.6: Second generation pilot tone module modifications. The original pilot tone module (top) with incoming 2.4 GHz signals for the pilot tone generation (upper left corner) and system clock division (center top). Unused outputs of the pilot tone distribution are terminated. To reach full performance, the pilot tone dividers were individually shielded by copper caps (bottom left) and the on-board amplifier was replaced by a stand alone alternative (bottom right) that was connected to a heat sink for better heat dissipation.

While the pilot tone module in its original form achieved performance under certain thermal conditions, smaller modifications improved the heat dissipation and made it easier to meet the required timing stability with the given test setup. These modifications are shown in Figure 7.6 and include 1) replacing the on-board amplifier by a stand alone alternative connected to a heat sink and 2) installing copper caps for shielding of the pilot tone dividers. The phase shift over temperature for this pilot tone module was found to be $0.49 \pm 0.04\,\mathrm{mrad/K}$ over the temperature range between 17 and 23 °C.

SYSTEM CLOCK GENERATION There are no hard requirements on the system clock, but the evaluation of the full phase measurement system was done with a system clock generated by the pilot tone module which had no impact on the overall performance. Hence the generated clock signal is suitable.

7.3.2 ADDITIONAL COMPONENTS FOR FULL FDS FUNCTIONALITY

Auxiliary functions of the Frequency Distribution Subsystem (FDS) are not placed on the pilot tone module itself but implemented as stand alone components. The reference oscillator mixer (Figure 7.7, right) that produces a differential signal to compare the two GHz reference oscillators for excess noise removal in post processing consists of a power splitter, a frequency mixer and a low-pass filter. The modulation combiner (Figure 7.7, left) which adds the PRN code (ranging and data transfer) and the native GHz reference oscillator signal (pilot tone jitter correction) for optical phase modulation consists of a

Figure 7.7: Implementation of FDS auxiliary functions. Left: modulation combiner, right: reference oscillator mixer.

power combiner and two filters for better isolation of the input ports. A pilot tone bridge custom made from a PTFE-free semi-rigid cable with additional high-pass filters to suppress cross talk was designed to pass the pilot tone from the FDS to the ADC modules.

The timing fidelity of all these components is shown in Figure 7.8. Two reference oscillator mixers and pilot tone bridges were tested differentially and provide exceptional timing accuracy. The reference oscillator mixer was tested in depth outside the scope of this project. It was used in an optical experiment by Delgado et al. [29] who verified that sidebands present in the PRN modulation do not affect the ranging accuracy. Barke et al. [21] used electro-optic modulators (EOM) to modulate GHz sidebands onto laser beams. The timing fidelity of these sidebands was meeting LISA requirements even when a PRN modulation – added by the modulation combiner as described above – was present. As a result, full functionality of the developed Frequency Distribution Subsystem is proven and all stability requirements are met, providing the basis for further optical tests of the LISA Metrology System.

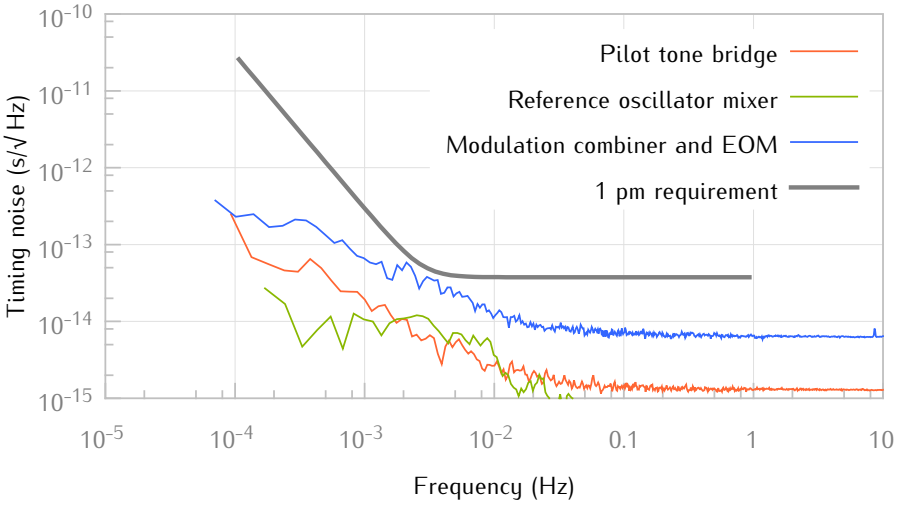


Figure 7.8: Phase measurements for the pilot tone bridge (red) and reference oscillator mixer (green) were performed differentially at 75 MHz, converted to timing noise and divided by $\sqrt{2}$ to represent the noise of a single device. An individual modulation combiner (blue) was evaluated electro-optically with 2 GHz sidebands and PRN code present modulated by an EOM.

7.4 FULL SYSTEM PHASE PERFORMANCE

The most critical tests for the breadboard are the phase noise performance measurements with the fully assembled system. They reveal the noise performance between independent ADC modules and ADCs, they utilize the complete system architecture, including the bridge FPGA, the CPU and the interface to a PC, and they reveal temperature or other influences from the clock, DAC or main module. In short, these measurements determine if the LMS as a complete system is able to perform its main function.

A comprehensive test campaign was conducted to determine the phase noise performance levels for various input signals. It was preceded by additional measurements that were done with varying means of temperature stabilization, signal distribution and signal parameters. These initial measurements were done to determine the set-up configuration to achieve optimal performance. Altogether more than 50 measurements with a duration of more than 12 hours each were performed.

The basic testing scheme that was used for the assembled system is the zero-measurement described in Section 7.1. An LMS consisting of two ADC modules, one main module, one DAC module and one pilot tone module was used for the tests. LISA-like signals generated by the dedicated signal generator were split and fed into the eight input channels of the two ADC modules. The respective ADPLLs in the LMS measure the phase of the carrier tones, of the side band tones and of the pilot tones simultaneously. The so generated signals are then filtered, decimated and stored in a PC. The pilot tone correction, as well as the spectrum estimation is then done with the PC data.

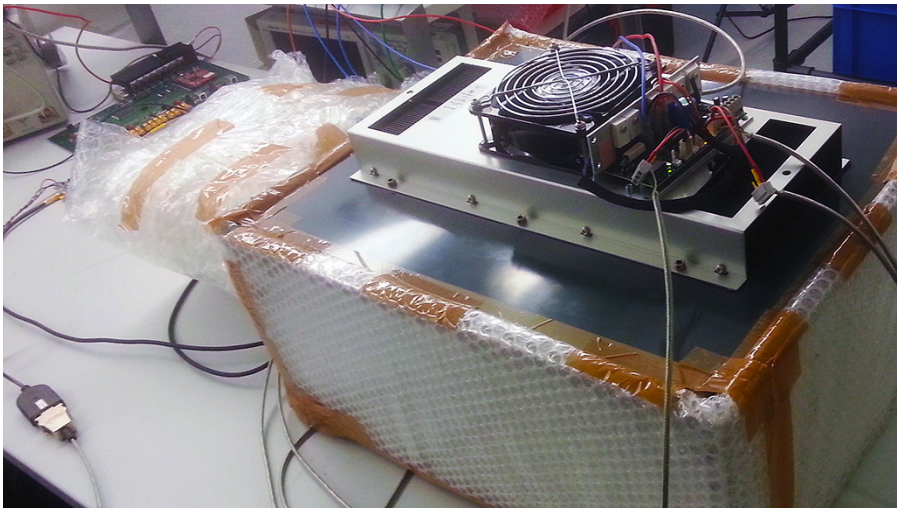


Figure 7.9: Photograph of the measurement set-up for the full system tests. The LMS is enclosed in the active thermal control housing. The input from the signal generator is fed through an 8-way splitter and the distributed to the LMS. The resistive splitter is thermally isolated by four layers of bubble wrap foil (shown on the left of the housing).

The two most significant modifications that were required to achieve full performance were active temperature stabilization and an improvement in impedance matching. The influence of temperature fluctuations caused excess noise at low frequencies, which even for good passive isolation of the analogue front-end spoiled the performance at the knee of the requirement curve (3 mHz). The active stabilisation described in Section 6.2.1 finally allowed achieving the desired performance.

An unknown noise source also caused excess white noise with unequal levels in some of the channels. The coupling of this effect is not yet understood. However, this noise was not present when a commercial signal generator was used as input source, which was locked to the LMS clock. The different signal dynamics between these two cases are currently understood to be the reason for the different coupling of this noise. Non-optimal impedance matching was thought of as a possible source of this and investigated experimentally. By optimizing the resistor values of the resistive signal splitter that was used to distribute the signal to the eight channels, it was indeed possible to reduce this noise in most of the channels below the requirement. One channel (4D, channel D on the ADC module in slot 4) was intentionally left poorly matched. Thereby the behavior of the noise level was monitored during the full measurement campaign, revealing its dependency on the frequency and SNR of the input signal.

All experience gained with the EBB during the testing campaign is summarized in the technical note 5-1 [TN51].

Throughout the measurement campaign the phase noise performance for tracking the carrier signals and side band signals was validated for a wide range of input frequencies and for two cases of additive noise levels: one corresponding to the inter satellite link with low received power (75 dB Hz) and one corresponding to the local interferometer configurations with higher received powers (95 dB Hz). For all cases and all tones the requirements were met. The most critical performance measurement was for the lowest SNR (75 dB Hz) and for the highest input frequency (25 MHz), because the influence of temperature fluctuations rises with the signal frequency, due to the coupling mechanisms in the analogue components. For this case a performance level of $12 \times 10^{-6}\,\mathrm{rad}/\sqrt{\mathrm{Hz}}$ was required and the results for one of the corresponding measurements are shown in Figure 7.10. Except for the earlier described excess noise in channel 4D the noise levels are significantly below the requirement. This measurement also utilized the second generation pilot tone module for distributing the pilot tone to the ADC modules and for providing the system clock. Reaching this performance is the final proof for the feasibility of the overall system architecture of the here developed LISA Metrology System. ■

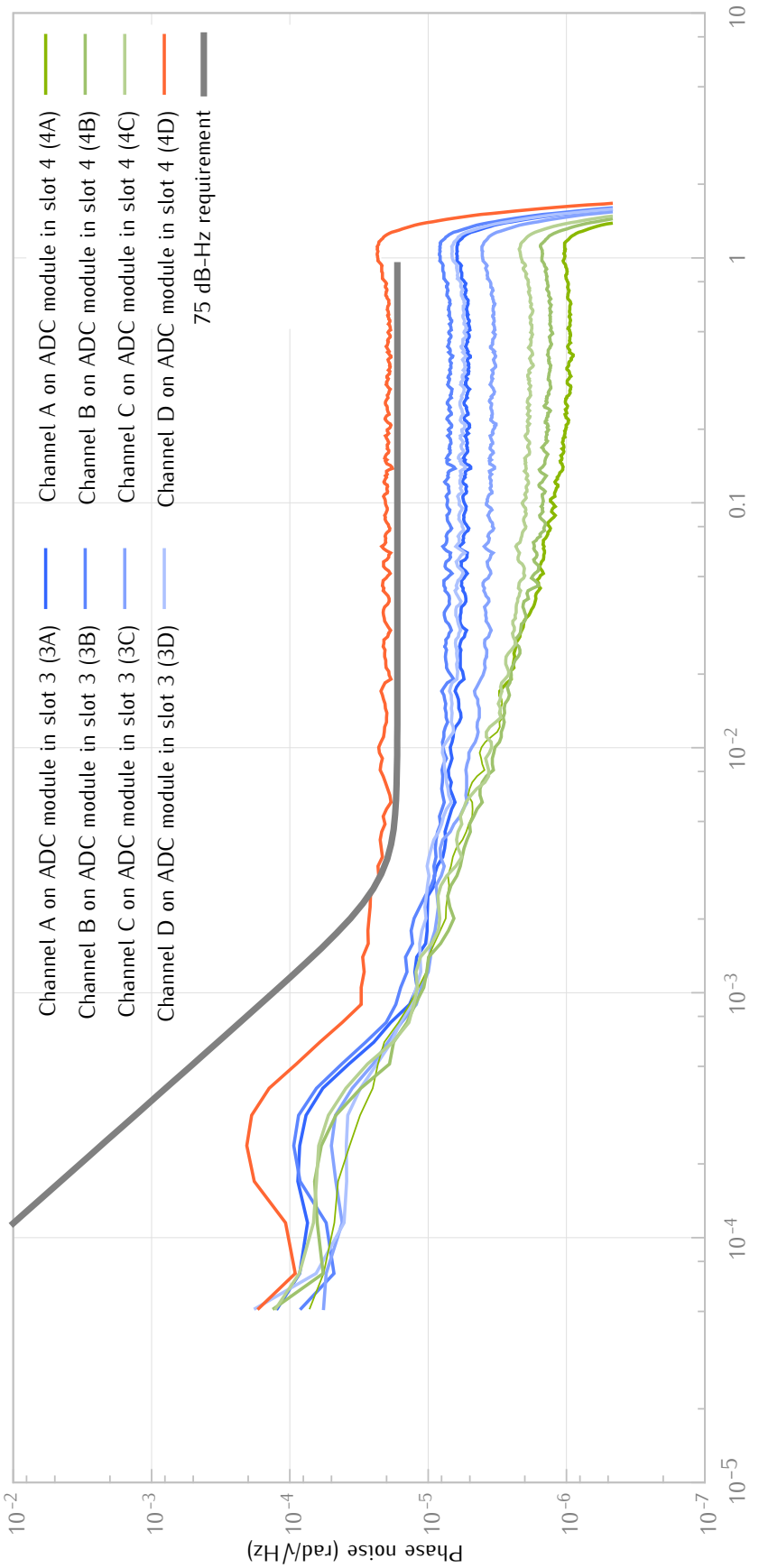


Figure 7.10: Final performance test of the full LISA Metrology System. Differential phase noise between the carrier channels (25 MHz) on two ADC modules after 75 MHz pilot tone correction. The signal contains laser frequency noise, PRN modulations, clock tone side bands and it has an SNR of 75 dB Hz. To monitor a coupling mechanism in the analogue components for one channel (4D, channel D on the ADC module in slot 4) the impedance matching was intentionallly left uncorrected which allowed for a better monitoring the observed white noise level throughout the measurement campaign. All other channels with proper impedance matching performed well within the required phase stability.

8 CONCLUSION

The metrology system ("phase meter") developed in this project fulfills all the stringent requirements for LISA and its derived concepts eLISA and NGO. This includes not only carrier phase measurement at the µcycle level of a drifting MHz signal with poor SNR, but also all auxiliary functions needed to implement the LISA interferometry such as clock syncronization, absolute ranging, data transfer and beat note acquisition.

Other interspacecraft laser interferometry missions might also profit from this development. For example, a GRACE Follow-On like geodesy mission with laser interferometry would have similar but much relaxed requirements on the phasemeter that would easily be fulfilled by a subset of the system developed here.

The hardware developed in this project uses components with a known path to space qualification, demonstrating the feasibility of the design. Nevertheless, considerable work will be necessary to produce real flight hardware. This concerns in particular the performance evaluation of flight model version components in the analog circuitry (AD front end and clock distribution chain), for which the relevant data is not available from manufacturers measurements, and the thermal management.

On the science side, the next logical step is to integrate the phasemeter in an optical testbed with the ultimate goal of demonstrating as far as possible on ground all the ingredients needed to implement time-delay interferometry (TDI).

This project represents a key step to provide in Europe the last missing important technology item for LISA. The authors are very grateful to ESA for funding this project and for the efficient, uncomplicated and friendly handling of this contract. ∎

Part IV

ACRONYMS & REFERENCES

ACRONYMS

AAF	Anti-Aliasing Filter
AC	Alternating Current
ADC	Analogue-to-Digital Converter
ADPLL	All Digital Phase-Locked Loop
AEI	Albert Einstein Institute in Hannover
AFE	Analogue Front-End
Axcon	Axcon ApS, Denmark
BER	Bit Error Rate
BNA	Beat Note Acquisition
BPSK	Binary Phase Shift Keying
CIC	Cascaded Integrator Comb (filter)
CI	Control Interface
CPU	Central Processing Unit
DAC	Digital-to-Analogue Converter
DC	Direct Current
DFACS	Drag-Free and Attitude Control System
DFT	Discrete Fourier Transform
DLL	Delay-Locked Loop
DPLL	Digital Phase-Locked Loop
DSP	Digital Signal Processing
DSS	Digital Signal Simulator
DTU	Danish Technical University
DWS	Differential Wavefront Sensing
EBB	Elegant Breadboard
EOM	Electro-Optical Modulator
ESA	European Space Agency

FDS Frequency Distribution System

FFT Fast Fourier Transform

FIFO First-In-First-Out Memory

FIR Finite Impulse Response (filter)

FPGA Field Programmable Gate Array

FSM Finite State Machine

GRACE Gravity Recovery and Climate Experiment

GSE Ground Support Equipment

GW Gravitational Wave

HDL Hardware Description Language

IAD Integrate-And-Dump

IF Interface

IFO Interferometer

IIR Infinite Impulse Response

IP Internet Protocol

IQ In-phase and Quadrature phase

LISA Laser Interferometer Space Antenna

LMS LISA Metrology System

LO Local Oscillator

LUT Look-Up Table

MUX Multiplexer

NCO Numerically Controlled Oscillator

NGO New Gravitational Wave Observatory

NPRO Non-Planar Ring Oscillator

OpAmp Operational Amplifier

PA Phase Accumulator

PCB Printed Circuit Board

PC Personal Computer

PD Photo Diode

PID Proportional-Integral-Differential (controller)

PIR Phase Increment Register

PI Proportional-Integral (controller)

PLL Phase-Locked Loop

PMS Phase Measurement System

PND Power-to-Noise Density

PRN Pseudo-Random Noise

PR Photo Receiver

PSD Power Spectral Density

PT Pilot Tone

QPD Quadrant Photo Diode

RMS Root Mean Square

RTEMS Real-Time Executive for Multiprocessor Systems

S/C Spacecraft

SSB Single Side Band

SA Spectrum analyser

SG Signal Generator

SMA SubMiniature version A connector

SNR Signal-to-Noise Ratio

TCP Transmission Control Protocol

TDI Time Delay Interferometry

TIA Trans-Impedance Amplifier

TS Temperature Sensor

USB Universal Serial Bus

USO Ultra Stable Oscillator

VHDL Very High Speed Integrated Circuit Hardware Description Language

XOR Exclusive-Or

eLISA evolving Laser Interferometer Space Antenna

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Documents by the LISA Metrology System Team. Availability can be inquired through ESA/ESTEC, Contract No. AO/1-6238/10/NL/HB.

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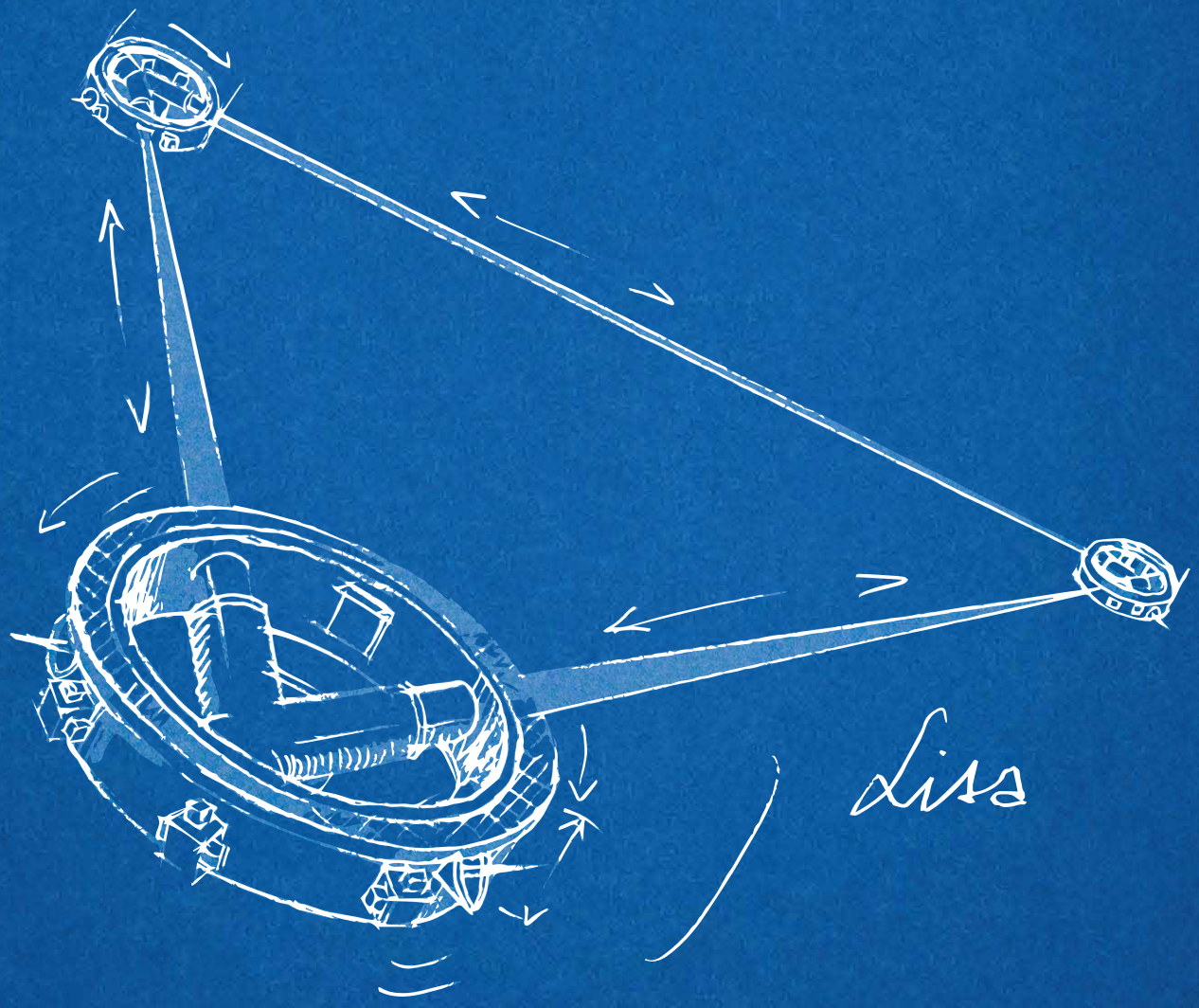

www.estec.esa.int