Report on the Low-RF-Power and Data-Acquisition-Systems of the 2.45 GHz Lower-Hybrid Transmitter at the ASDEX Tokamak

by

Michael Zouhar and Francesco Monaco
(Lower-Hybrid Group)

IPP 4/238 März 1989

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Die nachstehende Arbeit wurde im Rahmen des Vertrages zwischen dem Max-Planck-Institut für Plasmaphysik und der Europäischen Atomgemeinschaft über die Zusammenarbeit auf dem Gebiete der Plasmaphysik durchgeführt.

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Abstract:

This report relates to the low-power section of the 2.45 GHz transmitter used for current drive experiments at the ASDEX tokamak. The high-RF-power section is dealt with elsewhere. Data acquisition and evaluation of quantities pertaining to the Lower Hybrid experiment are also treated here. As in the previous report on the 1.3 GHz system (M.Zouhar: "Beschreibung des Niederleistungsteils des HF-Systems fuer die LH-Experimente in ASDEX.", IPP-report 4/218, February 1984), most space is spent in commenting upon the amplitude (power)- and phase- feedback control loops.

Acknowledgement.

The author feels indebted to Mr.M.J.Muenich for valuable discussions concerning the interface to the high-power section of the LH-plant and the design of the phase monitors.

The author thanks the members of the ASDEX data acquisition group, especially Dr.N.Ruhs, Mr.M.Harnau, Mr.A.Kus and Mr.H.Bauer, who provided both the hardware and software requested by the Lower Hybrid Group.

Objective of this work.

The Lower Hybrid Experiment at the ASDEX Tokamak aims at current drive by microwaves at 2.45 GHz, the frequency chosen on the basis of the underlying physics and the availability of high power microwave equipment.

The Lower Hybrid Transmitter uses a special waveguide antenna ("grill") consisting of 48 (2 arrays of 24) waveguides stacked together to couple up to 2.4 MW of RF-power to the plasma. The transmitter comprises 6 klystron amplifiers, each feeding eight waveguides of the antenna. The antenna requires correct phasing between adjacent waveguides in order to achieve successful coupling. This phasing is attainable by:

>>> controlling the klystron output phases (closed loop control)

>>> setting the high power phase shifters in each of the 48 waveguides (open loop control)

Amplitude feedback control loops (A-loops) are used to control the six output power levels of the klystrons.

The data acquisition system gathers the pertaining data:

>>> klystron output power data (throughout the LH-pulse)

>>> both the incident and the reflected power data of the antenna (48 incident, 48 reflected, throughout the pulse)

>>> klystron output phase data (time multiplex during the pulse, 40 to 320 ms per displayed phase)

››› the antenna incident wave phase data (all 48 waveguides, time multiplex of 24 or 48 phases chosen by the triggering equipment, 5 to 40 ms per displayed phase).

This report informs about how this objective was achieved.

List of Symbols and Abbreviations.

A_{IF}	IF-Amplitude of the Double Balanced Mixer used as phase comparator (at the former 1.3 GHz-project)
A-loop	Amplitude Feedback Control Loop
CRT	Cathode Ray Tube
CV	Control Voltage
CVA	Control Voltage applied to the Amplitude Control Element (PIN-Diode Attenuator)
CVφ	Control Voltage applied to the Phase Control Element (electronic phase shifter)
DBM	Double Balanced Mixer
H	logical "high" (5 volts)
HF	High Frequency (used here as generic term for local oscillator frequency (LO) and radio frequency (RF))
HPA	High Power Amplifier
IC	Integrated Circuit
IF	Intermediate Frequency
L	logical "low" (0 Volts)
LH	Lower Hybrid
LO	Local Oscillator (frequency)
PLL	Phase Locked Loop
RF	Radio Frequency
SW	Square Wave
U_{DBM}	Output Voltage at the IF-port of the Double Balanced Mixer
φ_i	incident phase (=phase of the incident wave)
φ_r	reflected phase

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1. Introduction.

The task that was solved here, resembled the former 1.3 GHz project. Therefore the list of specifications is similar (**Fig. 1**). However, there are some differences in the technical layout:

>>>>> the antenna consists of 48 waveguides

>>>>> each of the six klystron amplifiers feeds a group of 8 waveguides of the antenna

>>>>> the antenna consists of two floors (24 waveguides each, designated as "upper grill" and "lower grill"), the phasings of which can be set individually and changed with respect to each other (e.g. 75° at upper, 120° at lower, any phase offset between upper and lower)

>>>>> the floors of the antenna are independent (i.e. they may or may not be triggered coincidentally, may have different power settings and different phasings)

>>>>> there are twelve feedback control loops (six by six for amplitude and phase)

>>>>> the phase feedback control loops use the heterodyne principle with IF = 1 MHz

>>>>> as there are so many channels in the antenna, a phase monitoring facility was devised to display the phases in succession and repeatedly during the LH-Pulse (time multiplex employing multiple-input PIN-Diode microwave switches)

2. Master Oscillator.

The master oscillator unit comprises two independent oscillators at 2450 MHz and 2451 MHz. The latter provides LO-power for the mixers of the heterodyne system of the phase control loops. Bandpass filters provide 50 dB suppression of spurious frequencies.

Besides feeding (through pre-amplifiers) the klystron inputs, the 2450 MHz oscillator supplies the phase references for the quadrature mixers of the phase monitors (at 2450 MHz) and the phase feedback control loops (at 1 MHz, using the heterodyne system).

3. RF-Pulse-Shaping and Power Division.

Single Pole Single Throw (SPST) PIN-Diode Switches are used to turn on and off the RF-Power (**Fig.2**). A two-way power divider before the switches enables independent operation of the antenna floors (each floor comprises 24 waveguides); this is accomplished by triggering each of the PIN-Diode Switches by different trigger signals. A single switch provides 55 dB attenuation, when closed.

It takes 3 µs to switch on the RF-power, 500 ns to switch off. However, the leading edge of the RF-pulse is up to 5 ms long (depending on the power level chosen) due to the response of the amplitude control loop (A-loop). In case of emergency shut

down RF-power is of course switched off in less than 10 µs due to the action of the SPST-switches (no influence of the A-loop).

Four-way power dividers are used for further power splitting. This yields eight outputs. Two outputs of these eight serve monitoring purposes.

4. Use of Circulators

Both coaxial and waveguide circulators are widely used in the system:

>>>> at the outputs of amplifiers and oscillators to prevent damage by reflected RF-power

>>>> at the outputs of power dividers and directional couplers, where limited directivity might be a problem

Since mixers are especially sensitive to mismatch and since we have ample power throughout the system, attenuators are used instead of circulators at mixer inputs.

5. Amplitude (Power) Control.

5.1 Objective.

The amplitude control ensures that the output power levels of the klystron amplifiers hold the desired values during the LH-pulse. The amplitude may be modulated, if necessary.

The settling time (true amplitude within ±5% of reference) must be chosen to enable the phase control loop to settle at the leading edge of the LH-Pulse, fairly below the maximum output power. Otherwise the system might be shut down due to improper phasing at the antenna during the rise time of the pulse (**Fig.3**: RF-Pulse).

5.2 Details of the A-Loop.

The circuit diagram is shown in **Fig.4**. A detector is used to take the true (actual) value of the amplitude (**Fig. 5**: diode characteristics). The non-linear characteristics of the detector has to be taken into consideration when designing the desired value selector (the rectified voltage increments shrink with decreasing RF-power). As our selector is linear, only two decades of power can be precisely handled (this is sufficient for our purpose).

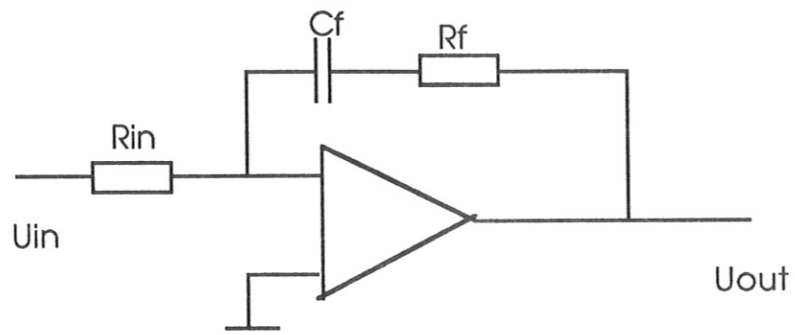
The circuit consists of the voltage comparator ("desired versus actual") and the controller having a proportional and an integral

part. Because of the latter, the rise time of the RF-pulse depends on the desired power level chosen and varies between 1 and 5 ms (The phase control loop settles 20 dB below maximum RF-power at the very latest, irrespective of the RF-level chosen (Fig.3)). The output of the amplitude control circuits drives a PIN-Diode Attenuator (55 dB dynamic range). At the beginning of the RF-pulse, the circuit starts from the maximum attenuation value.

Some more comment is necessary on the settling time of the A-loop. The proportional part of the controller (Fig.4, IC 3, R_f = 12.1 kOhms/R_{in} = 10 kOhms) has usually to be kept low to prevent the loop from self-excitation. The integral part (Fig.4, IC 3, R_{in} = 10 kOhms, C_f = 10 nF) is necessary to avoid an intolerable difference between desired and actual values in the settled loop (steady state error). This might happen with the genuine proportional controller.

Since the controller output responds to a step U_{in} as:

$$\frac{dU_{out}}{dt} = \Delta U_{in} \times \frac{1}{R_{in}C_f}$$



the settling time of the A-loop under consideration may be as short as 50 µs (response to 1 dB step (as an example) of the desired A-value at full power, 500 kW) or as long as 5 ms (leading edge of the RF-Pulse at the lowest desired A-value).

6. Phase Control.

6.1 Objective.

Correct phasing (between the adjacent waveguides) of the incident waves at the antenna is imperative for the successful coupling to the plasma. This phasing must be held constant during the shot, it must be established on the leading edge of the RF-pulse fairly below the maximum power to prevent the protection circuits from shutting down the whole system due to mismatch at the antenna-plasma boundary. This implies that the PLL has to be fairly fast and must have sufficient dynamic range (in terms of RF-power). Furthermore there is the need of coping with any input phase at the phase comparator. Irrespective of the initial (before the RF-pulse) state of the PLL, the action of the circuit must restore any desired output phase (at the antenna). The circuit must avoid persevering of the manipulated output (-voltage) driving the control element (electronic phase shifter) at one of the edges of the control voltage (CV-) range.

6.2 General Comments.

The task encountered both in the 1.3 GHz- and 2.45 GHz-systems is slightly different from the phase locked loop (PLL) met in communication systems. There a voltage controlled oscillator has to be pulled from its current frequency to the reference frequency, using an appropriate PLL-circuit. In our case the frequencies of all the outputs of the six klystron amplifiers are the same from the onset of the RF-pulse. The output phases, i.e. the electrical lengths at each particular output have to be controlled using PLLs.

The design of the controller itself is straightforward. Ordinary operational amplifiers serve the purpose. The real difficulties come up elsewhere:

- >>>> at the phase comparator that should be able of handling all combinations of actual and references phases together with at least 20 dB dynamic range at the actual-phase input (RF-input)
- >>>> in the correct response of the circuit when one of the edges of the CV-range of the phase control element (electronic phase shifter) is reached
- >>>> nonlinearity of the electronic phase shifter
- >>>> accuracy of the phases (both actual and reference)

In the former 1.3 GHz system a double balanced mixer (DBM) was used as a phase comparator at 1.3 GHz (i.e. the compared signals were not downconverted). The output of this mixer is nonlinear

with respect to both RF-input power and the phase difference between the RF- and LO-inputs. If RF-power is held constant then:

$$U_{DBM} = A_{IF} \times \sin(\Delta\varphi)$$

where A_{IF} is the amplitude of the sinusoidal DBM-output. If φ is held constant the output varies much like the output of a diode detector (Fig.5), i.e. A_{IF} = f(RF-power). As (sin φ) changes sign, only a range of 180° is usable in the loop (negative feedback turns into positive one within the other 180°). In the 1.3 GHz system this problem was circumvented by presetting the control voltage to phase shifter in absence of RF-power (as a result the operation of the LH-system was limited to several discrete ranges of klystron collector voltages, 360° apart from each other, this fact being somewhat irksome). Now, since the operating frequency is higher (2.45 GHz) and as the DBM was rather sensitive to mismatch at 1.3 GHz (this was annoying especially at low RF-power levels, where the deviation from the desired phase could hardly be identified), a different approach was chosen. The 2.45 GHz system employs the heterodyne principle (IF = 1 MHz), i.e. both the actual phase values and the reference phases are downconverted to 1 MHz.

6.3 Details of the Phase-Loop.

The circuit diagram of the PLL is shown in **Fig.6**. The phase comparator itself comprises two digital integrated circuits (IC 13

in the circuit diagram). It requires square wave signals to operate properly. There are two 1 MHz sine waves carrying the actual and reference phase information initially available at the outputs of the downconverters at 2450 MHz. These sine waves are transformed into square waves (SWs) by chains of limiting amplifiers (IC 1 through IC 6 and IC 7 through IC 10). These chains were designed in such a manner as to enable the phase comparator to operate at constant levels. Therefore the loop is independent of the power level at the RF-port of the actual-phase downconverter. The annoying problem of mismatch at the HF-ports of the downconverter is accordingly surmounted (the mismatch still exists, but it does not spoil the IF-amplitude).

The controller consists of four operational amplifiers (IC 15 through IC 18). The settling time of the loop is determined by the circuit arrangement at IC 17.

The remaining part of the diagram contains the circuitry required for preventing the loop from persevering at one of the edges of the CV- range (0 to 30 V) of the electronic phase shifter ("hooking up"). If this voltage (CVφ) reaches 29.5 Volts (as an example) during the settling process of the loop, the circuitry forces the output to jump by 29 Volts (this corresponds to slightly more than 360°) as quickly as possible and continue the settling process until the desired phase is reached (CVφ = 4 V, as an example, instead of 33 V not permitted by the CVφ-Range).

The loop usually settles in 50 µs to within 5% of the desired value. If there is a 29 V-jump of the control voltage CVφ, the

settling time extends up to 200 µs. The settling time is nearly independent of the RF-power level (due to the action of the limiting amplifiers). However, it depends slightly on the desired phase value chosen, due to the nonlinear characteristics (**Fig.7**) of the electronic phase shifter used (This implies that the loop gain depends on the CV applied to the phase shifter). The range of usable RF-power levels exceeds distinctly 20 dB (the value specified). The ratio of maximum RF-power at the downconverter to the constant LO-power is kept below 1:10 to prevent distortion of the actual phase value (in the loop that has settled) at high RF-Power levels.

The response of both the A-loop and the PLL is depicted in **Figs.8** and **8a**. This is a laboratory test result with the square-wave phase-modulated input signal. Settling events of the PLL are shown while the amplitude is rising (leading edge of the RF-pulse). The response of the loops is monitored by means of a quadrature mixer. This device provides two outputs (y-component = A x (cos φ), x-component = A x (sin φ), φ being related to an arbitrary phase reference). The result is shown in Figs.8, 8a as polar plot (top) and as a function of time (bottom). Both figures differ in the loop gain within the PLL (the response in Fig.8a is clearly faster).

7. Phase Monitors. Accuracy of Phase Measurements.

7.1 Necessity of Phase Monitoring.

As the antenna phasing was of utmost importance, we felt that phase monitoring should be done. The LH-System comprises two phase monitors (see Fig.2) for the klystron output phases (φ1 through φ6) and "grill"-phases (φ1 through φ48), incident phases only. As there are so many phases to be displayed, monitoring all of them throughout the LH-Pulse would have required a rather expensive equipment. To cut down on the cost, a time multiplex system was devised to display the phases one after another and repeatedly during the pulse. The time (between 5 and 40 ms) devoted to one separate phase is determined by the triggering equipment. This is true for both monitors. The phases are displayed by digital storage oscilloscopes. A X-Y-(polar) display is used, so that a single *controlled* phase yields a point. Switching between X-Y-display and Y-T-, X-T-display of the stored data is possible. Most of the chosen phasings lead to characterisic patterns on the CRT-screen. As the attenuation values in the individual channels of the phase monitor vary, the phase patterns are expected to consist of various numbers of clusters of points (in case of 60°-, 90°-, 120°-, 180°-phasings) or they come up as sequences of points distributed evenly along a circle centered at the origin of the polar coordinate system (in case of 75°-, 105°-phasings, as an example). In practice this distribution is not perfectly even, both in phase and amplitude (s. section 7.3). Some examples are shown in **Figs.15** and **16.**

7.2 Phase Reference-Planes.

Several "phase reference planes" were established within the LH-System. "Phase reference" used here is not to be confused with "reference phase" of the PLL. Obviously the phasing at the grill mouth is not accessible to measurement, once that the antenna is immersed into the tokamak vessel. Therefore a reference plane had to be created near the antenna in such a manner that the phasing (accessible to measurement and control) at this plane was the same as at the grill mouth with the exception of a phase offset common to all the incident waves. "Grill measurement couplers" (Fig.2) were employed and the phase reference plane was established at the outputs of these couplers by feeding an appropriate power into the high-power power-divider and measuring the phases at the input to the straight waveguide section of the grill *and* at the phase reference plane. This procedure was repeated for all individual channels of the grill. Phase correspondence was restored by inserting coaxial lines, wherever necessary. This measurement was performed in the laboratory. The antenna was moved to ASDEX later.

A similar reference plane was installed at the "klystron measurement couplers." As both coupler systems were separated by 30 meters of coaxial line from the cabinets containing the monitoring and phase control equipment, additional phase reference planes were established:

>>>> at the RF-inputs to the quadrature mixers

>>>> at the RF-inputs to the downconverters (both actual and reference phases for the PLL)

7.3 Accuracy of Phase Measurement.

Since installing reference planes requires connecting coaxial lines in series, the overall accuracy of the phase measurement deteriorates with the number of lines connected this way. The task is made easier by the fact that no absolute phase measurement is necessary. The reference oscillator (-phase) is required to be stable, but otherwise may be arbitrary. The "phasing" at the antenna only refers to relative phases between adjacent waveguides. The wavelengths encountered here are:

>>>> 122.45 mm in free space

>>>> 147.82 mm in WR 430 waveguide

>>>> 161.24 mm in WR 340 waveguide

>>>> 84.50 mm in teflon-filled coaxial line

Obviously, 1° corresponds to 0.23 mm in coaxial line. Since cable connectors usually cannot be mounted precisely enough on semi-rigid cable (mostly installed), let alone the procedure of cutting the cable to the length required, precise mechanical phase shifters were used at all phase reference planes for the final phase adjustment.

It was already mentioned that no absolute phase measurement was necessary. If only the relative phasing matters, the following procedure can be used to determine the accuracy: φ_1 through φ_n be a set of n phases (e.g. n coaxial lines) to be

trimmed to the desired phase φ_d (desired electric length). If all these phases are compared with the same reference phase (of the reference oscillator) then an average φ_{avg} can be calculated, with the particular phases φ_i distributed around it. The thoroughness of the adjustment determines the difference $(\varphi_{avg} - \varphi_d)$, while the standard distribution σ of the φ_i- data taken does not fall short of the value predestined by the equipment used. The following σ-values were attained in the 2.45 GHz system:

a) 3° for a typical (φ_i)- measurement (adjustment of a set of coaxial lines)
b) 6° for two coaxial lines sets in series
c) 9° for the resulting phasing at the grill mouth, taking into consideration the resetability and stability specifications of the PLL (Fig.1).

These estimates are fairly conservative. Better results were achieved in practice (6° for the resulting phasing). This was inferred from the output of the grill phase monitor. Digital oscilloscopes with 12 bit vertical and horizontal resolution were used for this measurement.

8. Data Acquisition and Evaluation

Besides the phases displayed at the phase monitors the following quantities were measured and evaluated:

1) at the antenna:
   incident power (variable names H1L through H48L)
   reflected power (variable names R1L through R48L)
2) at the input to the high power divider;
   incident power (variable names K1L through K6L)

These quantities were obtained by means of diode detectors. The output voltage of each detector was converted to yield a value in kilowatts (rectified voltage - incident RF power characteristics were determined for each detector).

3) Phase data (output of quadrature mixers) were recorded as well, but the polar plots did not prove very appealing, so resort was taken to immediate output of Q-mixers displayed at the oscilloscopes.

Following quantities were calculated;

1) total incident power for upper grill (1 through 24)
   total reflected power for upper grill (1 through 24)
   total net power = incident minus reflected

A plot of these quantities as a function of time was obtained, **Fig.9** and **12**

2) the same for the lower grill (25 through 48), **Fig.10** and **12**
3) overall values (1 through 48), **Fig.13**
4) A time interval was chosen and the "power reflection factor" (= "reflected/incident") calculated for each channel i of the

antenna (i = 1 through 48) from mean values within the time interval. These reflection factors were depicted as a "snap shot" for upper and lower grill together with numeric values of Incident (LH-Inc.), Reflected (LH-Refl.) and Net (LH-Net.) powers (**Fig.14**).

Raw data were written into ASDEX-shot file. This shot file was completed 4 minutes after the shot. The conversion "millivolts to kilowatts" took at least 10 minutes. Therefore the kilowatt-data were available with a delay of 20 minutes. As a consequence the plots were of no use for immediate decisions on the parameters of the next LH-shot. These decisions were made on the basis of data displayed on oscilloscopes. To emphasize: in spite of the data acquisition we had 20 (!) oscilloscopes in our LH-plant for continuous monitoring.

The data acquisition hardware collected more than 500 kBytes per LH-shot. 112 variables were recorded at a rate of 1000 samples/second, at 12 bit resolution and -5 to 5 Volts full scale range. Two stop watches were provided to record the timing signals for the antenna floors.

Appendix 1: Some Details of the A-Loop Circuit

The amplitude control circuit (Fig.4) operates as follows:

>>>> if there is no trigger pulse present at the "HF-time U(L)", (U = upper, L = lower (grill)), the output 6 of IC 2 is essentially at 0 V. This potential is set precisely at -50 mV by means of the offset potentiometer at input 2 of IC 2. Hence the output of IC 3 is forced to take the value of approximately 9.5 V. The PIN-Diode attenuator at CVA-output assumes its maximum attenuation (55 dB).

>>>> if the trigger is applied to "HF-time U(L)", the CVA output assumes approximately 6 V within several µs. This results in a klystron output power level that can be handled by the PLL. Then the A-loop starts the settling process (leading RF-pulse edge = 1 ms). The PLL settles within 50 µs .

>>>> if RF-power has to be shut down due to excessive reflection, the whole grill floor (upper or lower), where the reflection occurred, is shut down (not just one klystron), by setting "HF-time" = 0 Volts by the protection circuitry ("HF-time" is applied to one of the SPST PIN-Diode Switches in Fig.2). As a consequence, CVA leaps to 9.5 V again and the PIN-Diode attenuator is reset to its maximum attenuation state. The next RF-pulse may then follow.

>>>> the desired value selector (DG-C-10K-3D-0P) may store as many as 8 desired A-values per klystron. The desired values are connected via analogue switches (IC 5, IC 6) and a unity gain buffer (IC 4) to the input 3 of IC 2 ("desired - actual" value comparator). The analogue switches are triggered by the combined action of IC 8 (data selector: manual selection or timer) and IC 7 (4 bit BCD to 1-of-10 active high decoder). The active output of IC 7 selects the desired amplitude value. The selection may be performed by the timer circuitry, resulting in amplitude (power) modulation. As an example, a series of power steps may be realized this way and applied repeatedly during the LH-pulse.

Appendix 2: Some Details of the PLL Circuit

This appendix contains detailed explanations about the mode of operation of the PLL circuit. The reader should use Figures 6 and 6a when studying these explanations.

The circuit of Fig. 6 compares two 1 MHz-signals. These are sinusoidal at the inputs (far left corner of the diagram). The power level at the "1 MHz reference"- input is kept constant (at 0 dBm); however, the amplifier chain IC 7 through IC 10 is able of handling the input power range of -10 dBm to +10 dBm.

The actual-phase-signal power level varies between -20 dBm and 0 dBm at the input to the amplifier chain IC 1 through IC 6. However, the loop can handle even lower levels down to -30 dBm, as measured in the laboratory.

Both input signals are filtered by passive RC-bandpass filters (centre frequency = 1 MHz). Both amplifier chains consist of low-phase-shift limiting amplifiers (Plessey 532C). Two square waves (SW) result at the outputs of the chains (slope time about 100 ns, amplitude about 0.6 V).

The high (H)- and low (L)- levels at the inputs of IC 11 are established by superimposing these SWs onto the DC-levels of the voltage dividers at IC 11 inputs. IC 11 contains four NAND-Schmitt triggers, 2 inputs each. The resulting SWs at the IC 11-outputs have 4 ns slopes, good enough for the subsequent phase comparison.

The phase comparator consists of three positive-edge triggered data-latch flipflops (IC 12, IC 13) used together with IC 14 (containing 4 NOR gates). The mode of operation is explained in Fig.6a (using designations of Fig.6).

There is a (in general asymmetric) SW at the output of IC 14 (that may be inverted by the subsequent NOT gate, if necessary); which of the outputs is used, is determined by a soldered bridge to "1" or "4" of IC 14. The inverted output 4 is used instead of 1, when the LO in the heterodyne system is placed below the RF instead of above it. Obviously the pulse duty ratio of this SW depends linearly upon the phase lag (or phase lead) of SW1 with respect to SW2.

The following operational amplifier, IC 15, type OP27, provides for filtering and smoothing. The output 6 of IC 16 assumes a voltage between 0 V and -4.5 V with up to ±40 mV ripple. Offset voltage is superimposed onto this signal at the output 3 of IC 16. This offset is used to:

>>>> carefully balance the PLL in the settled state, i.e.:

>> case "b" in Fig.6a is chosen

>> consequently a symmetric SW results at the output of IC 14

>> approximately -2.25 V appear at the output of IC 15

>> 0 V (plus ripple) result at the output of IC 16 by appropriate choice of the offset voltage

>>>> presetting the control voltage CVφ (in absence of RF-input signal) at the output of the final stage consisting of IC 18 and transistors T1, T2. If only the 1 MHz-reference is present, a symmetric SW (500 kHz) appears at the output of IC 14, yielding (together with the offset at IC 16) the quiescent value CVφ = 15 Volts.

IC 17 performs the essential controller function. The optimal response is achieved by matching the input and feedback resistors and capacitors to the properties of the plant under consideration. The output of IC 17 assumes between -0.6 and +10 V, since only positive output CVφ is required for the phase shifter. IC 18, together with the final stage T1-T2 provides the full range of control voltages CVφ = 0 V through 30 V.

This part of the circuitry, treated so far, is sufficient for the normal operation of the PLL. As soon as the RF-pulse starts, the

loop begins settling (CVφ rises, as an example). If there is no settling point between 15 V (quiescent point) and 30 V (maximum CVφ specified by the manufacturer), the remaining part of the circuitry must take over and force the controller to find the settling point between 0 V and 15 V (both settling points differ by 360°).

At first the reader should direct his attention to IC 20 comprising four fast (1.3 µs response time) comparators. Two of them (the pair at the right) are devised to sense, whether CVφ exceeds 29.5 V(upper limit) or falls short of 0.25 V (lower limit). Then a logical high (H) appears at either input 6 or input 1 of IC 23. As input 12 of IC 23 is usually H (exceptions are described below) and input 13 is H due to "HF-Time"-signal present, when RF-power is on:

>> inputs 2 and 5/IC 23 take on H

>> H appears either at output 3 or at output 4 of IC 23

>> one of the positive-edge triggered flipflops CD4013 in IC 21 is triggered (output 1 or 13 takes on H)

>> analogue switch SW7510 (IC 19) is actuated (either 15 and 16 or 13 and 14 are connected through)

>> an auxiliary voltage (positive or negative) appears at the input 3 of IC 17 forcing CVφ to seek the new settling point by a 360°-jump (CVφ jumps by 360° in 25 µs, upwards or downwards).

During the 360°-jump, CVφ passes through the settling point somewhere. In that very moment output voltage of IC 16 passes through zero and the seeking process has to be stopped.

As soon as |Uout, IC 16| ≤ 50 mV, the other pair of comparators in IC 20 become active and a short pulse (discharge through 1 nF/10 kOhms, positive pulse only) appears at the input 14 of IC 24:

>> output 5 of IC 24 takes on logical L

>> output 10 of IC 23 takes on L

>> output 10 of IC 22 takes on H

>> both flipflops in IC 21 are reset (both Q outputs take L and disconnect the actuated output of IC 19, i.e. auxiliary voltage is disconnected)

>> both $\overline{Q}$ outputs take H

>> output 3 of IC 22 takes on L

>> output 4 of IC 24 takes on H

>> IC 19 becomes active, the auxiliary voltage still present at the input 3 of IC 17 discharges through 1kOhm/47nF (at 3 of IC 17) and 226 Ohm at 11 of IC 19.

Two additional protective measures were implemented:

>> if, by accident, both flipflops in IC 21 are set simultaneously, they would be reset via IC 22/output 11, IC 23/output 10 and IC 22/output 10

>> usually the settling process is finished within 50 µs. If this does not happen, an "emergency brake" - IC 24/ output 2 enables the circuit to have a next try:

>> output 3 of IC 22 takes on logical H, if at least one of the $\overline{Q}$-outputs of IC 21 takes on L; then:

>> output 2 of IC 24 takes on L for a short time (time constant at the input by 10 kOhm/10 nF: 100 µs)

>> output 10 of IC 22 takes on H

>> both flipflops of IC 21 are reset

In conclusion one can state that the circuit under consideration is rather delicate. The principal settling constant is determined by the circuitry at the input 2/IC 17. The other time constants (at input 3 of IC 17, output 2 of IC 20, input 3 of IC 24) must be painstakingly matched to the principal time constant and with respect to each other. In spite of this apparent difficulty, the circuit worked satisfactorily at ASDEX.

Fig.1: List of Specifications (page 1)

Frequencies:	2450 MHz (principal) 2451 MHz (auxiliary) 1 MHz (intermediate frequency)
Frequency Stability:	10^{-6}
Available Power (klystron outputs)	6 x 500 kW
Maximum Pulse Length:	1 s 2 s if the floors of the antenna are not triggered coincidentally
Dynamic Range of the Amplitude Control Loop:	>20 dB
Dynamic Range of the Phase Control Loop in Terms of RF-Power:	>20 dB
Range of Desired Values of the Phase Control Loop:	360° (i.e. arbitrary output phases)
Range of Initial (Input) Phase Values to be Coped with by the Phase Control Loop:	360° (i.e. arbitrary input phases)
RF-Pulse Rise Time:	1 ms min. 5 ms max.
Settling Time of the A-Loop (to within ±5% of reference):	50 µs min. 5 ms max.
Settling Time of the PLL (to within 5% of reference in terms of control voltage):	50 µs min. 200 µs max.
Settling Level (in Terms of RF-Power) of the PLL at the Leading Edge of the RF-Pulse:	20 dB below any maximum RF-power value chosen, at the very latest

Fig.1(page 2)

Short Term Stability of the A-Loop:	< 0.05 dB
Long Term Stability of the A-Loop:	desired value ± 0.1 dB
Short Term Stability of the Phase Control Loop:	< 0.5°
Long Term Stability of the PLL (not to be confounded with phase measurement accuracy):	desired value ± 1°
Resetability of the A-Loop:	desired value ± 0.1 dB
Resetability of the PLL:	desired value ± 1°
Amplitude Measurement Accuracy (48 Amplitudes Measured at the "Grill Measurement Couplers", Standard Deviation from the Mean Value, Evaluated by the Data Acquisition System)	± 8 %
Phase Measurement Accuracy (Standard Deviation from the Mean Value of a Set of Six Phases):	± 6°

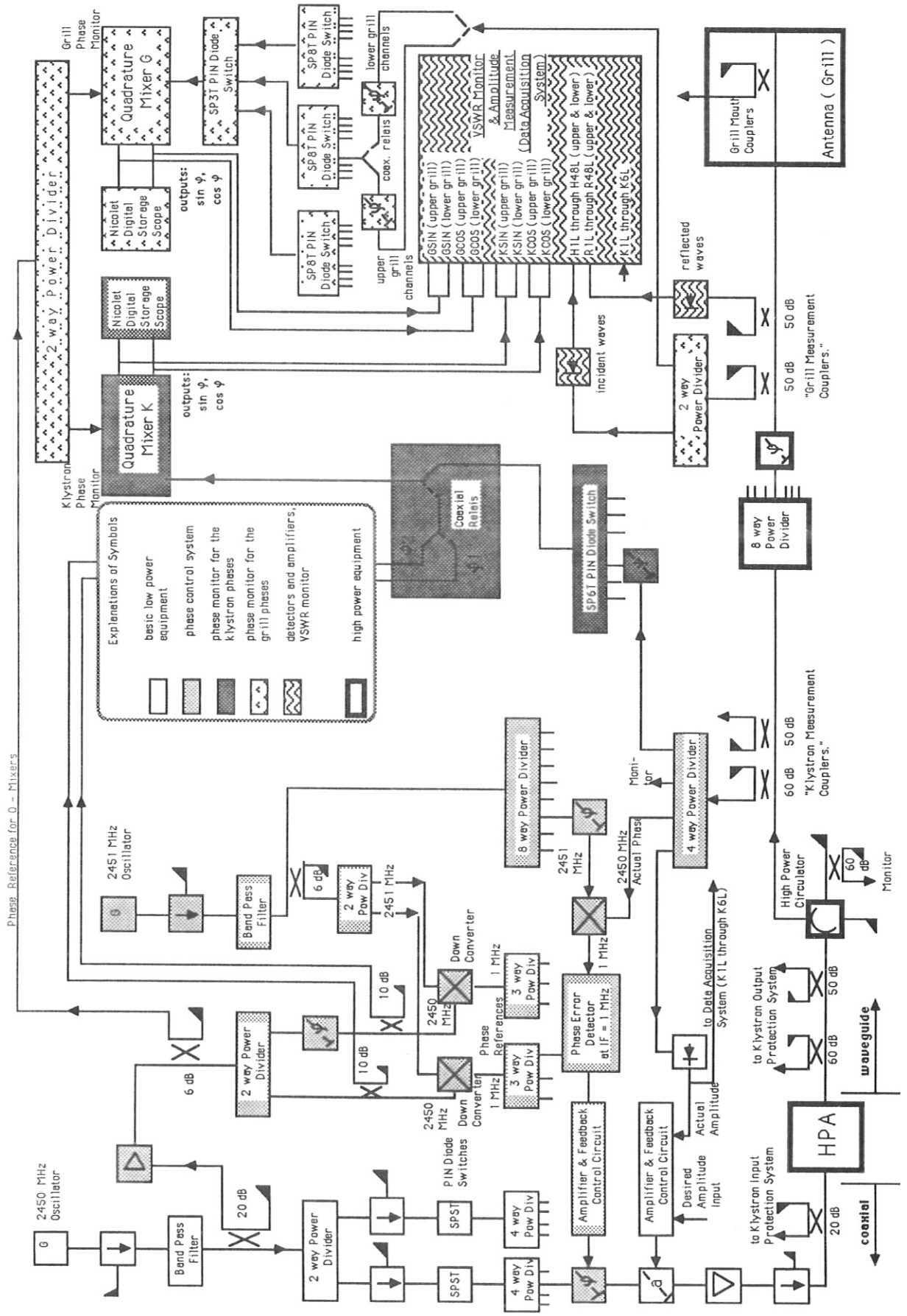
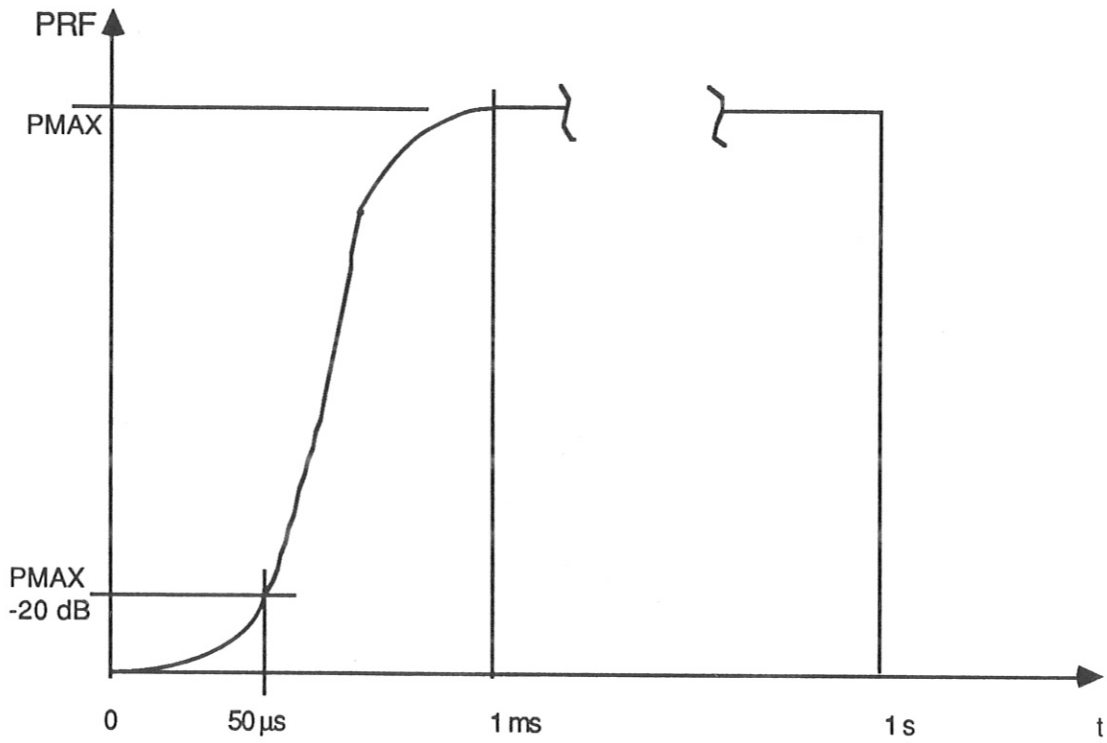


Fig. 2: 2.45 GHz RF-System (Feedback Control, Phase Monitor, Amplitude Measurement).



PRF	RF-power
PMAX	maximum value chosen
t	time
50 µs	settling time of the phase control loop
1 ms	rise time of the RF-pulse
1 s	maximum length of RF-pulse (if both floors of the antenna are triggered conincidentally)

Fig.3 RF-Pulse

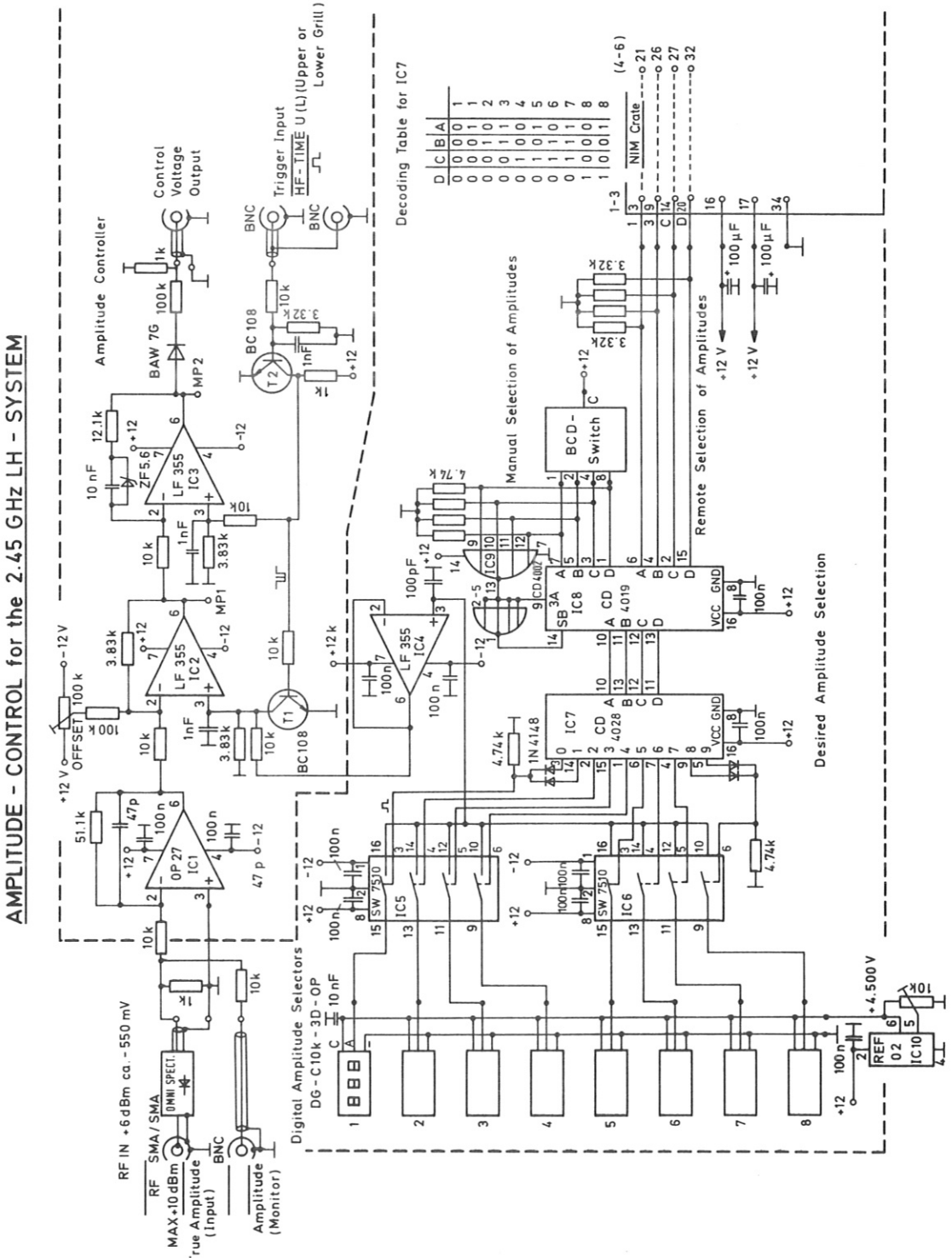
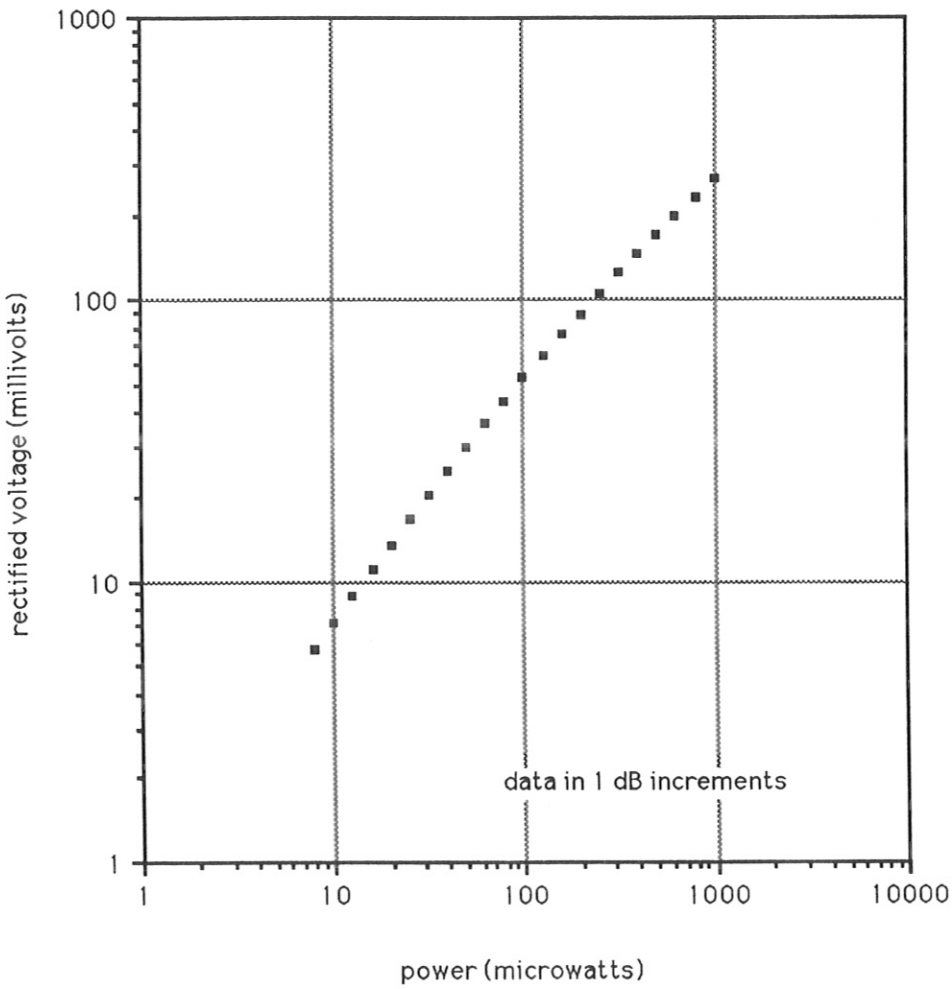


Fig.4: Amplitude Feedback Control Circuit.

Fig. 5: Diode Characteristics



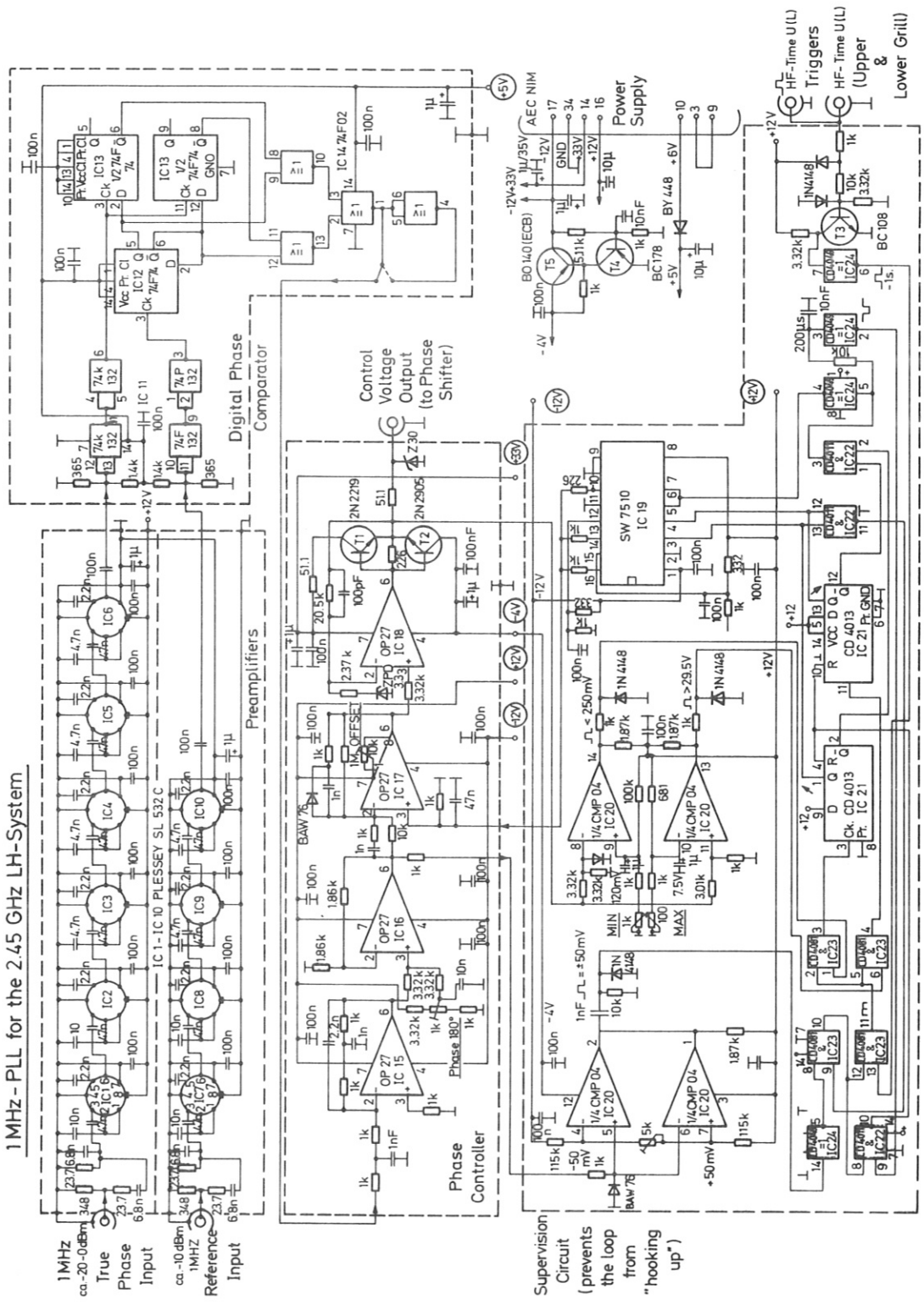
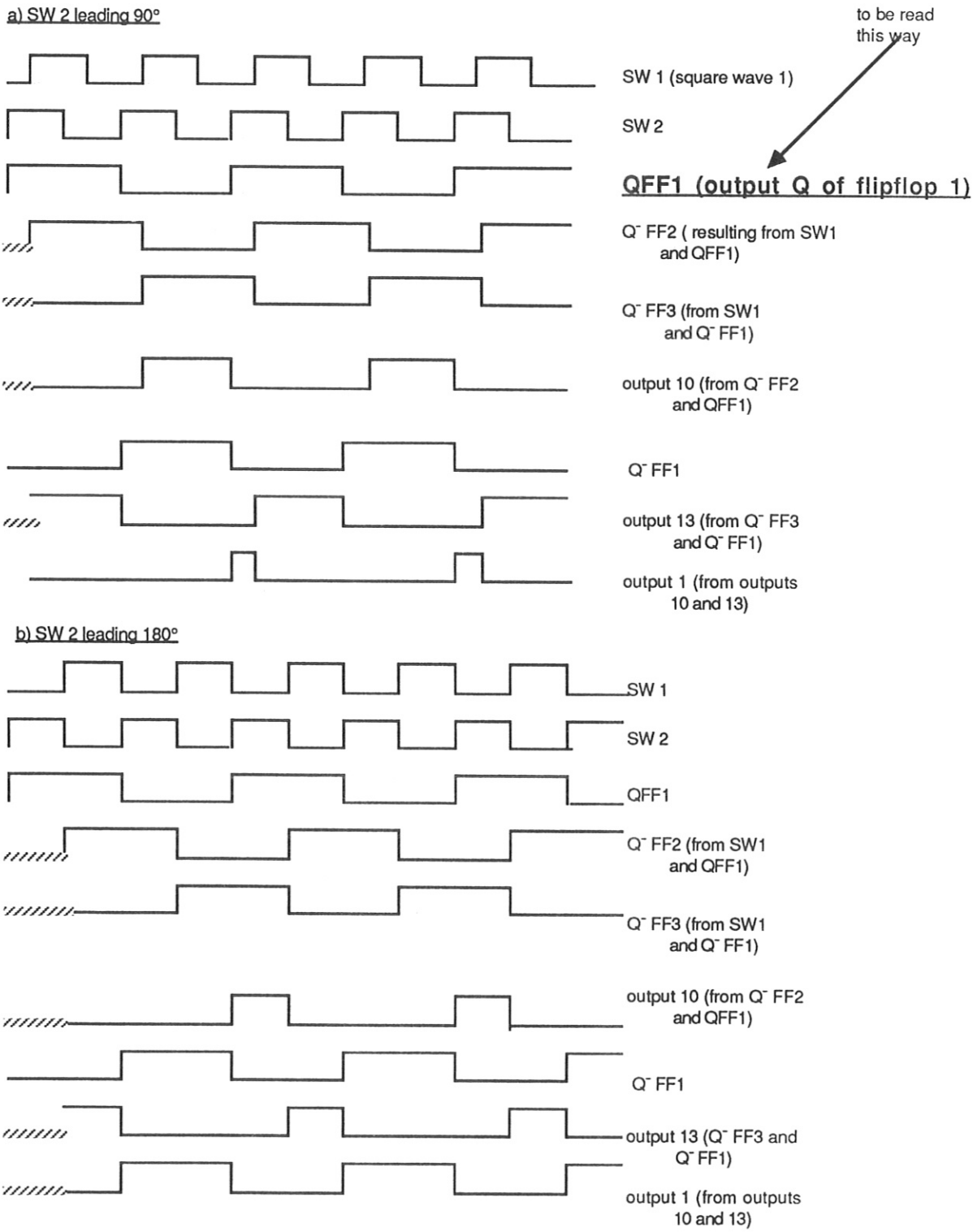


Fig.6: Phase Feedback Control Circuit.

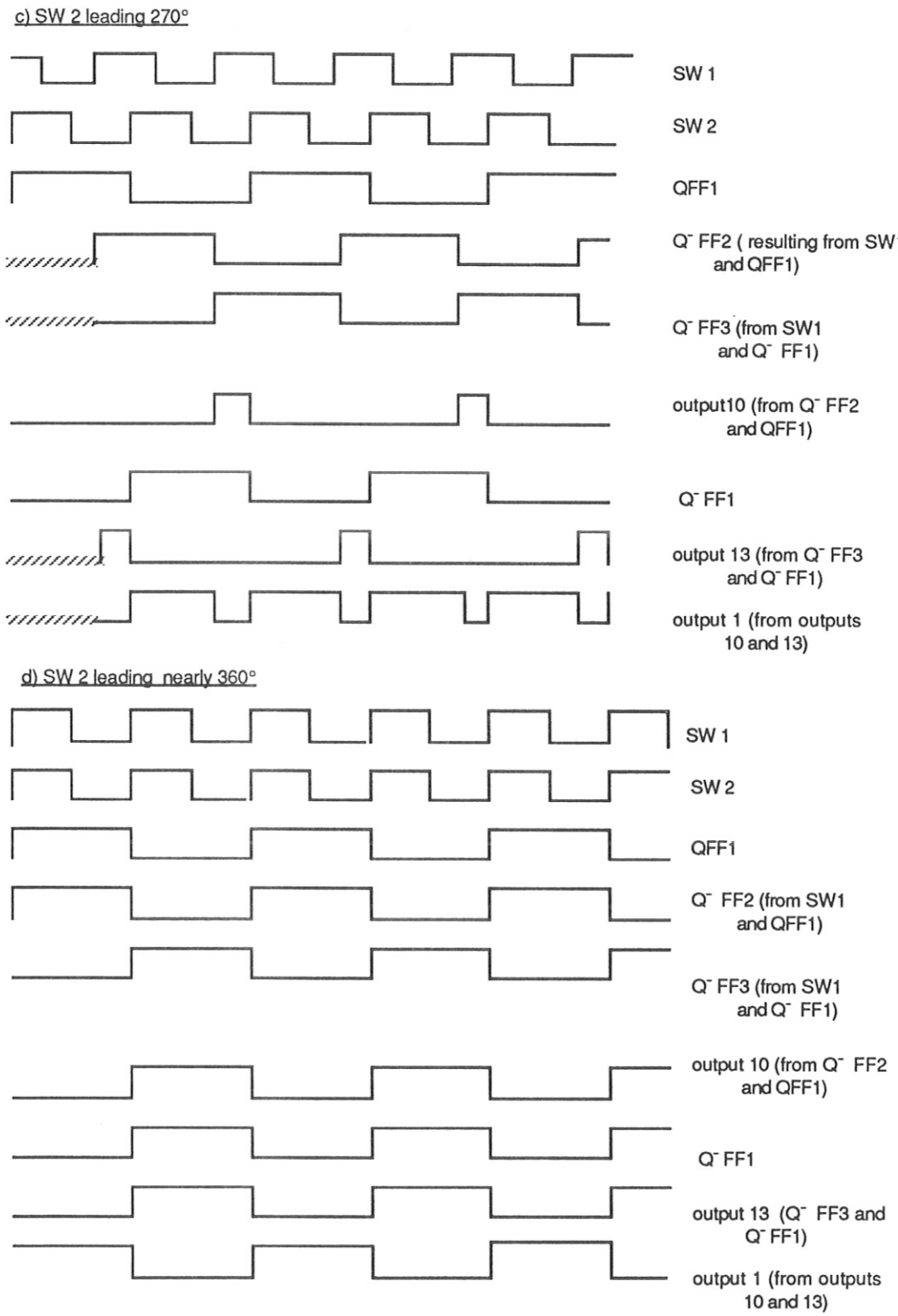
Fig. 6a: Phase Comparator's Mode of Operation (page 1).
(to be used together with Fig.7)



SW	square wave
FF	flipflop
Q,Q⁻	flipflop outputs

designates undefined output level (this takes into consideration that the signals resulting from SW1 and SW2 have to propagate through the circuit)

Fig. 6a: Phase Comparator's Mode of Operation (page 2).



SW	square wave
FF	flipflop
Q,Q⁻	flipflop outputs

//////// designates undefined output level (this takes into consideration that the signals resulting from SW1 and SW2 have to propagate through the circuit)

Fig.7: Electronic Phase Shifter Characteristics

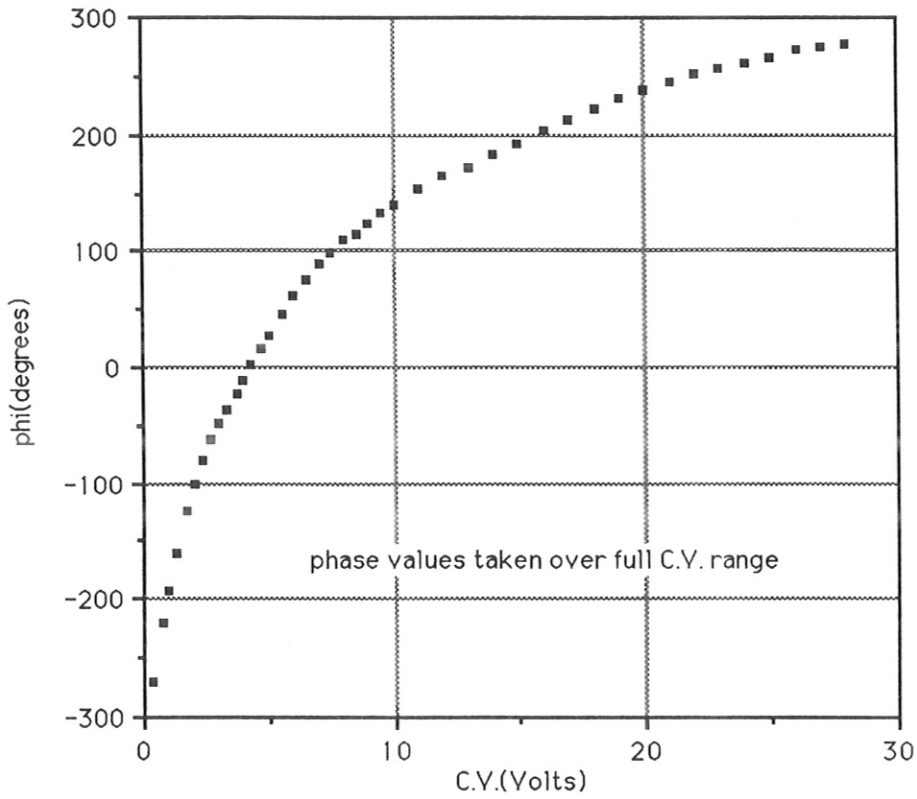
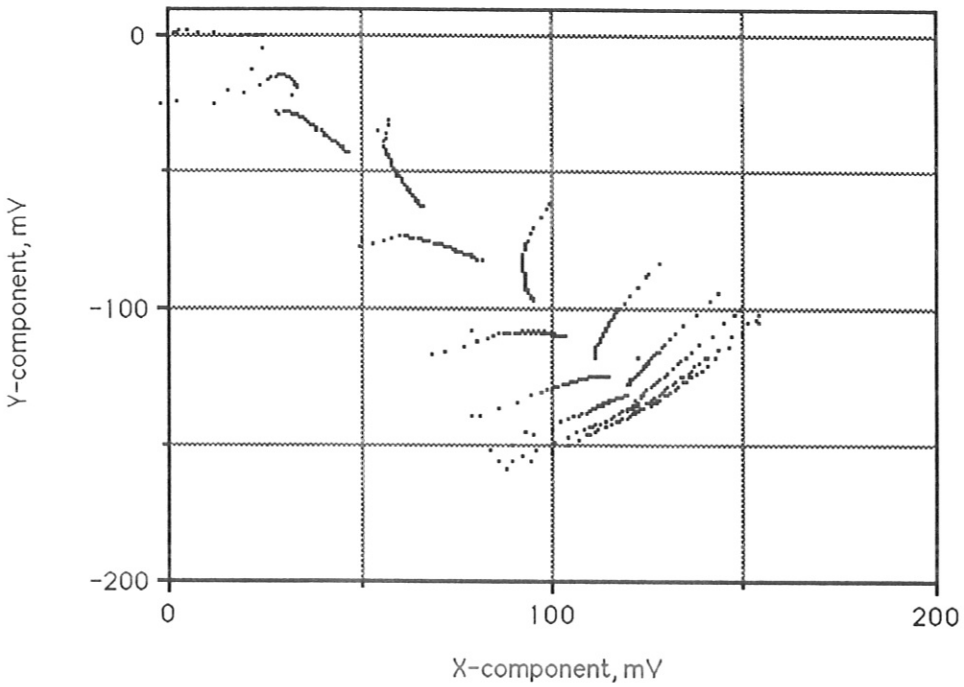


Fig. 8: Simultaneous Response of Both Loops



Polar Plot

case 1:

slow response of PLL

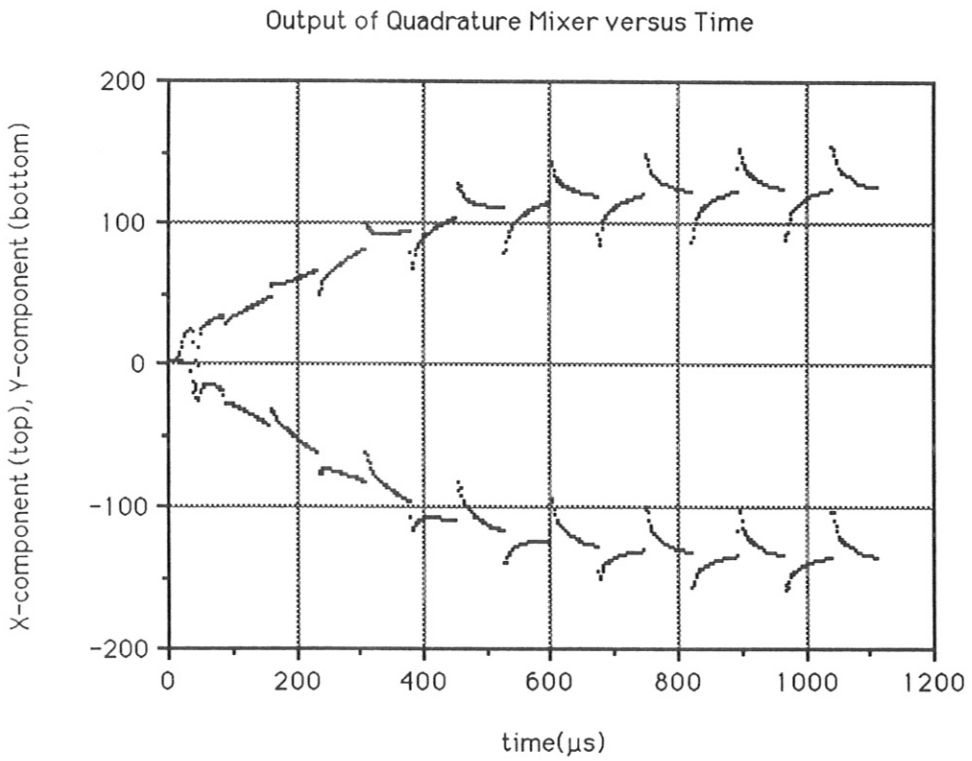
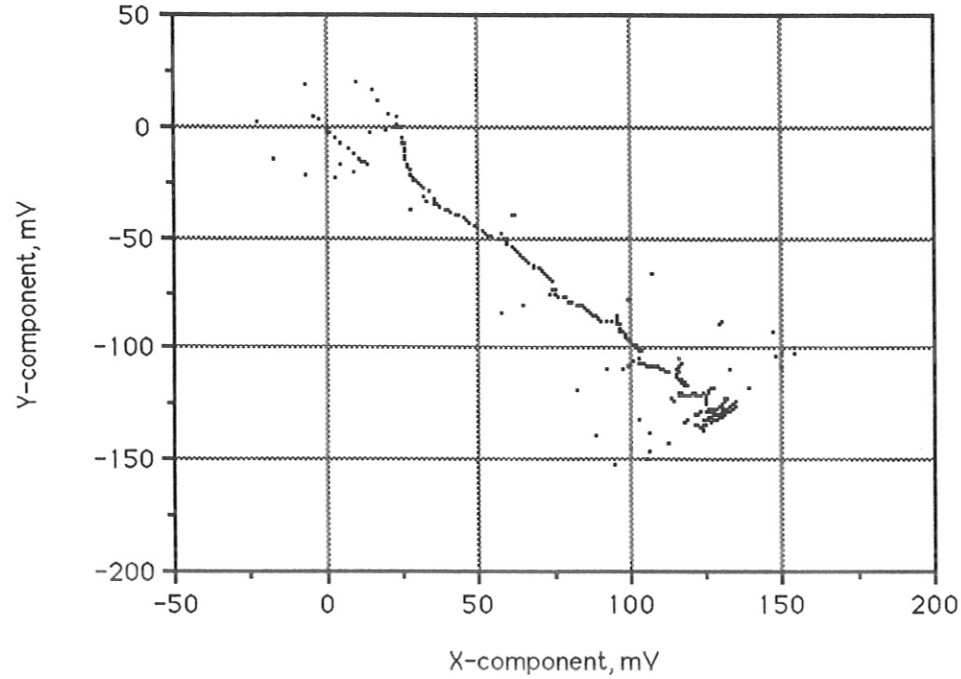


Fig.8a: Simultaneous Response of Both Loops

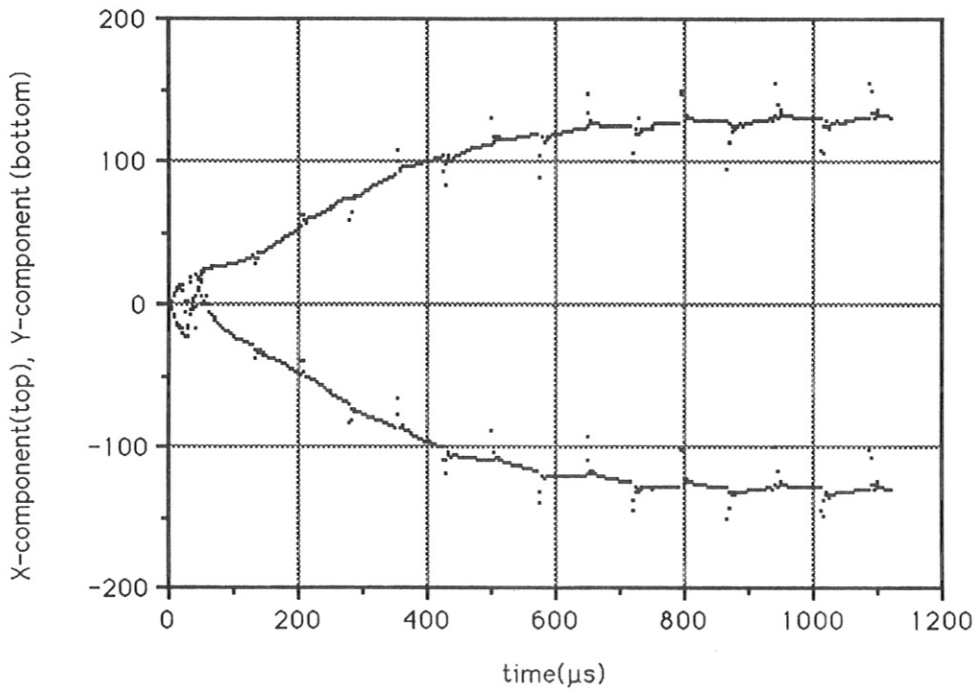


Polar Plot

case 2:

fast response of PLL

Output of Quadrature Mixer versus Time:



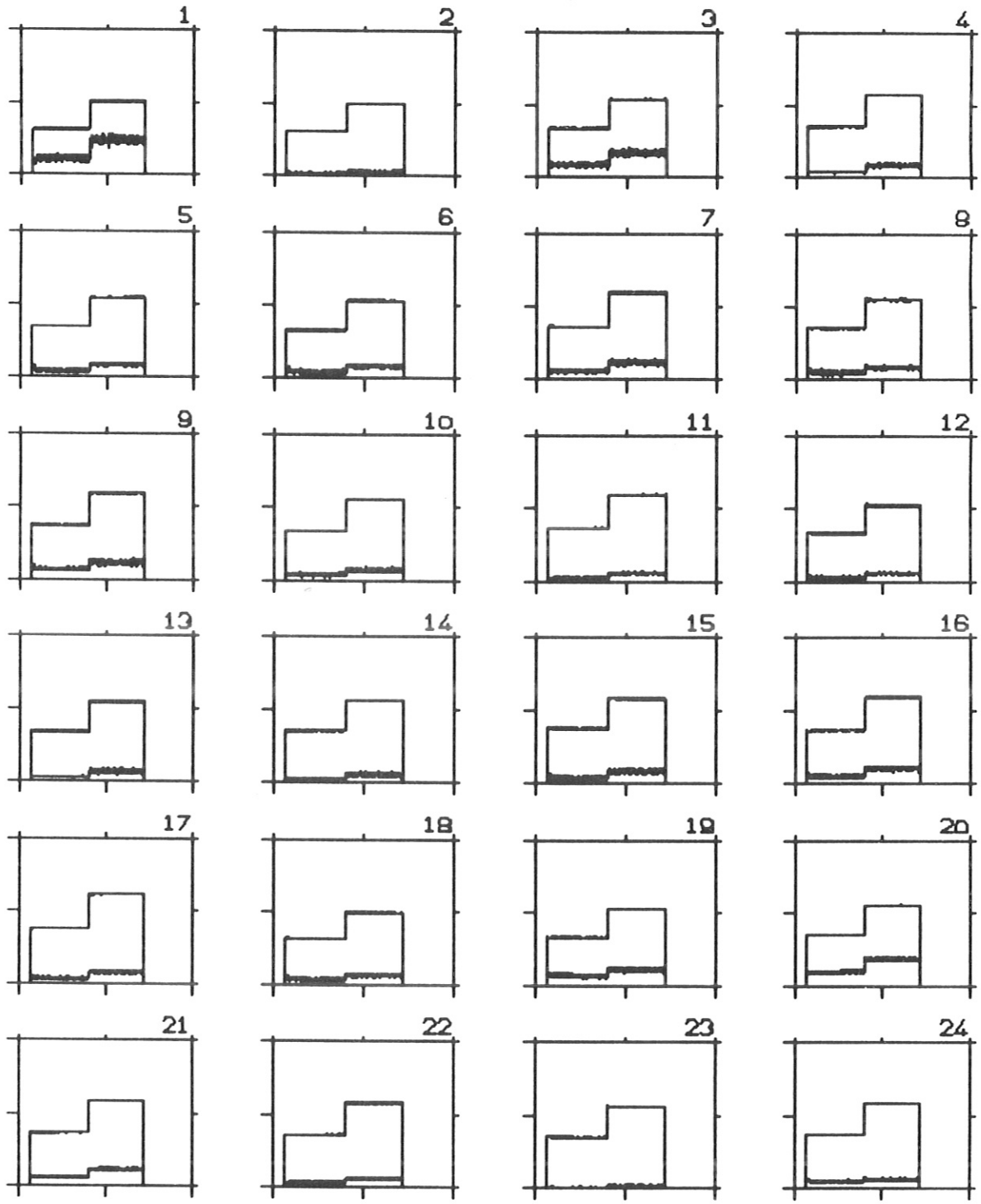


Fig.9: Incident and Reflected Power in Upper Grill
(Variable Pairs HiL, RiL, i = 1 through 24)

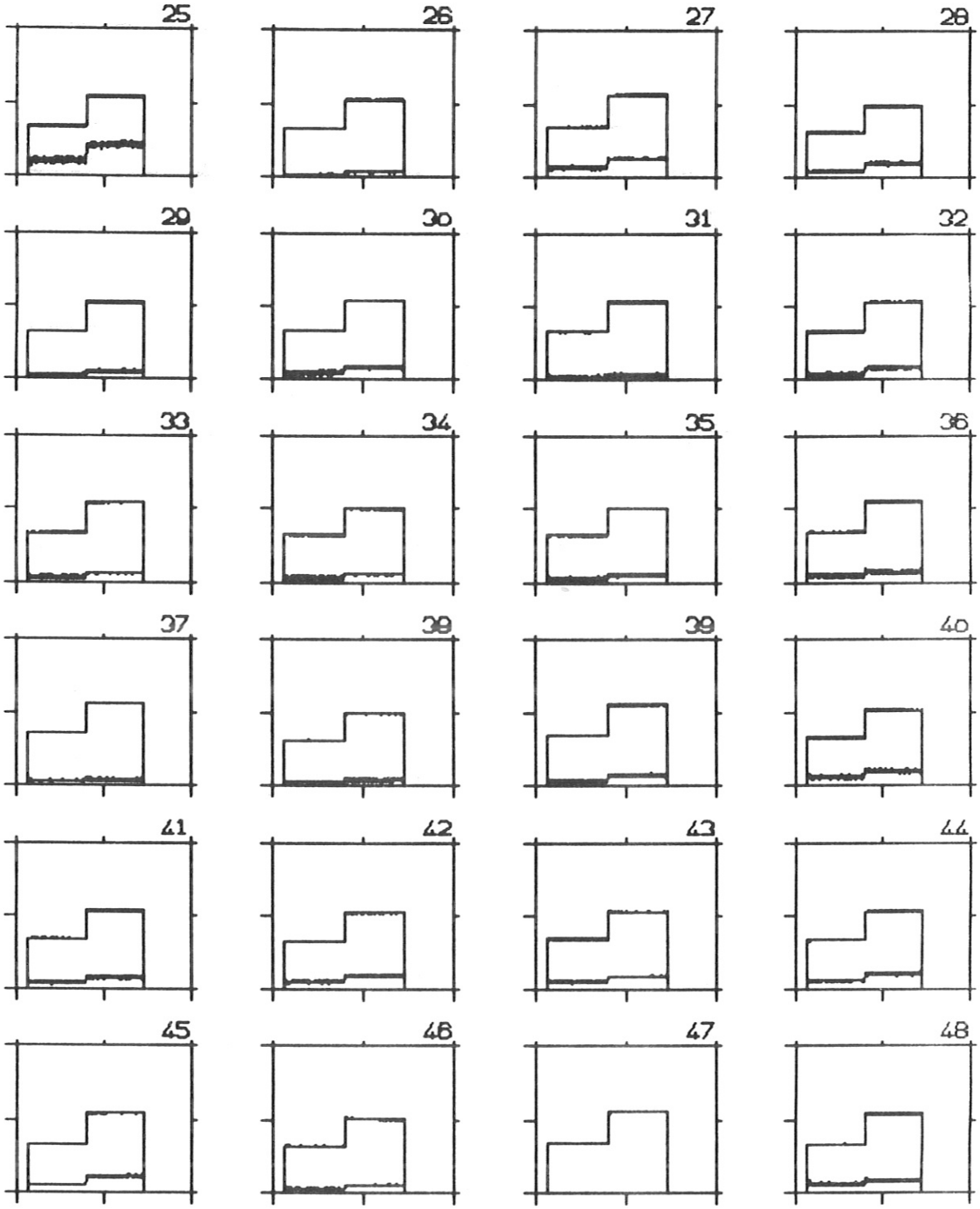


Fig.10: Incident and Reflected Power in Lower Grill
(Variable Pairs HiL, RiL, i = 25 through 48)

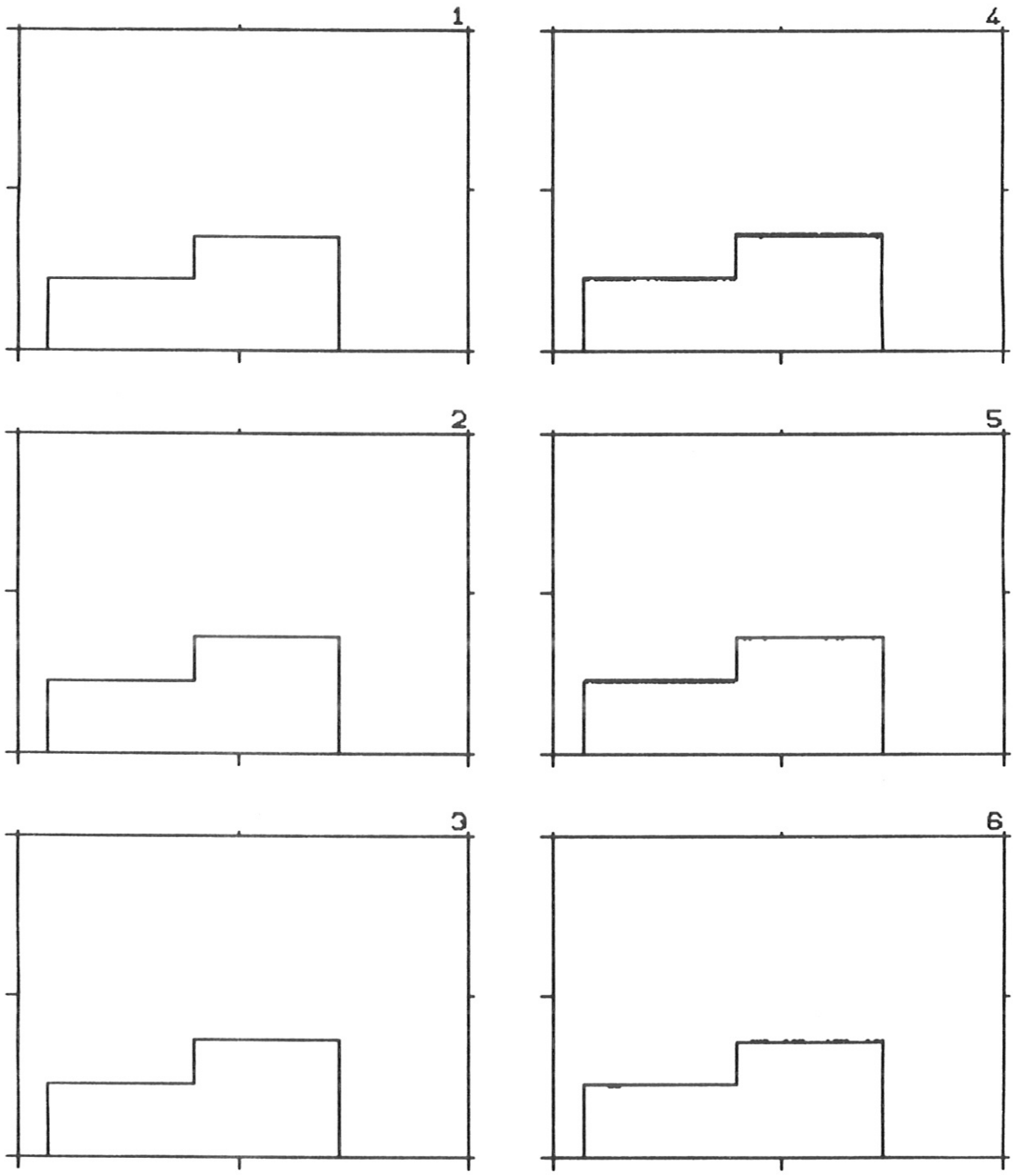


Fig.11: Incident Power at '1 to 48'-Power Divider
(Variables KiL, i = 1 through 6, Power at Klystron Outputs)

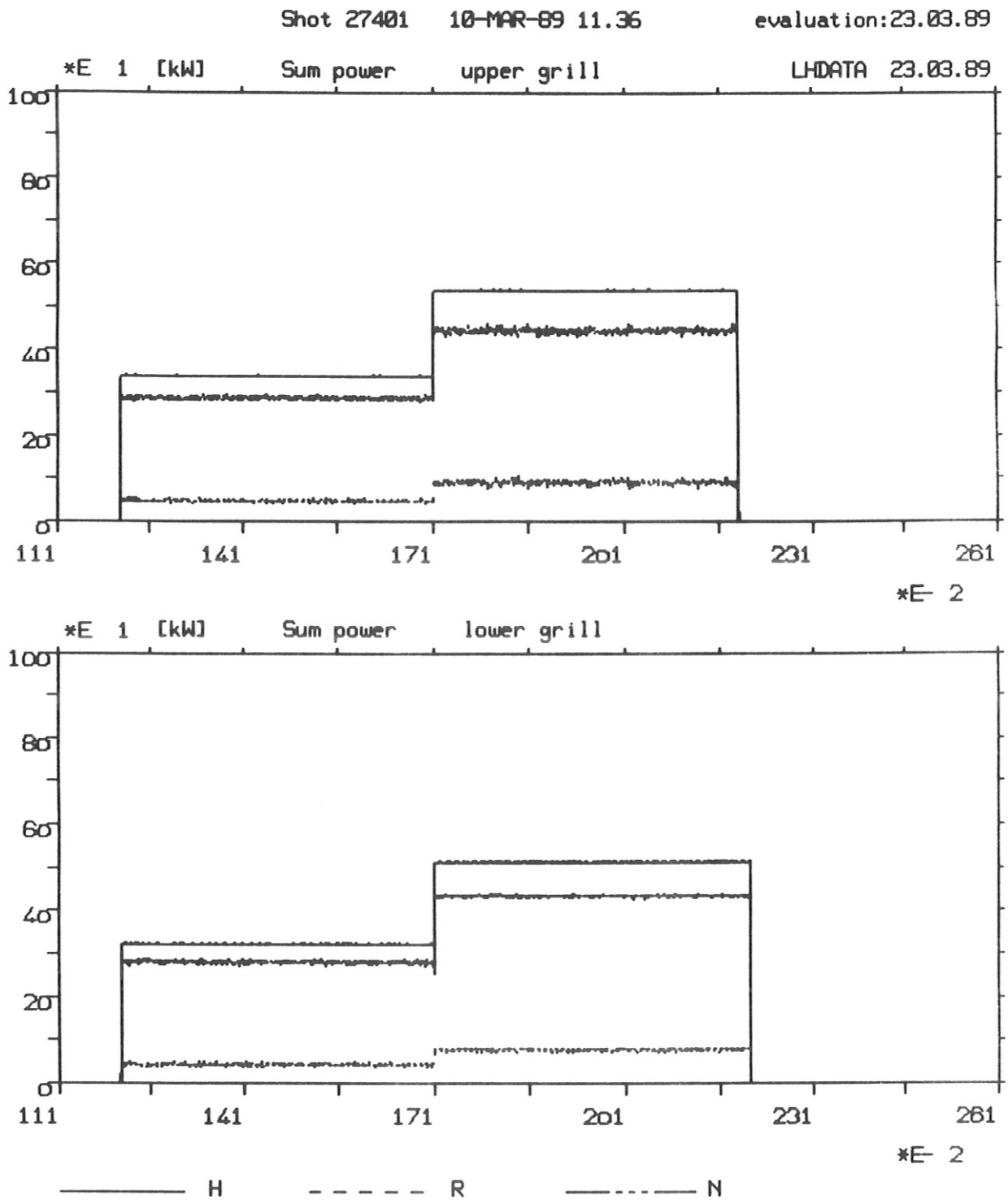
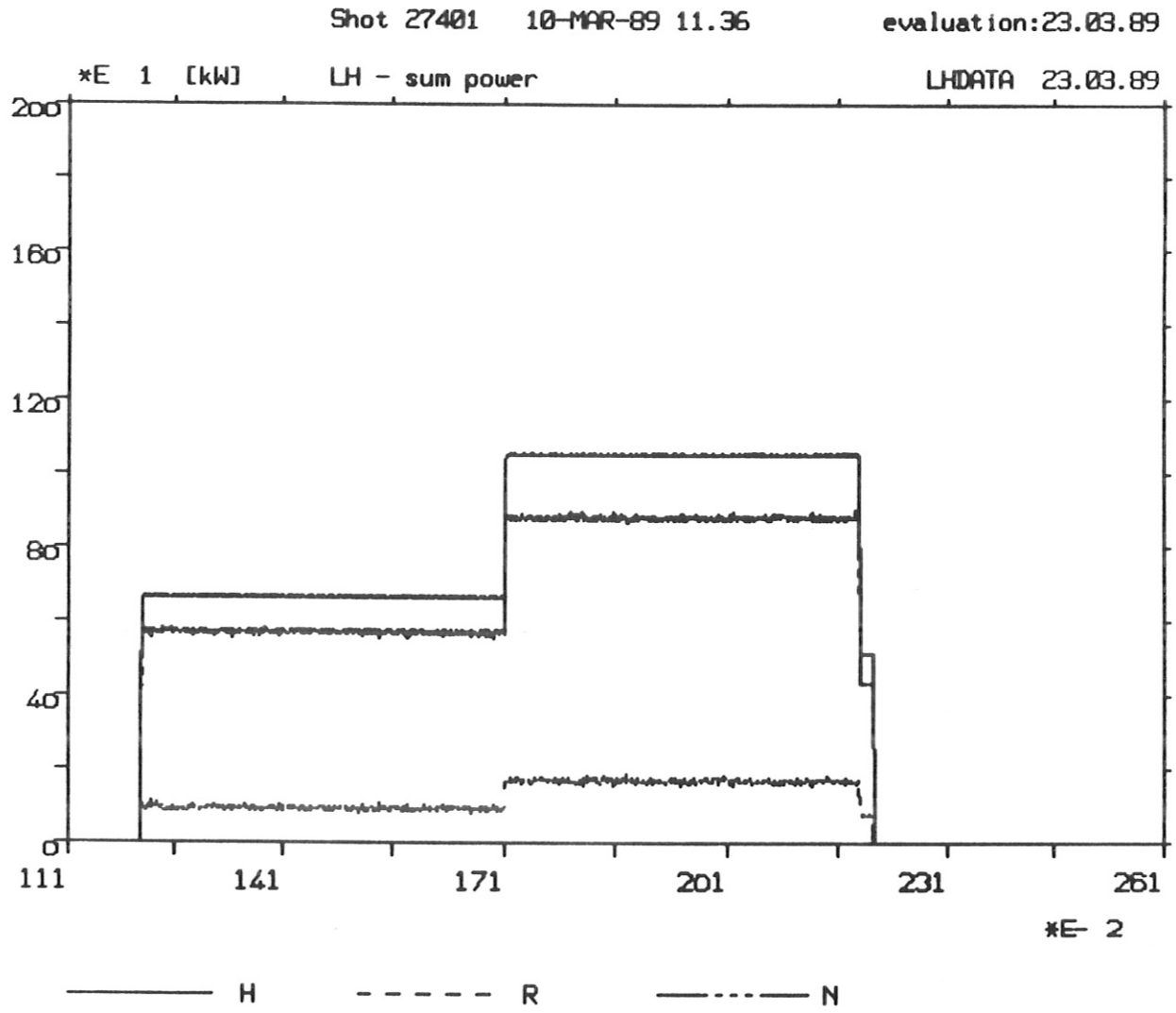


Fig.12: Total Power at Upper- (Top) and Lower- (Bottom) Grill



	upper	lower	total
LH-time [sec]:	1.211 - 2.190	1.212 - 2.209	1.211 - 2.209

Fig.13: Total Power (Incident, Reflected, Net)
(All 48 Channels of the Antenna)

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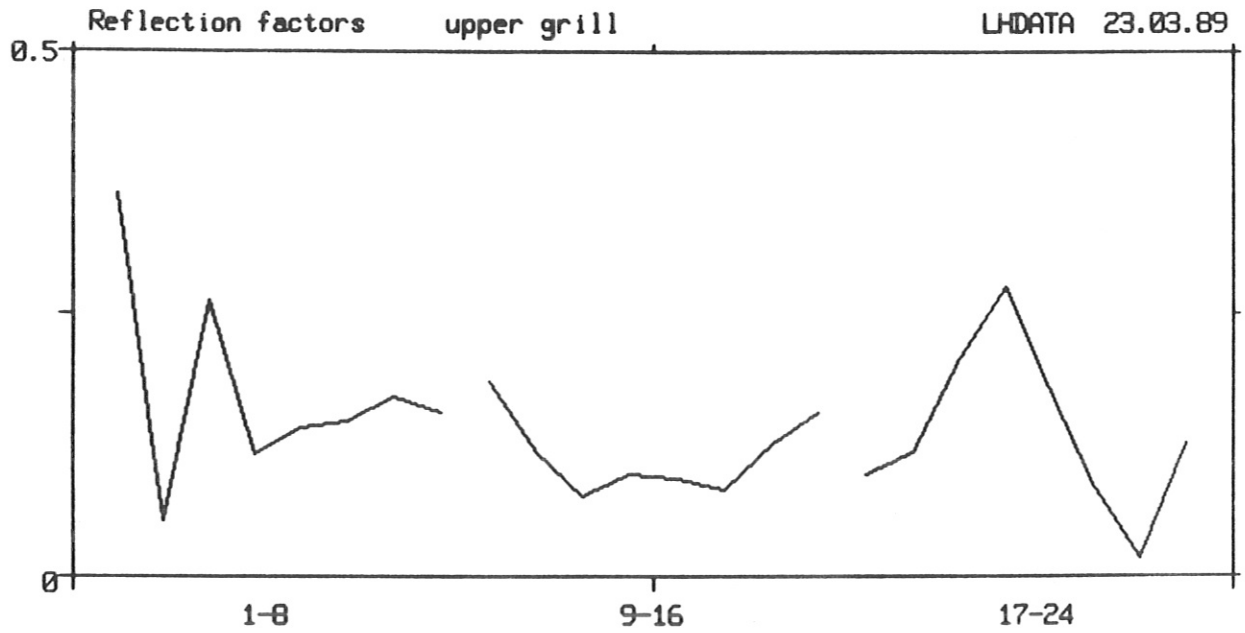
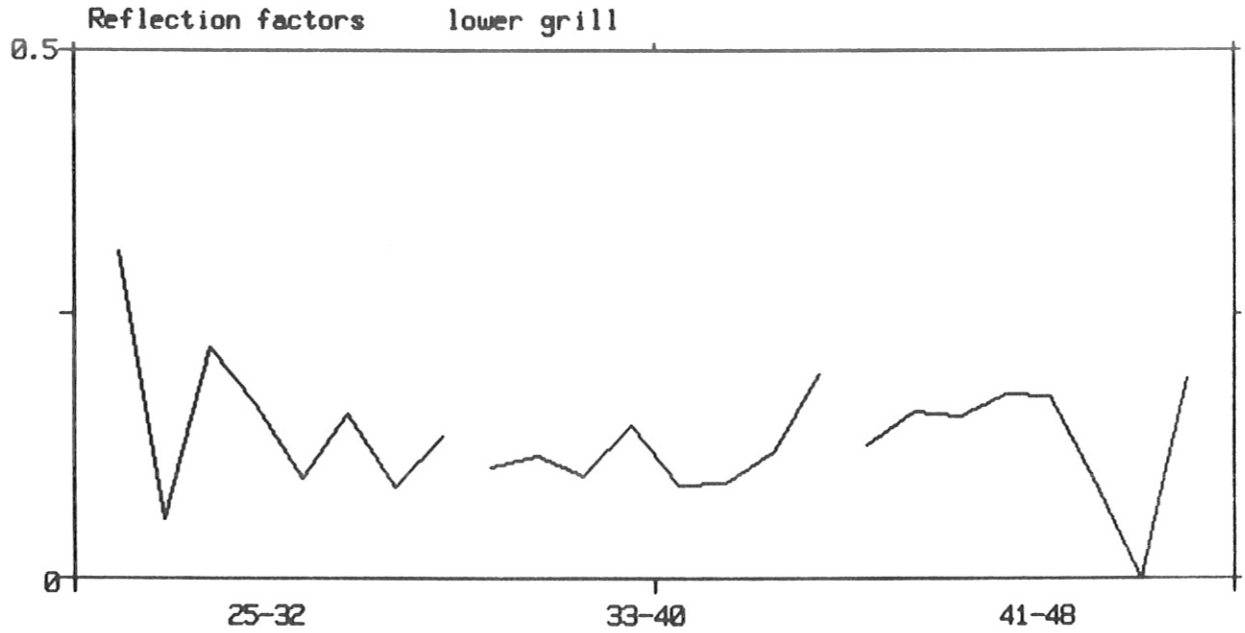
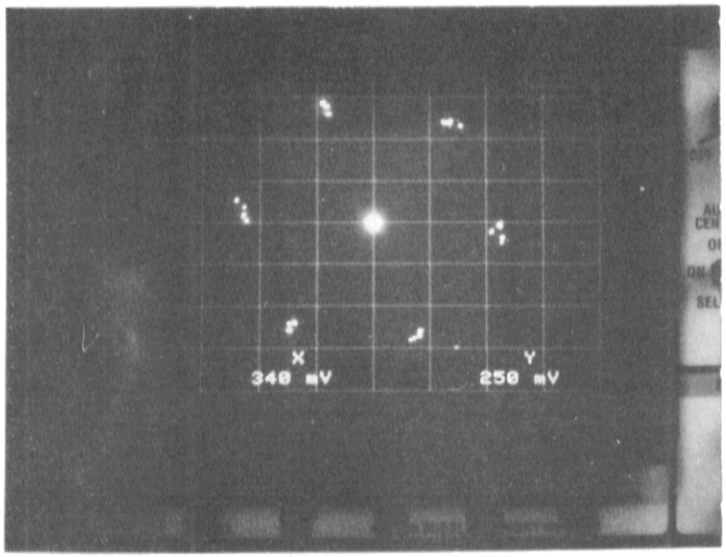
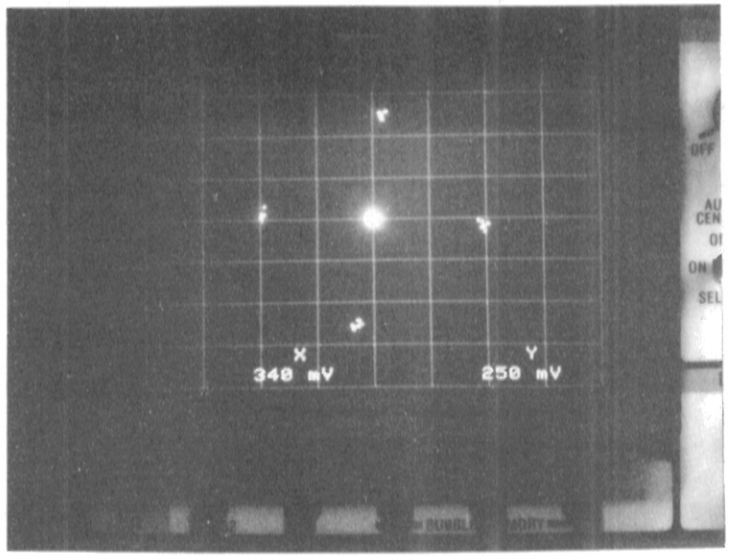


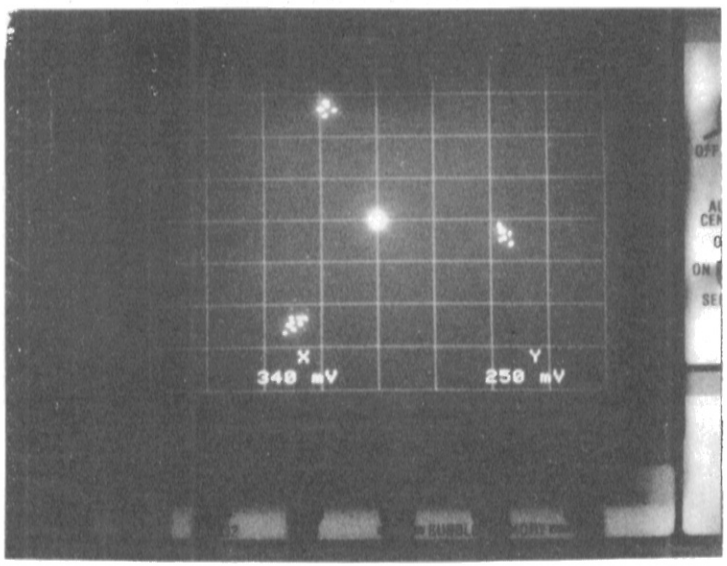


	upper	lower	T: 1.410 - 1.430
LH-Inc. [kW]:	356.7	341.1	
LH-Refl. [kW]:	51.4	45.9	
LH-Net. [kW]:	305.3	295.2	
Refl/Inc. [1]:	0.144	0.134	

Fig.14: Reflection Diagrams







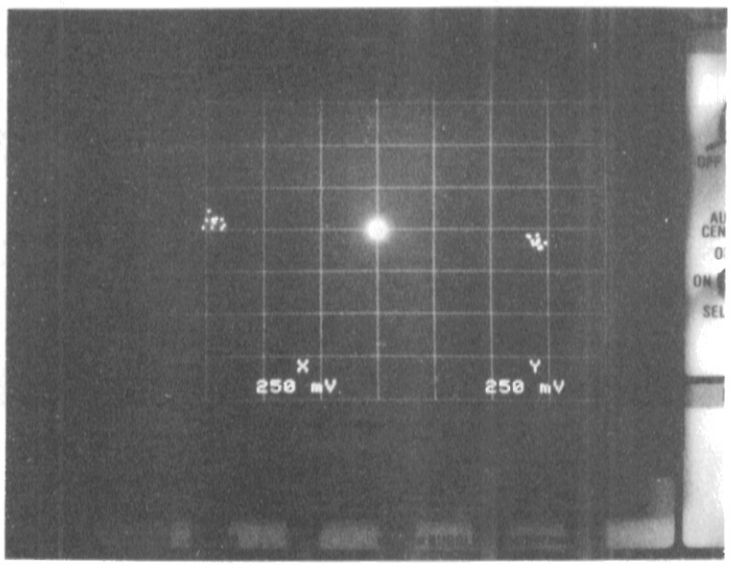
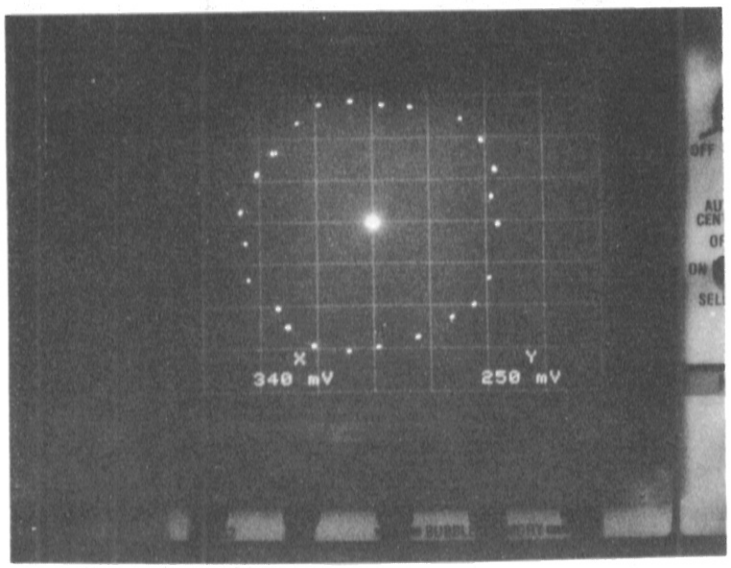
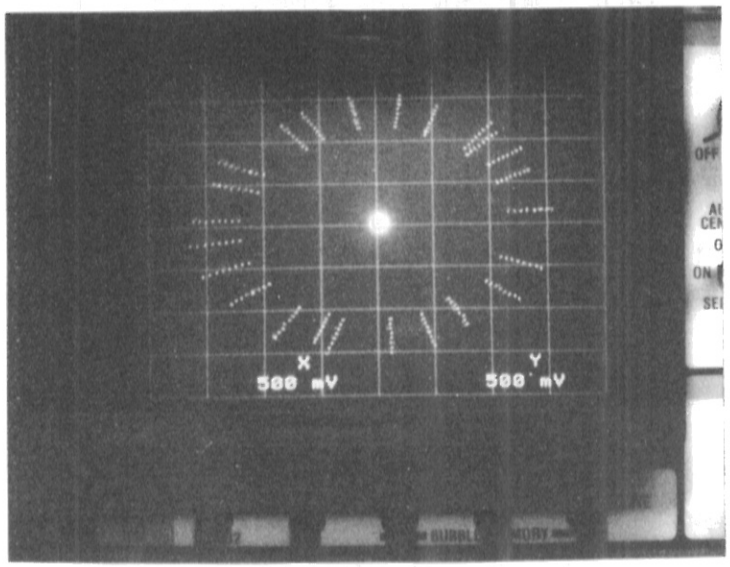
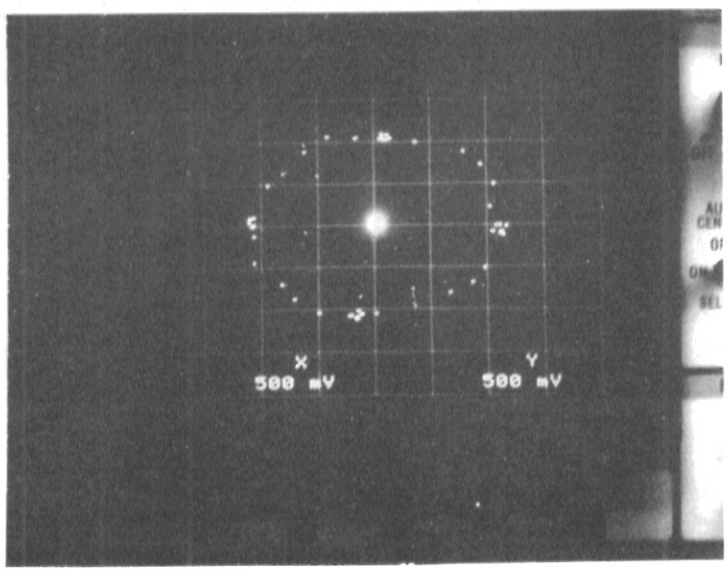


Fig. 15:
Output of Grill Phase Monitor
(Phasings:
60° 90°
120° 180°)







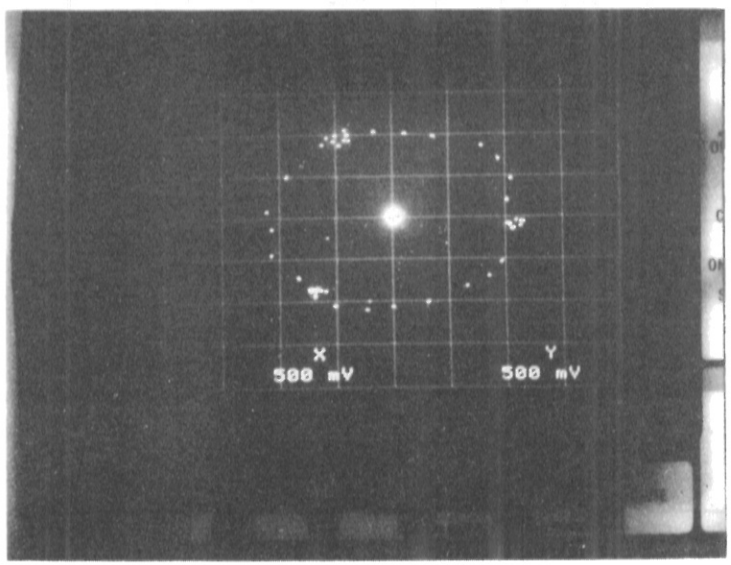


Fig. 16:
Output of Grill Phase Monitor
(Phasings:

upper, lower,
75°, 75°,
without with
power modulation

mixed phasings at
upper and lower grill:
75° and 75° and
90° 120°)