

The Distribution of Voltage in a
Capacitor in Response to applied
Pulses

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INSTITUT FÜR PLASMAPHYSIK
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The Distribution of Voltage in a
Capacitor in Response to applied
Pulses

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Abstract

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A capacitor was excited with pulse rise-times between 50 nsec and 3.5 μ sec and the distribution of internal voltages plotted. The capacitor was also driven with a power oscillator in the frequency range 1 kc/s to 5 Mc/s and the internal voltage plotted as a percentage of the terminal voltage.

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Abstract

A capacitor was tested with pulse rise-times between 30 nsec und 3.6 μ sec and the distribution of internal voltages plotted. The capacitor was also driven with a power oscillator in the frequency range 1 kc/s to 5 Mc/s and the internal voltage plotted as a percentage of the terminal voltage.

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1. Introduction

Capacitors can frequently be subjected to applied voltage pulses of high amplitude and/ or frequency. Under these conditions it is important to know how this applied pulse voltage is distributed across the various circuit inductances, and in particular, what voltage must be withstood by the windings of the capacitor.

The capacitor used for these tests was a B.I.C.C. 7.7, μF , 18 kV DC charge, serial number X 2411/34. The case was cut open and drained of oil, giving access to the internal connections. The internal layout is sketched in fig 1 (a), but it should be noted that the inter-winding connections were as short as possible and the upper and lower connections were in the same plane - not as drawn for clarity in fig 1 (a)

Some windings on one half of the capacitor were damaged during the opening of the case and that half was disconnected from the output terminals and the tests made on one half only (3.85, μF nominal value).

2. Tests

Because the capacitor was no longer oil-filled, all the tests had to be made at low voltage which gave a large apparent internal resistance.

The discharge and applied pulse tests were very limited in the range of rise-times which could be conveniently covered and the oscillator test was necessary to give full coverage.

The results of the discharge and applied pulse tests are graphed in figs 6 to 10 inc. These show that for very slow pulses, the

2.1 Capacitance measurement

Using the Wayne Kerr Universal Bridge, the capacitance between the output terminal and earth was measured. Also, measurements were made across each set of windings and the capacitance to earth calculated for each measuring position. The bridge measuring frequency was 1.592 kc/s.

2.2 Discharge

The circuit diagram is shown in fig 2 and two values of the inductance in the switch branch were used. Discharging the capacitor produced a very heavily damped waveform due to the characteristics of the dielectric at such a low voltage, but as the results are a comparison of amplitudes, they are never the less valid.

2.3 Applied pulse

The circuit diagram is shown in fig 3. The switch was the same for each test, but three different capacitors were used for c, to obtain different rise-times of the applied pulses.

2.4 Power oscillator

The circuit diagram is shown in fig 4 with a list of the equipment used.

3. Results

The results of the capacitance measurement are recorded in fig 5, where the reciprocal of capacitance is plotted against the measuring positions. This therefore shows the error which can be expected between the two sets of windings, due to capacitive division alone.

The results of the discharge and applied pulse tests are graphed in figs 6 to 10 inc. These show that for very slow pulses, the capacitor winding takes the full amplitude and that close to the resonance frequency, the windings may experience an amplitude about 20 % higher than that applied. Reference to the vector diagrams in fig 11 clarify how it is possible to measure a greater amplitude at the windings than is measured at the external

terminal. In the above measurements, the detector was insensitive to the phase of the signal. With faster pulses, the inductance of the output termination absorbs up to 40 % of the applied amplitude and therefore limits the loading of the winding.

The results of the oscillator tests are plotted in fig 12 and for a smaller frequency range in fig 13. These graphs confirm the results of the pulse tests qualitatively but the agreement at higher frequency is not very satisfactory. The upward trend of the graph at higher frequency may be less pronounced than is indicated, but it is predictable by the increase in resistance.

Fig.1(a) Internal layout and connection of windings

Fig.1(b) Equivalent circuit showing the measuring positions

4. Conclusion

The results show how the applied pulse will be divided between the circuit inductances and the extent to which the capacitor windings are protected against fast pulses by the inductance of the output termination. From these results it appears that, of the total inductance of the unit, the winding itself constitutes about 60 %.

5. Acknowledgements

The provision of the test facilities by the High Voltage Technology Group is hereby acknowledged.

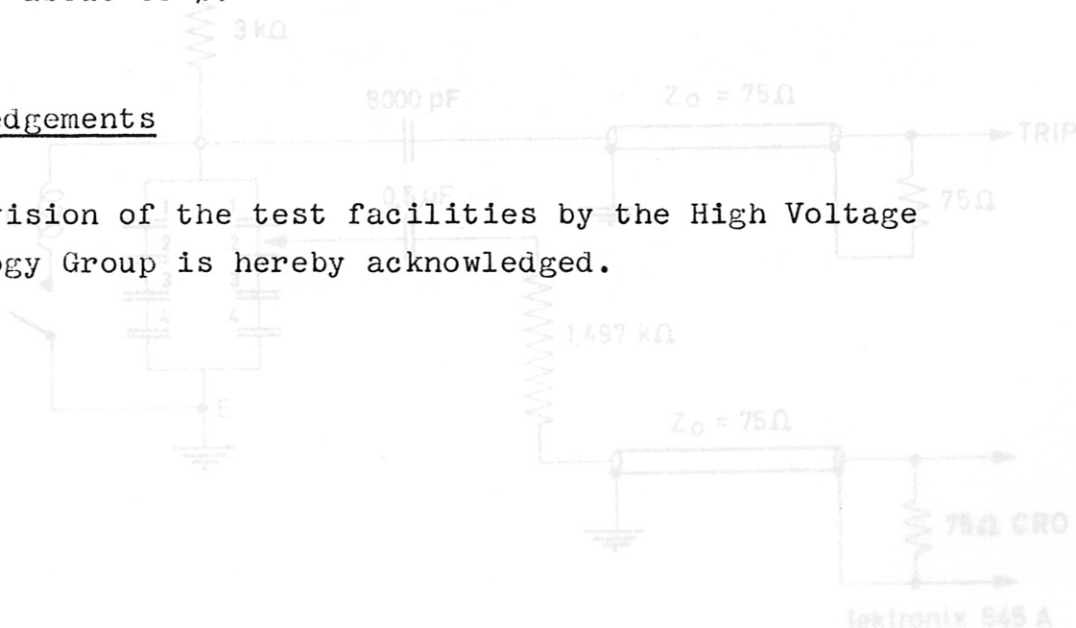


Fig.2 Circuit diagram for discharge tests.

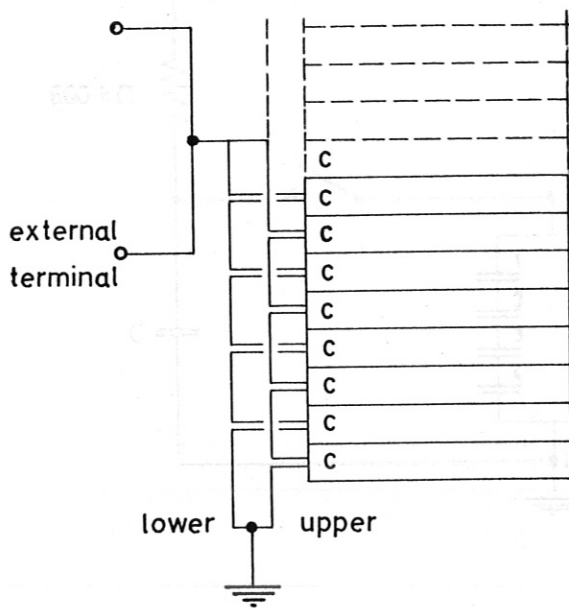


Fig.1(a) Internal layout and connection of windings (drawn for 1/2 culy)

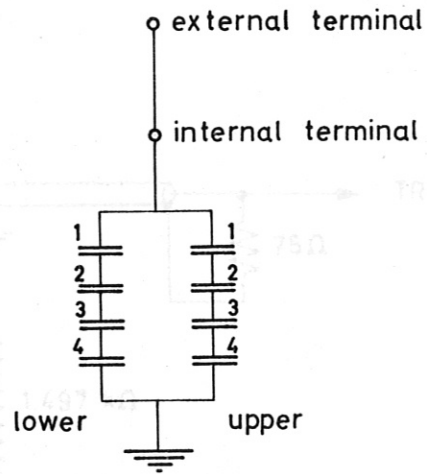


Fig.1(b) Equivalent circuit showing the measuring positions

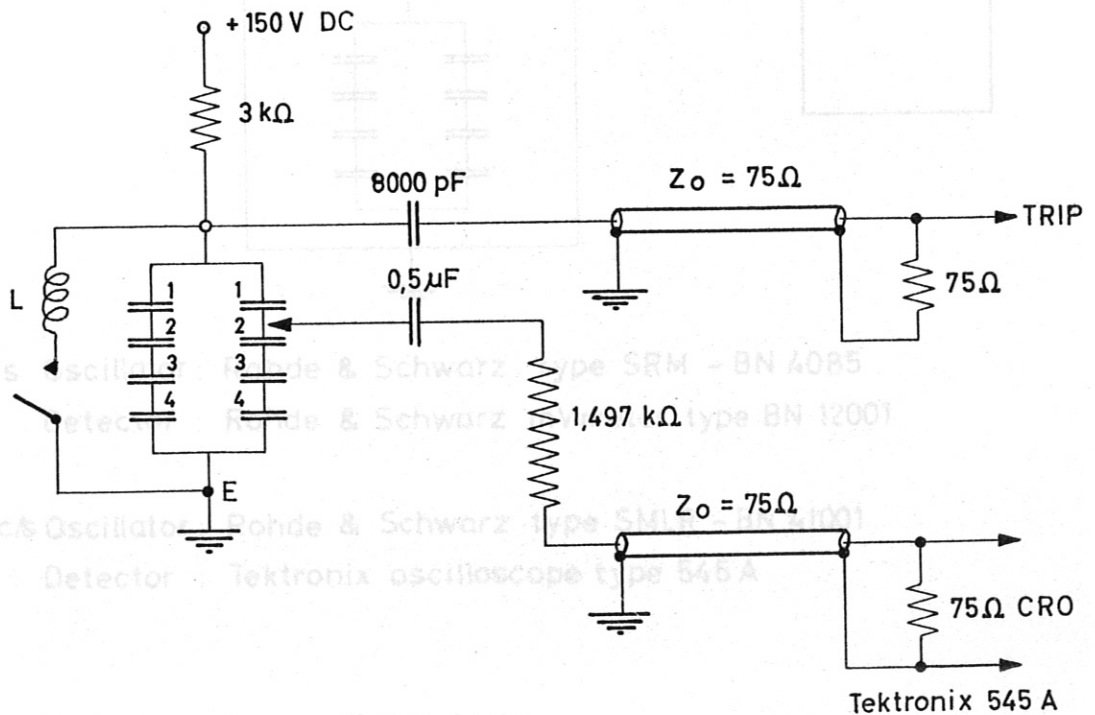


Fig.2 Circuit diagram for discharge tests.

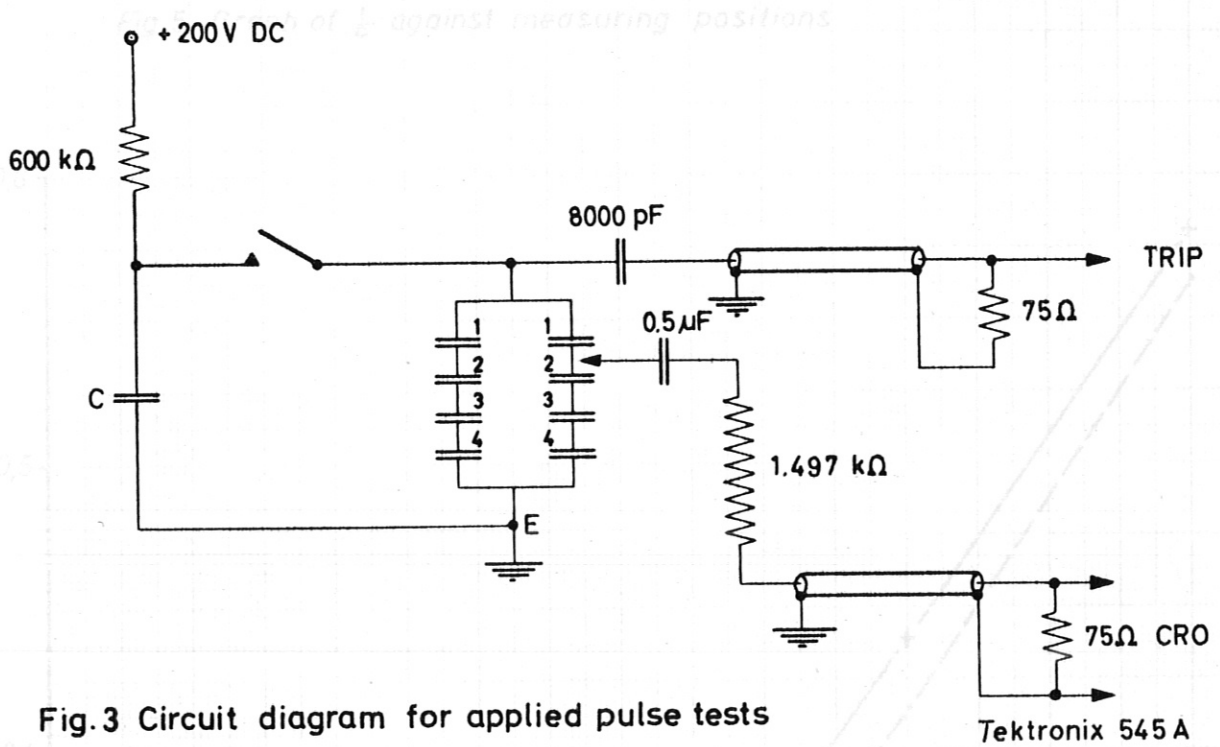
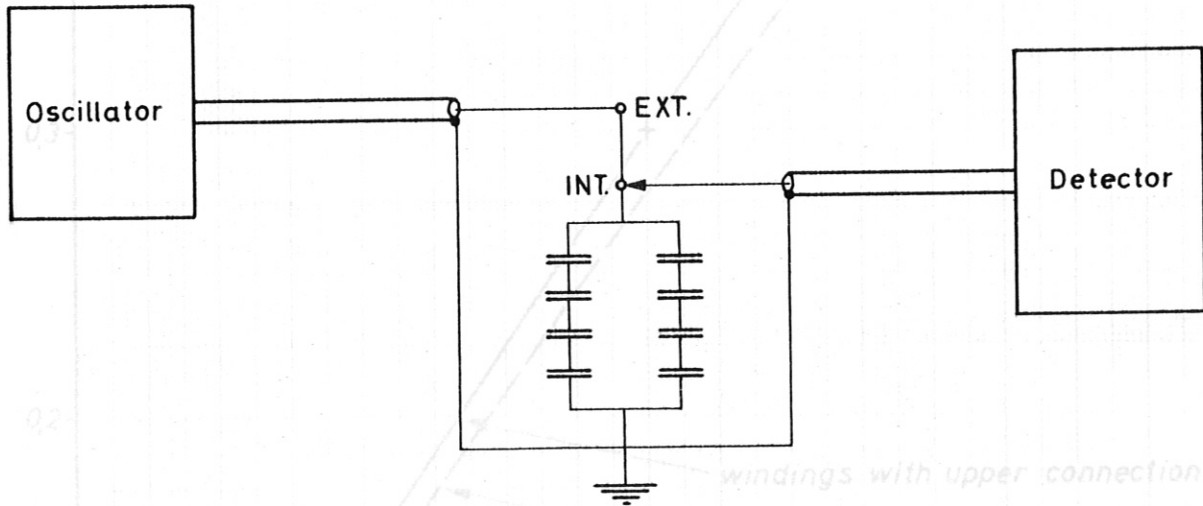


Fig.3 Circuit diagram for applied pulse tests



1 - 100 kc/s Oscillator : Rohde & Schwarz type SRM - BN 4085
 Detector : Rohde & Schwarz mVmeter type BN 12001

100kc/s to 5Mc/s Oscillator : Rohde & Schwarz type SMLR - BN 41001
 Detector : Tektronix oscilloscope type 545 A

Fig.4 Circuit diagram for oscillator tests.

Fig.5 Graph of $\frac{1}{C}$ against measuring positions

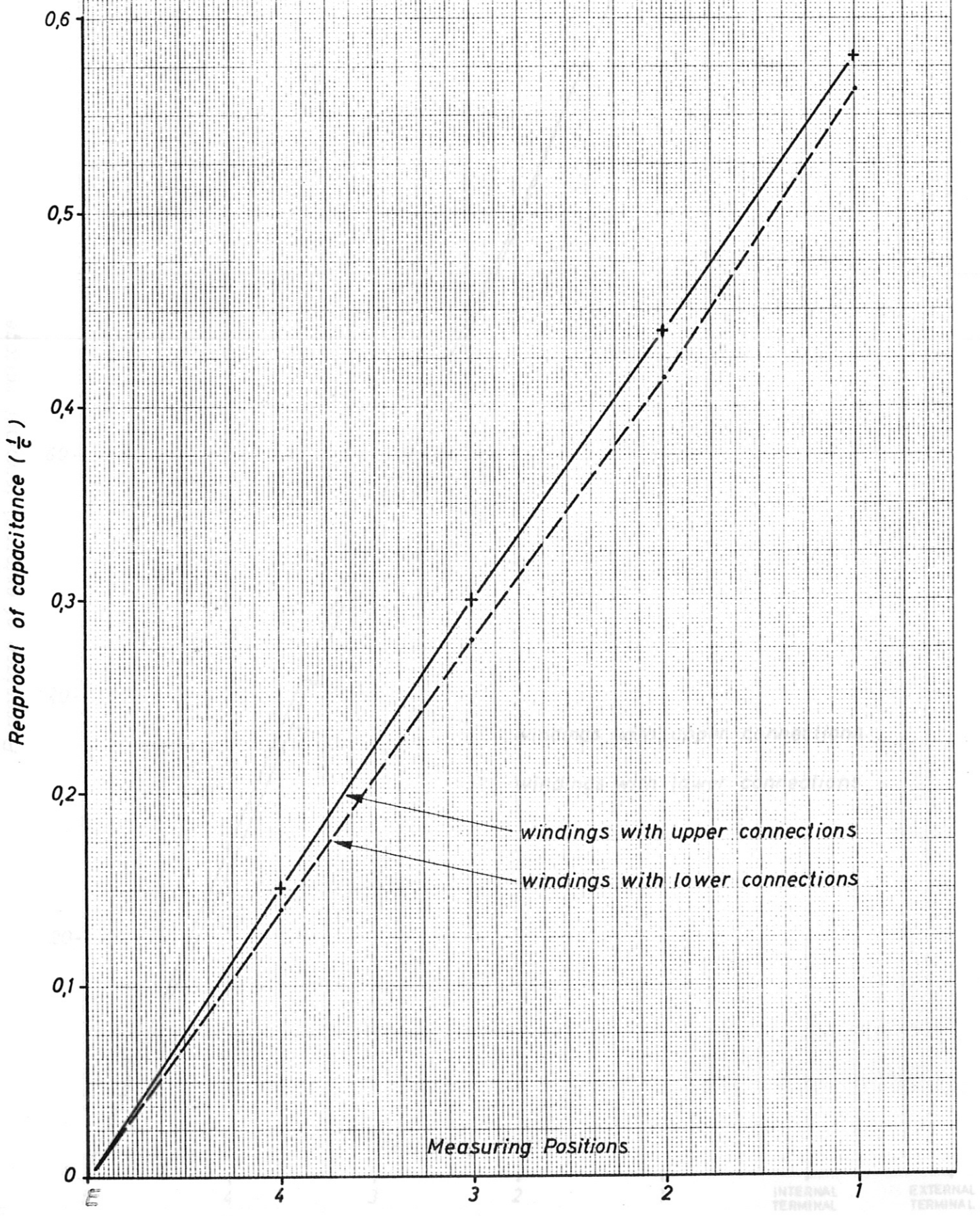
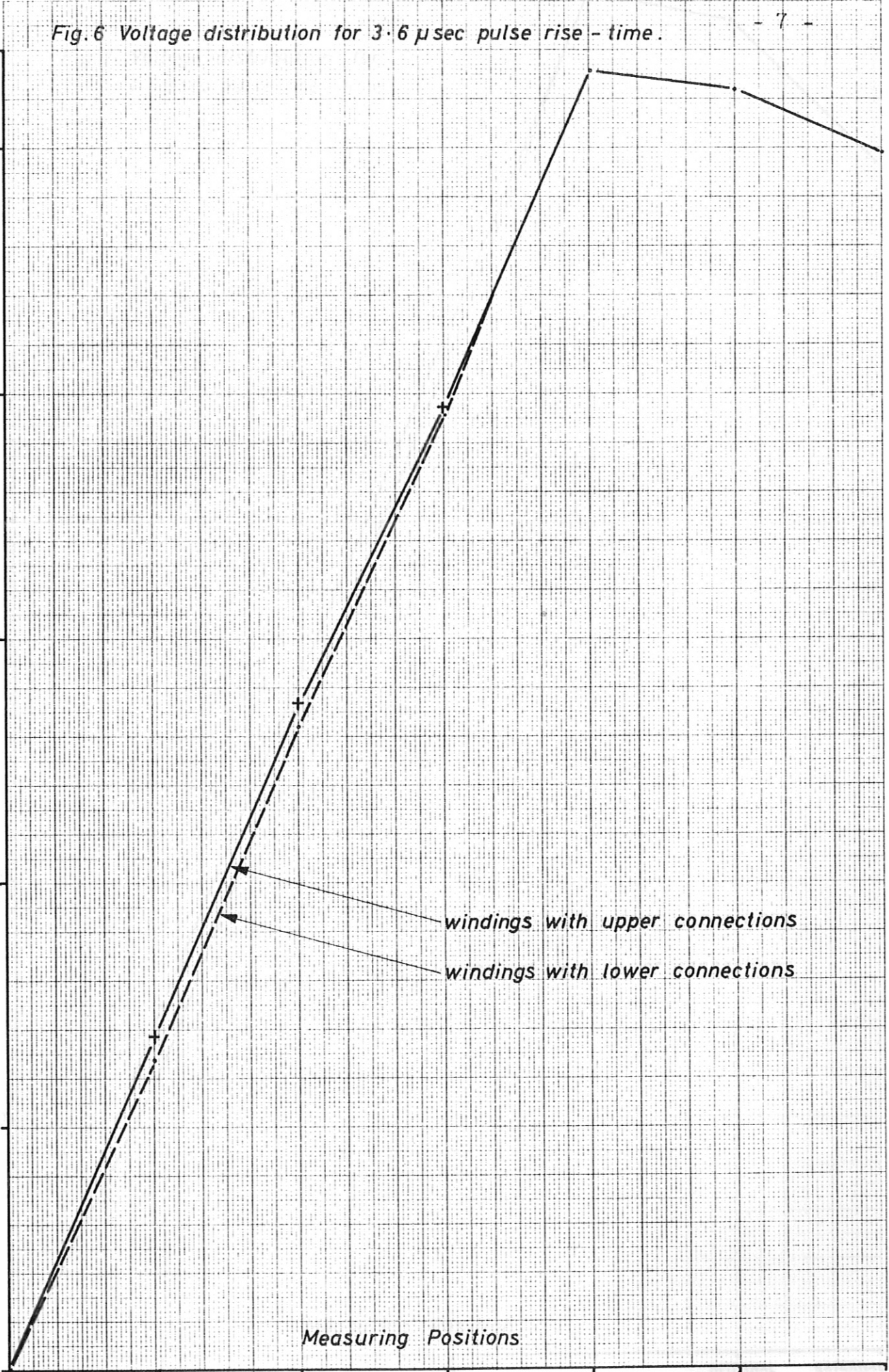


Fig. 6 Voltage distribution for 3.6 μ sec pulse rise - time.

Percentage of external terminal voltage

108
100
80
60
40
20
0



Measuring Positions

INTERNAL TERMINAL EXTERNAL TERMINAL

windings with upper connections
windings with lower connections

Fig.7 Voltage distribution for
1.5 μ sec pulse rise-time

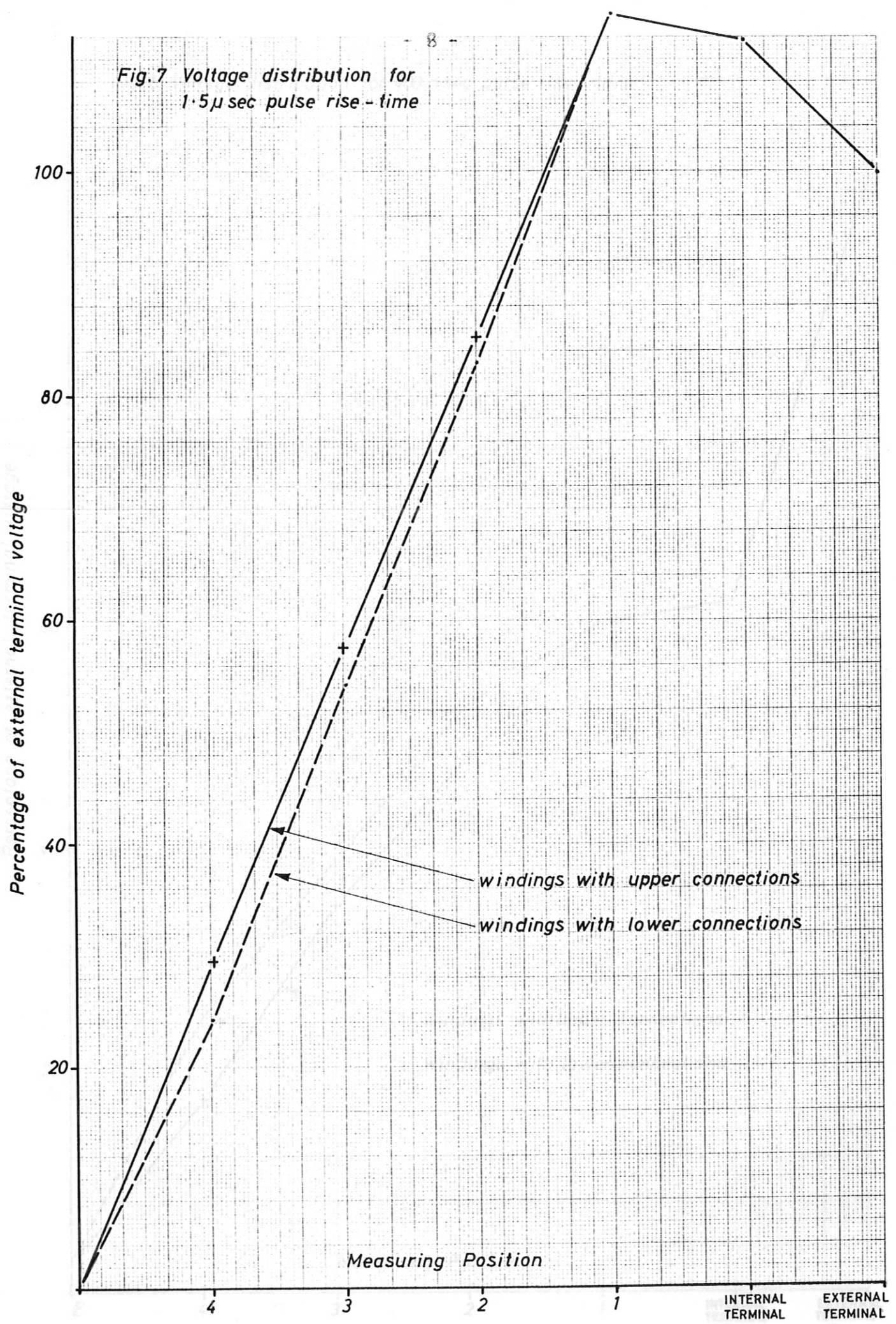


Fig. 8 Voltage distribution for 400 nsec pulse rise - time

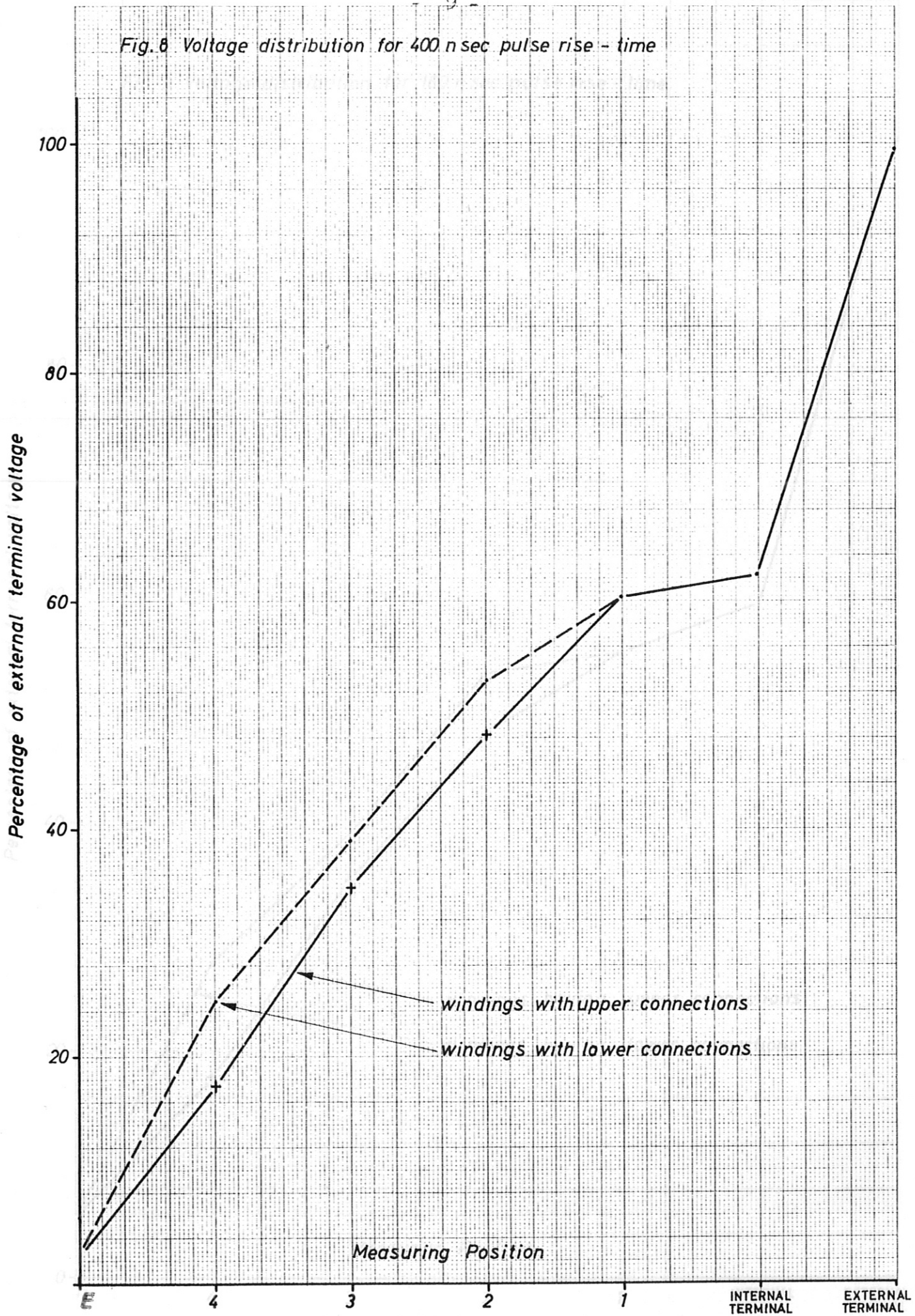


Fig. 9 Voltage distribution for 160 n sec pulse rise - time

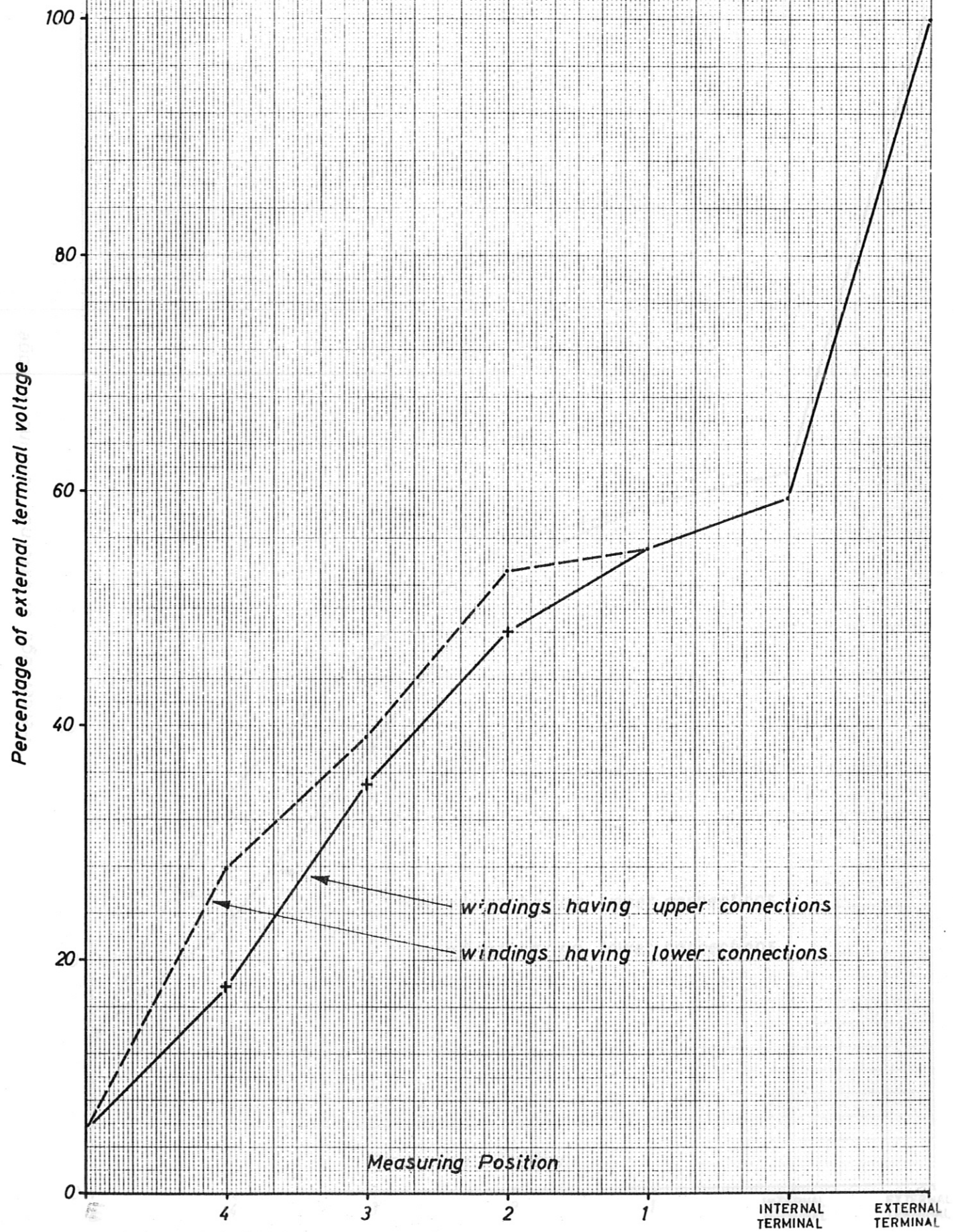
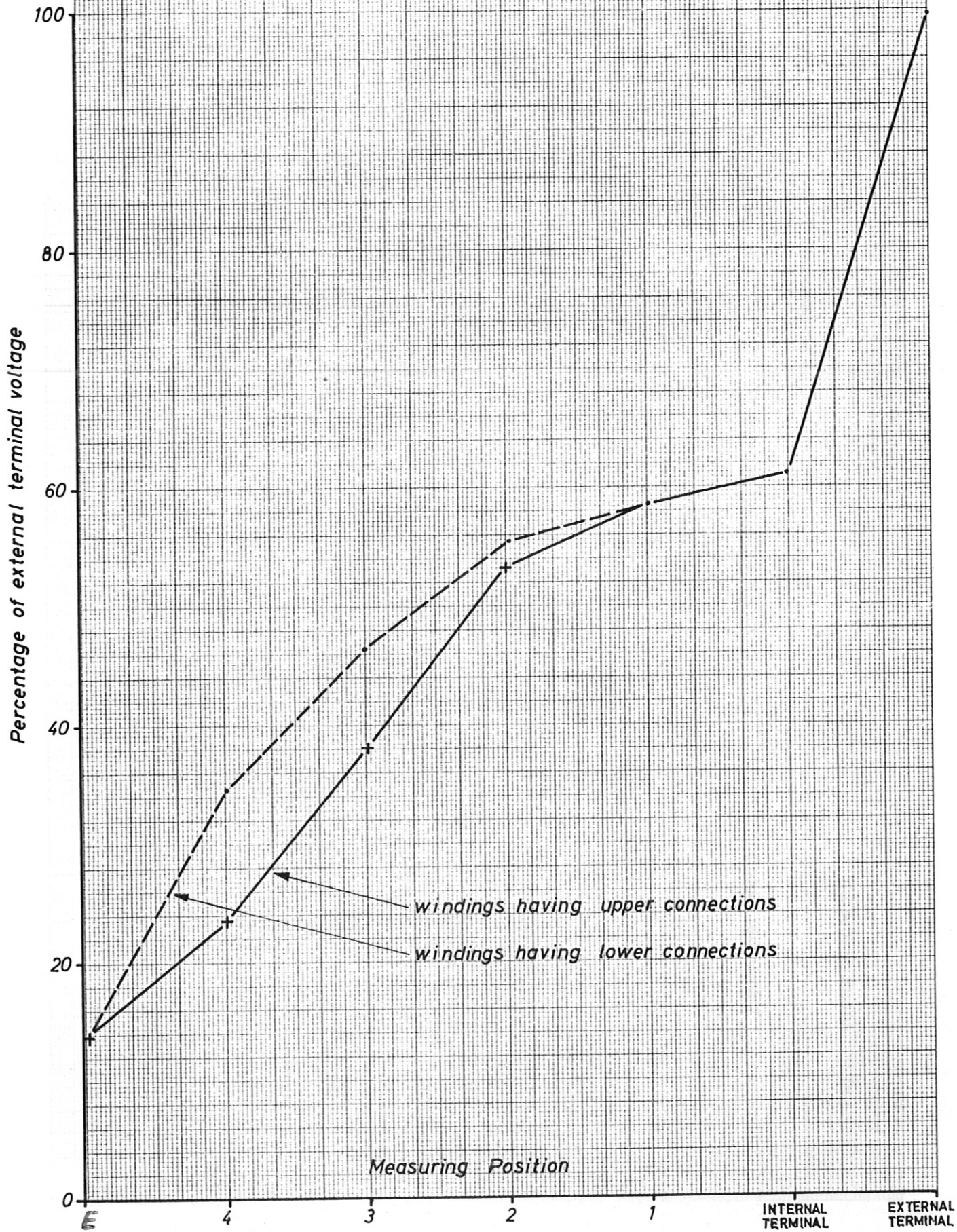
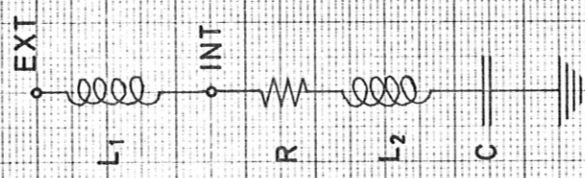
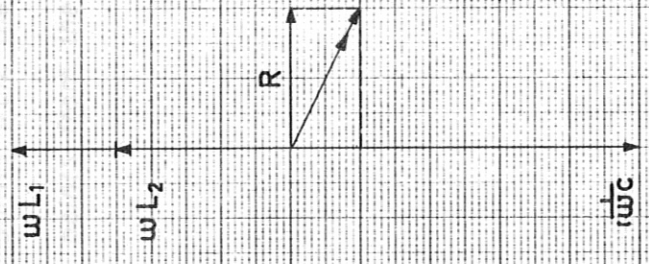


Fig. 10 Voltage distribution for 30 nsec pulse rise - time

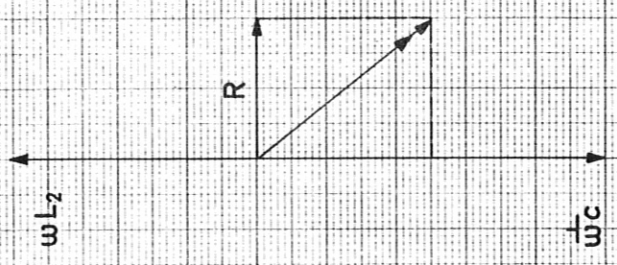




Equivalent circuit



at the external terminal



at the internal terminal

Fig. II Vector diagrams

Fig. 12 Internal voltage as a percentage of the terminal voltage (1Kc/s to 5Mc/s.)

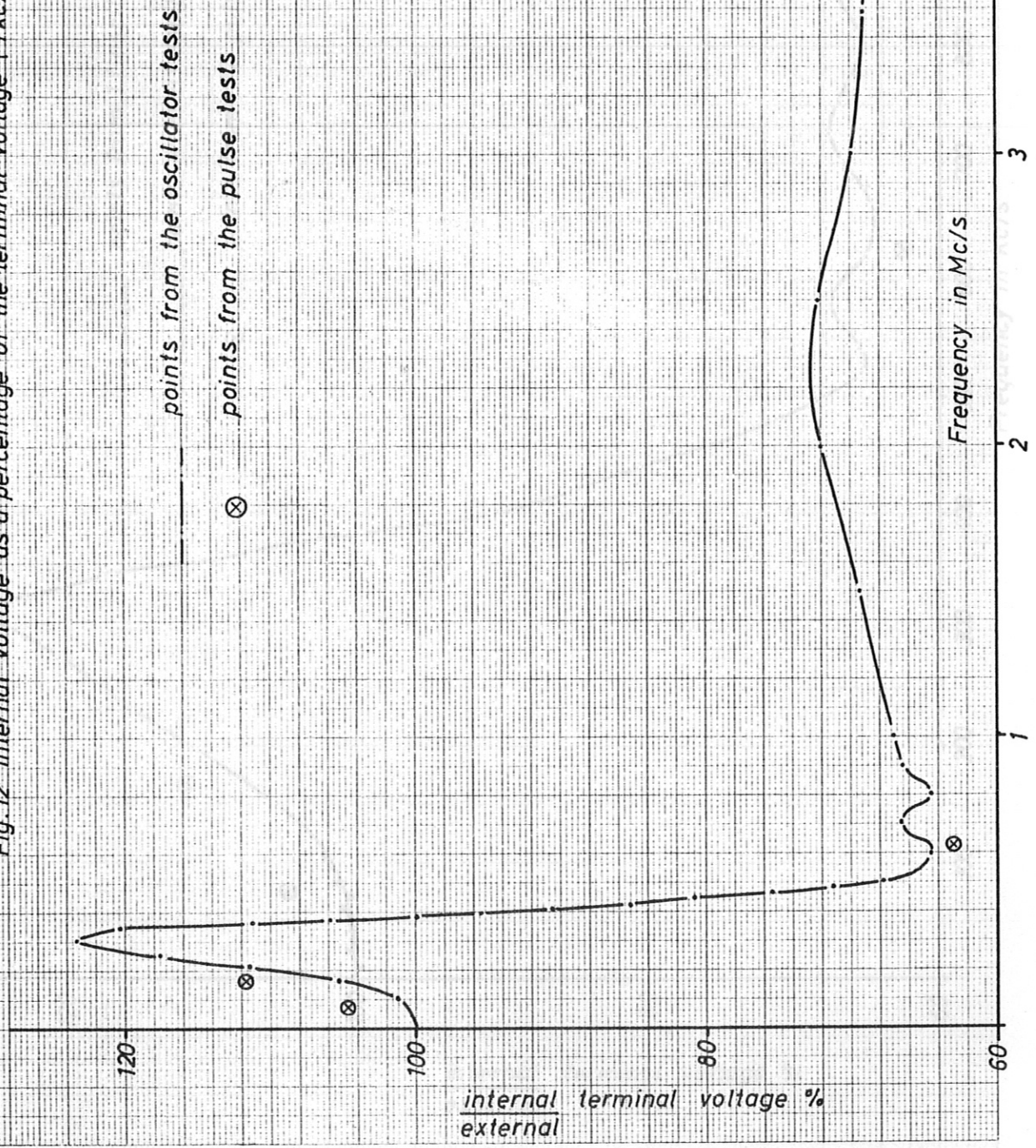
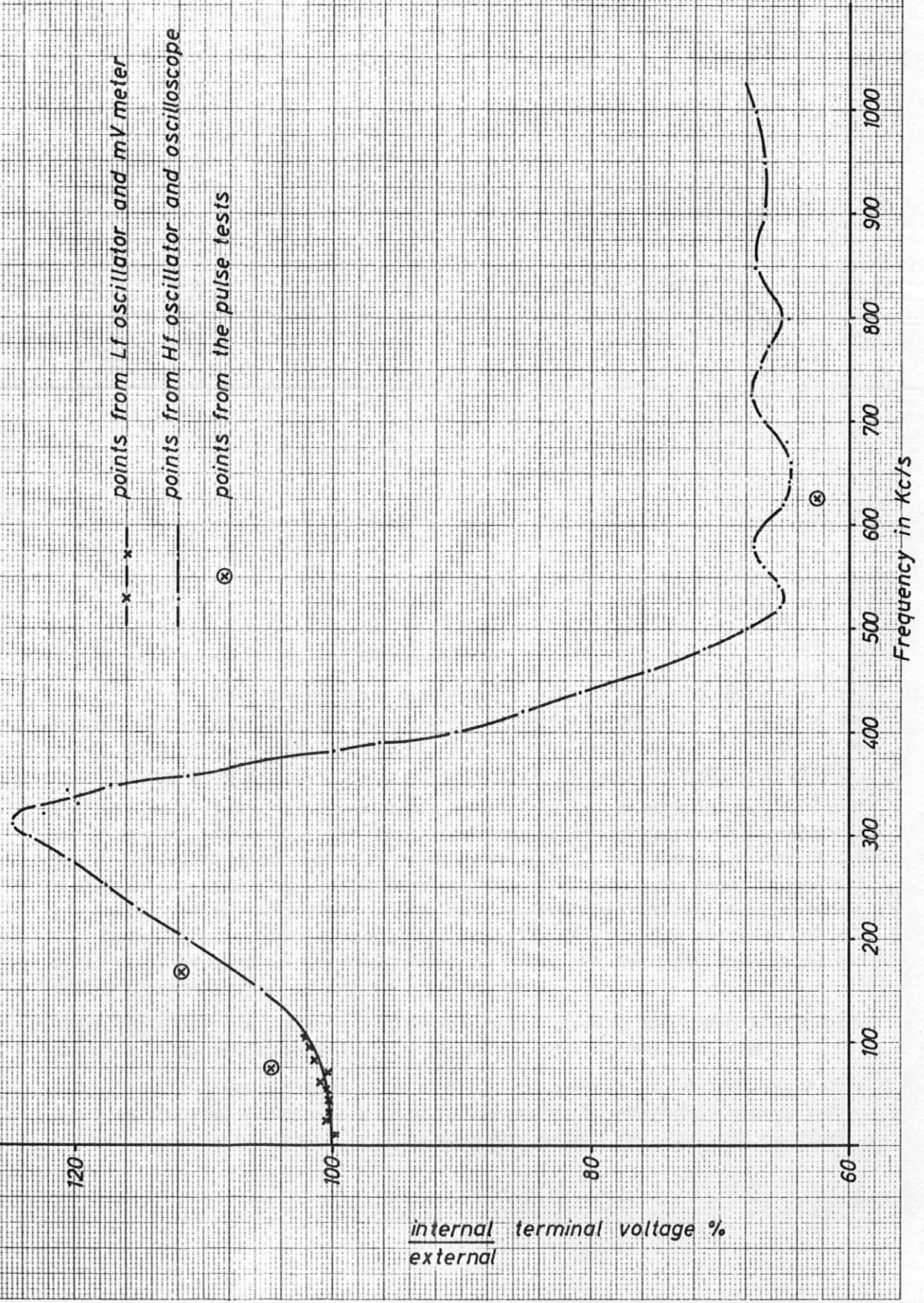


Fig. 13 Internal voltage as a percentage of the terminal voltage (1 - 1000 Kc/s)



$\frac{\text{internal terminal voltage \%}}{\text{external}}$