The ASDEX Upgrade UTDC and DIO cards - A family of PCI/cPCI devices for Real-Time DAQ under Solaris

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Abstract

A Universal Time to Digital Converter (UTDC) and a Digital I/O (DIO) card have been purpose-built for the new ASDEX Upgrade control system, the Thomson Scattering diagnostic, a renovation of the Magnetic Measurements, and a couple of other diagnostics requiring renewed timing or real-time features. The principal features of these cards are presented and it is shown how synergy in hardware and software development was achieved. Examples of actual usage in diagnostics are given. Measurements of the real-time behaviour of cPCI based diagnostics show low jitter of the Solaris operating system and highly reliable operation under moderate real-time conditions. Future applications of this family of cards are foreseen.

Keywords: PCI/cPCI digital I/O, FPGA controlled DAQ, real-time Solaris

1. Introduction

UTDC stands for Universal (or may be Unlimited:-) Time to Digital Converter. Its development was carried out in 2001 to 2004 as a joint project between the ASDEX Upgrade and W7X Control and DAQ groups. The actual design and production was done by UCS a commercial contractor. In the meantime the new timing system of ASDEX Upgrade has been launched [1] and a series of these UTDC cards are in operation in several real-time systems and conventional diagnostics. On request a cPCI redesign of the UTDC has been done and a series of cPCI devices is under production. The detailed function of the UTDC as a device to measure time, to generate complex conditional trigger patterns, and to receive and distribute events through the timing network is described in [2].

When the Magnetic Measurements diagnostic at ASDEX Upgrade came up with a real-time data readout requirement for their magnetic field integrators, we were looking for an appropriate digital interface which could be adapted into the crate -based architecture of the integrator electronics used since the first days of ASDEX Upgrade in the

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early 1990s. (The old method of measuring the Magnetic field was to digitise the $\dot{B}$ signal from the coils, integrating it digitally, and converting the digital result to an analogue value to be measured by a conventional CAMAC module. This was the only method available at that time since handling the complete data stream digitally was impossible or too expensive.) - A first effort in 2002 to build a digital serial interface into the integrators was put aside in 2003, when the idea came up to take the ingredients of the UTDC development and to interpret their function as a flexible digital I/O device which would not only serve this particular purpose, but could also be used in more cases just by reprogramming the internal logic.

2. Design features of the DIO

DIO- and UTDC-cards are made in principle out of the same building blocks: a PCI-controller, a Field-Programmable Gate Array (FPGA) and a series of I/O line drivers. The hardware design has become this simple, because most of the logic which formerly had to be placed in separated ICs onto a specialised printed circuit layout is now a collection of software modules in the FPGA. This state of the art principle was applied to the TTE device development for W7X [3] as well as for the UTDC design.

While the UTDC was designed with the specialised TDC requirements and function groups in mind, for the DIO design an even more generalised FPGA-based approach was chosen. To illustrate this Fig. 1 gives the block structure of the DIO-board.

The central component is the FPGA (Altera Cyclone). Its main logical units are various control and I/O registers, a Cycle Control Machine (CCM) along with its program memory, and input and output FIFOs. The CCM is implemented as a RISC machine with a 20 ns cycle, fast enough to manage a data flow of up to 10 Mbytes/s.

32 pins of the FPGA are connected to a series of low voltage differential signal (LVDS) line drivers, which can be used bidirectionally. These 32 bits (max. 8 control bits, 8 address bits, and 16 data bits) together with additional power and ground lines are lead through to a 68-pin SCSI connector forming the physical interface. This flexible programmable

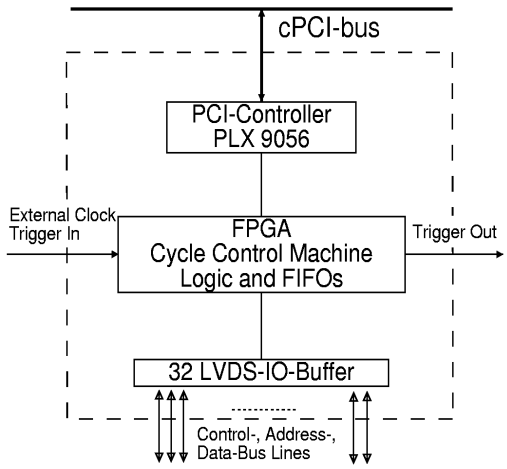

Fig. 1: Block diagram of the DIO-boards functional elements. The dashed line denotes the PCI card as a physical unit.

digital I/O interface must be adapted e.g. to the magnetic measurement internal digital device bus, but can as well be adapted to a variety of other digital interfaces. The flexibility is achieved through the CCM logic which will run small assembler like programs implementing the desired timing and logical behaviour of the 32 I/O lines in parallel.

Additionally optional connections have been implemented in the FPGA: Trigger In, Trigger Out, ext. Clock, 16 LEDs out. These are accessible through a piggyback board, and allow visualisation of internal states and synchronisation of the DIO board operation with other external devices like e.g. DIO or UTDC boards.

The cPCI-interface of the DIO is based on a PLX 9056 PCI-controller. This controller maps the FPGA registers into a 16 kB space on the PCI-bus. Two available DMA channels are assigned to the input and output FIFOs of the FPGA.

3. Driver features of the DIO-board

To achieve synergy with the UTDC driver software the same PCI controller chip was chosen for the DIO. So both device drivers could be kept very similar and differ only in the addressable registers. In fact the UTDC driver implements a more specialised register model according to its function groups, while the DIO driver restricts itself to communicating via the PCI-controller with the

generalised FPGA logic. For the UTDC board device drivers are available for VxWorks, Solaris, LINUX, and Windows. For the DIO board presently only Solaris and VxWorks drivers are operational, but it is expected that deriving the other versions from the respective UTDC drivers will be straightforward.

4. A diagnostic set-up with both DIO and UTDC

Fig. 2 shows how both cPCI-boards are integrated into the final set-up for the magnetic measurements diagnostic at ASDEX Upgrade. The upper dashed block is a computer like a "commodity" Sun PCI-bus based server SunFire V240. This server comes with two SPARC processors and 3 PCI-slots and provides a hardware architecture which is free of major bottlenecks.

The dashed block below is the cPCI-crate to house the cPCI-devices. The cPCI-crate is attached to the computer by a National Instruments PCI to cPCI (MXI-3) bridge with a fibre optic link between both parts. This easily solves possible problems when setting-up systems with multiple computers and many measuring channels.

The third dashed box is the crate of the legacy integrators, which have to be interfaced to the computer. This crate houses up to 8 integrators which use an internal data bus which is fed out to the DIO interface via a bus adaptor card.

Additional DIO boards in the cPCI crate can be used if more than one group of daisy chained measuring crates must be handled by one computer. One UTDC board per system is foreseen to synchronise the measuring process with the exact experiment time, time-stamp the measured samples in succession, and possibly generate a chain of external clock impulses for the data acquisition.

5. Real-time data acquisition with the DIO

Let me draw an idealised view of how all these parts operate together in real-time. To start and run the DAQ the system parts have to be initialised in a couple of steps before all parts are armed, running interrupt driven or in polling mode, and ready to transport data from the inputs to computer memory:

1) The CCM program memory has to be loaded with the appropriate CCM sequence.

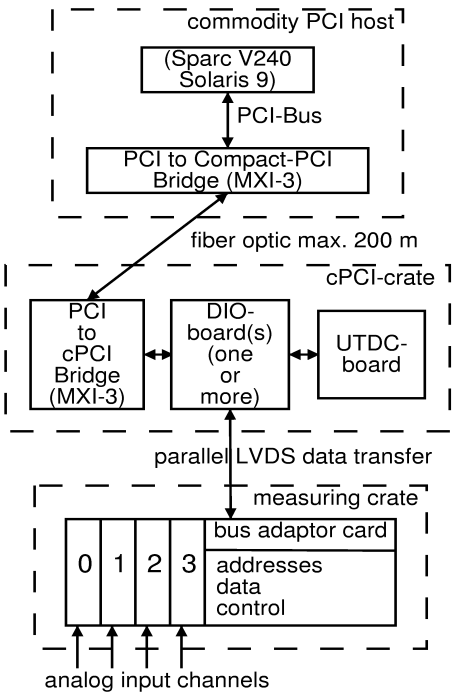

Fig. 2: A full diagnostic hardware set-up with one or more DIO boards and a UTDC timing module.

2) The integrators have to be reset in an early stage of the plasma discharge.
3) The planned time behaviour for the data acquisition has to be initialised which may comprise the download of a particular trigger generator program into the UTDC.
4) The DIO logic has to be initialised to a state where an external trigger can cause one CCM program cycle to run through which may result in reading one integrator value (or all at once) into the FIFO.
5) The computer has to allocate a memory section to receive the measured samples and a DMA has to be initiated which is suitable to transport any data from the PCI-devices into the allocated computer memory.

When these steps are finished the system is ready to receive an external trigger at one of its Lemo sockets or a trigger event via the UTDC timing network – depending on the actual settings-. If triggered, each part will start its activity. The front end part of the integrators will operate as always, the DIO will intercept the back end of the integrators

and divert a data-flow from this bus into its input FIFO independently. The DMA logic of the computer will transfer any incoming data from the FIFOs into the computer memory as it appears. Thus the measured $\dot{B}$ values (and possibly the corresponding time-stamps) appear in the computer memory without causing a noticeable load on the CPU in real-time. Following the DMA pointer a real-time analysis program will be able to evaluate the incoming data stream and forward selected results to other processes if required.

6. The real-time DAQ behaviour of Solaris

To make sure that this real-time DAQ scenario works under the Solaris operating system, we investigated the timing behaviour of the real-time Thomson Scattering diagnostic at ASDEX Upgrade. The set-up of this diagnostic is similar to the configuration described in that a cPCI-crate is connected to a SunFire V240 via a NI MXI-3 bridge in just the same way. The cPCI in this case contains a series of digitisers which deliver a burst of 8000 data samples taken within 500 ns. These bursts are read into computer memory via DMA periodically every 8 ms. The over-all action (DMA transfer, resetting and rearming the digitisers, re-initialisation of a new DMA, and a short on-line calculation) in total took between 1.95 and 2.33 ms. So the real-time task showed - compared to the expectations - very little jitter and absolute reliable real-time behaviour. Which means the expectation to finish this part of the real-time task within a given time horizon of 2.5 ms would have never failed and would leave another 5.5 ms for more detailed calculations and communication. (Of course the time horizon for each real-time task has always to be wide enough.)

7. Further applications and possible extensions

The flexibility of the DIO parallel interface which is based on three features, first the realisation of the complete logic in an FPGA, second the implementation of the Cycle Control Machine to control the full timing of the I/O-bus, and third the independent and flexible configuration of each I/O pin, makes it easy to adapt the DIO cPCI-card to various parallel and even serial applications.

Just by reprogramming the FPGA the implementation of a second version of a Transputer I/O board was achieved. This TPIO2 board features 16 bidirectional full duplex serial Transputer links to adapt the new control system to parts of the old still existing Transputer link based control periphery. Each of these 32 serial lines provides a throughput up to 10 Mbits/s.

Currently under consideration is the implementation of a PCI interface to the legacy CAMAC controllers still existing at ASDEX Upgrade. The approximately 100 CAMAC crates in operation are currently controlled by legacy Sun workstations using S-Bus interfaces. Because of their age these Suns will have to be replaced in the near future.

Providing about 10 MBytes/s average communication power the DIO seems well suited as an interface to other hardware developed for a particular purpose e.g. ADCs, device control units, etc.

8. Summary and outlook

With the DIO development based on the UTDC design, together with its variety of generalised operating system device drivers, the project ASDEX Upgrade has a tool box of digital devices at hand which enable real-time DAQ for nearly all diagnostics. Together with the further development of the ASDEX Upgrade control system and the extended collaboration between control and DAQ this will support ambitious future plasma control scenarios.

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