MAX-PLANCK-INSTITUT FÜR PLASMAPHYSIK

GARCHING BEI MÜNCHEN

Selector Channel Universal Interface Module
(S E L U M)

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GENERAL

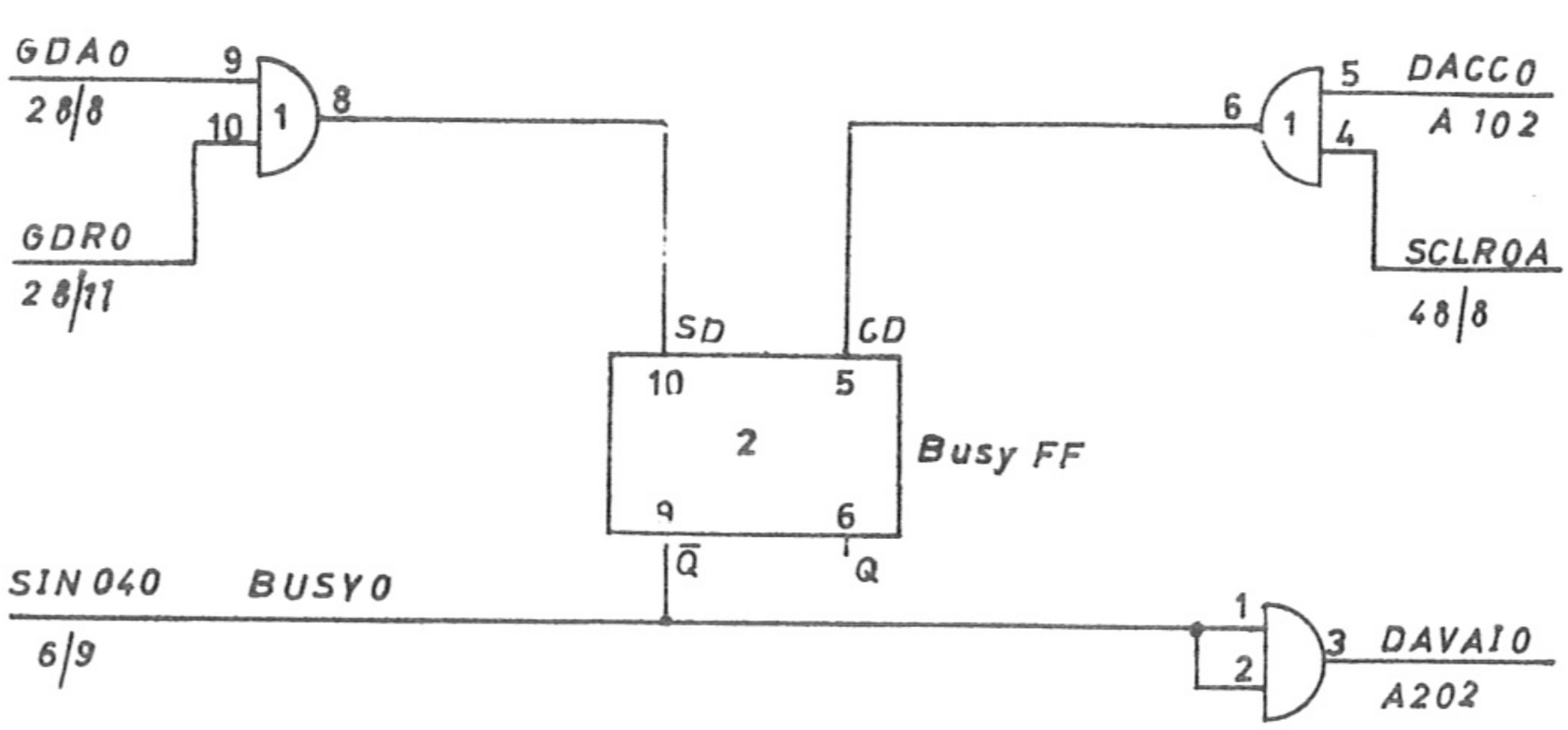
This paper describes an interface module (SELUM) with which special devices for which data transfer in genuine cycle stealing mode is appropriate can be connected to Interdata mini-computers. The module is a modified version of a universal interface module supplied by Interdata and can be operated either on the selector channel (for cycle stealing transfer) or on the normal multiplex channel. Due attention was paid in development to symmetry of the input and output signals so that processor-processor couples can also be performed with this interface.

1. Description

The basic component is the universal interface module (M48-oo9) of Interdata. This module already contains the necessary address logic, interrupt logic and the command decoder for the processor side and a buffer for the data output. For operation on the selector channel (M7o-1o3), however, there is no automatic setting and resetting of the busy bit in the status register. Fitting a flip-flop to the module for the busy bit makes it suitable for operation on the selector channel. The output of this flip-flop also serves as an output signal for the state "Data Available" in data transfer from the processor to the device, and conversely as a signal for the readiness of the processor to accept data from the device.

This flip-flop can be reset by the device by means of the signal "Data Accepted". This allows data transfer to be performed.

2. Circuit modification

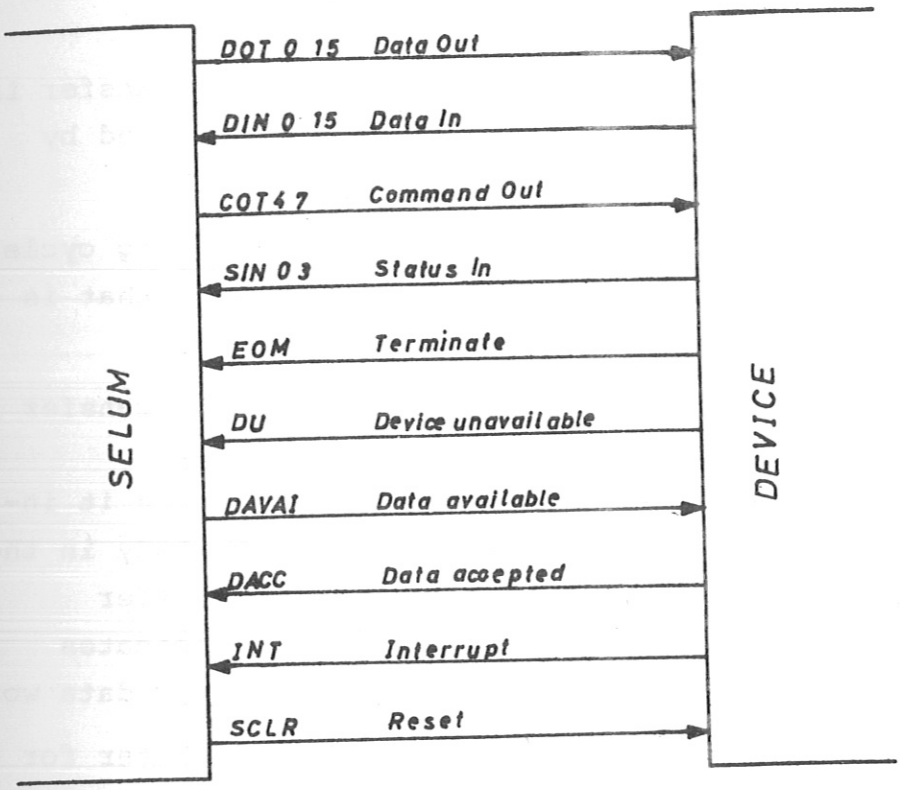


IC Nr.1 SN 7408

IC Nr.2 MC 845 P

These two integrated circuits can readily be fitted to the module near the connector "A". All that then need be done to the module is to separate the two lines to the connector "A", A 1o2 and A 2o2, and connect the two new signals Data Available (DAVAIO) and Data Accepted (DACCO) to the pin connector. The figures at the other signals refer to the IC No. with the respective pin No. on the universal interface module.

3. Output signals of SELUM



4. Explanation of signals

DOT = output data from SELUM to device (16 bits)

DIN = input data from device to SELUM (16 bits)

COT = command bits from SELUM to device. These bits can be set by the program with an output command (OC) to put the device in a certain state (4 bits)

SIN = status bits from device to SELUM. With these bits it is possible to read status information

from the device by means of a sense instruction (e.g. SSR). These are bits o - 3 in the sense byte.

Terminate (EOM) = This signal can terminate a data transfer in cycle stealing mode. This is indicated by setting bit 6 in the sense byte.

Device Unavailable (DU) = This signal also terminates a running cycle stealing transfer, but it is bit 7 that is set in the sense byte.

DAVAI (Data Available) = This signal is applicable to both transfer directions.
In transfer from SELUM to the device it indicates when a new data word is ready in the output register. In the other transfer direction, device to SELUM, it indicates when SELUM is ready to accept a new data word.

DACC (Data Accepted) = This signal confirms the data transfer for a word. It is applicable to both transfer directions.

INT = This interrupt signal initiates an interrupt in the processor if interrupts are enabled in the PSW and SELUM under program control.

SCLR = system clear and reset. This signal can reset the device to a defined initial state. It is produced by depressing the INT key on the operator control panel of the computer.

5. Pin assignment and signal levels

CONNECTORS		
J2	P1	PinNr.
DINooo	GND	o1
INTo	GND	o2
SCLRoB	DUo	o3
COTo7o	EOMo	o4
COTo6o	DACCo	o5
COTo5o	DAVAIo	o6
COTo4o	SINo3o	o7
DOT15o	SINo2o	o8
DOT14o	SINo1o	o9
DOT13o	SINooo	1o
DOT12o	DIN15o	11
DOT11o	DIN14o	12
DOT1oo	DIN13o	13
DOTo9o	DIN12o	14
DOTo8o	DIN11o	15
DOTo7o	DIN1oo	16
DOTo6o	DINo9o	17
DOTo5o	DINo8o	18
DOTo4o	DINo7o	19
DOTo3o	DINo6o	2o
DOTo2o	DINo5o	21
DOTo1o	DINo4o	22
DOTooo	DINo3o	23
GND	DINo2o	24
GND	DINo1o	25

The pin assignment here conforms to the description in the Instruction Manual for the Universal Interface Module (M48-oo9), Publication No. 29-273, except for the connection of P1 pin No. o3 - o5. The levels of the signals are equal to the normal DTL level.

Log 1 = o volt

Log o = 5 volt

R e f e r e n c e s :

(1) Universal Interface Modul Instruction Manual 29-273

(2) Interdata User's Manual 29-261RO1