A CMOS BIOSENSOR ARRAY FOR MEASURING CELLULAR EXOCYTOSIS

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Release of neurotransmitters and hormones from secretory vesicles plays a fundamental role in the function of the nervous system including neuronal communication. High-throughput testing of drugs modulating transmitter release is becoming an increasingly important area in the fields of cell biology, neurobiology, and neurology. In this thesis, I will describe the design and operation of a novel CMOS potentiostat circuit that is capable of measuring transient amperometric oxidation currents at the surface of an electrode with submillisecond time resolution and picoampere current resolution. In designing an array of such potentiostats, a shared amplifier scheme is employed, reducing the layout area of each unit in half, enabling high density and improved spatial resolution. In order to perform electrochemical experiments on the CMOS chip, an on-chip transducer was required. I will describe two post-CMOS fabrication methods to incorporate the electrochemical transducer material. I will present results from various experiments, that prove the feasibility of on-chip electrochemical measurements of dopamine, and catecholamine release from live adrenal chromaffin cells with sub-picoampere current resolution and sub-millisecond time resolution. I will also present system-level architecture of a high-throughput biosensor array that is capable of monitoring catecholamine release at a rate hundred times faster than the existing technology, and at one-tenth the cost.

BIOGRAPHICAL SKETCH

Sunitha B. Ayers was born on October 14, 1979 in Hyderabad, Andhra Pradesh, India. As an undergraduate, she attended the National Institute of Technology, Warangal, graduating with distinction in Electrical and Electronics Engineering in 2001. From 2001-2002, she attended Cornell University and received her M. Eng degree. She continued her graduate studies at Cornell University and received her Ph. D. in January of 2009.

In memory of Professor Peter Krusius (1944-2003).

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CHAPTER 1

INTRODUCTION

Research in human health relies on development of new techniques that enable us to observe, identify, and quantify various biological phenomena. The advent of biosensor arrays promises to bring about rapid changes in the field of medical research. Biosensors are analytical platforms that convert biological signals to detectable electrical signals. Biosensor arrays are miniaturized, high-throughput systems that can generate the large amount of data required to determine statistical significance of a biological response. Biosensors are generally highly scaleable, offer cost effective and less time consuming alternatives to traditional experimental methods. Biosensors involve different sensing methodologies which include optical, electrochemical, thermal, magnetic, mechanical, and piezoelectric transduction. Biosensors are now being used to solve a wide variety of analytical problems in medicine, drug discovery, defense, environment, and in-vivo measurements [1–5].

Monitoring real time sub-second processes, such as release of neurotransmitters present additional challenges in biosensor array design. Development of a biosensor array involves consideration of three main design issues:

- Biosensors typically measure very low level signals, picoampere currents and microvolt voltage changes over a millisecond timescale. The experimental conditions make the system more susceptible to external noise. The designer must consider these factors when choosing design specifications and criterion.
- Integration of the electronics and signal acquisition systems and transducers present fabrication and packaging challenges. The layout must be designed with processing and handling issues under consideration.

- High-throughput arrays also present a challenge in data analysis. Special software systems and algorithms should be developed to automatically reconstruct the currents for the individual electrodes and analyze the data.

1.1 Outline

This work involves the design of a novel biosensor system and integration of the CMOS electronics with the transducer.

In Chapter 2, I will describe the fundamentals of cell biology for the benefit of the non-biologists. Exocytosis and its impact on human health will be discussed. I will explore the advantages of using a CMOS biosensor array over the traditional methods of monitoring exocytosis.

In Chapter 3, I will describe the the MOS device channel current expressions and important incremental device characteristics for the non-circuit designers. I will also list some practical guidelines for successful chip design.

In Chapter 4, I will describe the circuit-level operation of a novel potentiostat circuit. I will describe how this design is superior to other potentiostat circuits in terms of low-frequency gain, stability, bandwidth, and output swing. Noise analysis will be described and techniques to reduce noise will be discussed. I will also describe how correlated-double sampling is achieved. The results of electrical measurements will be provided along with the performance specifications of the circuit.

In Chapter 5, I will describe the fabrication of the electrochemical transducer, which, in this case, the deposition of polarizable electrode on a standard CMOS

chip. Two methods were used for post-CMOS fabrication: focused-electron-beam deposition of platinum and thermal evaporation of gold using photolithography. Packaging methods suitable for performing on-chip electrochemical experiments will be described. I will present experimental results of electrochemical sensitivity of the chip from measurements of dopamine and catecholamine release from live bovine chromaffin cells.

In Chapter 6, I will describe system-level architecture of a fully electronic hybrid chip, that comprises of a eight-electrode linear array and a 100-electrode 2-D array. I will discuss the operation of a bias current generator that is capable of generating bias currents from subthreshold to above-threshold levels. I will also describe a timing scheme to generate the switching signals. Finally, I will present the simulation results and performance specifications expected from the hybrid chip.

In Chapter 7, I will summarize the work done on developing the biosensor, the results achieved and propose improvements to the CMOS biosensor.

REFERENCES

[1] Jenkner, M., Tartagni, M., Hierlemann, A., Thewes, R., "Cell-based CMOS sensor and actuator arrays," *IEEE Journal of Solid-State Circuits,* vol. 39, no. 12, pp. 2431-2437, 2004.

[2] Eversmann, B., Jenkner, M., Hofmann, F., Paulus, C., Brederlow, R., Holzapfl, B., Fromherz, P., Merz, M., Brenner, M., Schreiter, M., Gabl, R., Plehnert, K., Steinhauser, M., Eckstein, G., Schmitt-Landsiedel, D., Thewes, R., "A 128x128 CMOS biosensor array for extracellular recording of neural activity" *IEEE Journal of Solid-State Circuits,* vol. 38, no. 12, pp. 2306-2317, 2003.

[3] Schienle, M., Paulus, C., Frey, A., Hofmann, F., Holzapfl, B., Schindler-Bauer, P., and Thewes, R., "A fully electronic DNA sensor with 128 positions and in-pixel A/D conversion" *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2438-2445, 2004.

[4] Milgrew, M. J., Riehle, M. O., Cumming, D. R. S., "A 16x16 CMOS Proton Camera Array for Direct Extracellular Imaging of Hydrogen-Ion Activity," *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International,* pp. 590-638, Feb. 2008.

[5] George S. Wilson, Raeann Gifford, "Biosensors for real-time in vivo measurements," *Biosensors and Bioelectronics, 20th Anniversary of Biosensors and Bioelectronics,* vol. 20, no. 12, pp. 2388-2403, 2005.

CHAPTER 2

ION CHANNEL FUNCTION AND TRANSMITTER RELEASE

All functions of the nervous system, including sensory perception, learning, and memory, require nerve cells to communicate with each other through synaptic transmission. In this process of synaptic transmission, neurotransmitters are released from the presynaptic terminal and act on the postsynaptic membrane [1]. In synaptic transmission through *exocytosis*, synaptic vesicles fuse with the presynaptic membrane and release neurotransmitters into the synaptic cleft. Exocytosis occurs along two pathways: *constitutive* exocytosis and *regulated* exocytosis. Constitutive exocytosis requires no external signals, maintaining the continuous balance of lipids and proteins between the plasma membrane and the extracellular environment. Regulated exocytosis rapidly secretes products such as hormones, neurotransmitters, and digestive enzymes on demand, in response to specific stimuli, primarily through increased calcium ion concentration [2]. Regulated exocytosis, illustrated in Fig. 2.1, occurs in three trafficking steps: neurotransmitter-filled vesicles dock at the presynaptic membrane, the docked vesicles undergo priming to become fusion components, and the primed vesicles undergo rapid exocytosis in response to the action-potential-induced Ca^{2+} influx [3].

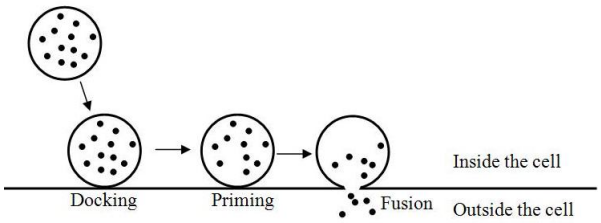

Figure 2.1: An exocytotic event. Vesicles packed with neurotransmitters and hormones fuse with the plasma membrane to release their contents to the outside in three trafficking steps: docking, priming and fusion.

A multi-step process facilitates regulated exocytosis following nerve stimulation [4]. The multi-step process involves the opening of the voltage-dependent ion channels, the generation and conduction of an action potential, and finally the activation of fusion machinery, leading to regulated exocytosis. This chapter introduces the cellular processes behind exocytosis, fusion process, methods of detecting release, and the need for microarray technologies to advance drug research and understanding of neuronal communication.

2.1 Cell Membrane

The cell membrane, which is also called the plasma membrane, separates the inside of the cell from the outside. The membrane is a diffusion barrier between the intracellular and extracellular space with specific transport properties, preventing the loss of vital cellular components through diffusion, but allowing specific solutes across the membrane. The basic structure of biological membranes is formed by *lipids* while *proteins* perform specific functions of the membrane, although recent experiments suggest that proteins form a greater percentage of the membrane area [5]. The universal basis of the cell structure, illustrated in Fig. 2.2, is the lipid bilayer. Lipids are fatty molecules that form 50% of the membrane in most animal cells while the rest of the membrane consists mostly of protein [2]. Lipid molecules have hydrophilic heads and hydrophobic tails. Transmembrane proteins have hydrophobic regions that pass through the membrane and hydrophilic regions that are exposed to the aqueous environment on either side of the membrane. Nonpolar, uncharged polar molecules, and urea diffuse across the bilayer; however, lipid bilayers are highly impermeable to ions due to their charge and degree of hydration.

Transport proteins transfer small molecules across the membrane. Proteins act as receptors for hormones and other signaling molecules and mediate the transport of signaling molecules across the membrane. Each protein transports molecules of particular class including ions, sugars, and amino acids. Transport proteins can be categorized into *carrier* proteins and *channel* proteins. Carrier proteins bind to specific solutes and undergo a variety of conformational and functional changes to transport the solute across the membrane. Channel proteins form aqueous pores that open across the lipid bilayer, allowing solutes to pass through. Transport through the pores is much faster than carrier mediated transport. The transport of solutes through channels and carriers down the concentration gradient is called *passive* or *downhill* transport. Pumps transport molecules against the electrochemical gradient, called *uphill* or active transport. The energy required to pump the transfer of molecules against the gradient is supplied by carrier-protein mediated ATP hydrolysis. Thus, transport by carriers can be either passive or active, while transport by channels is always passive.

Channel proteins that specifically transport inorganic ions are called *ion channels*. The transport efficiency of these channels is 10^5 times greater than carrier-mediated transport [2]. Ion channels are macromolecular pores in cell membranes and are the fundamental excitable elements of the membrane. The specific inorganic ions K^+, Na^+, Ca^{2+}, and Cl^- diffuse across the membrane to form the electrical signal in the form of an *action potential*. Understanding the electrical properties of the cell membrane is essential to understand the electrical excitability of cells. In the following sections, the electrical properties of the cell membrane, the properties of ionic channels and their role in receiving, conducting, and transmitting electrical signaling will be discussed.

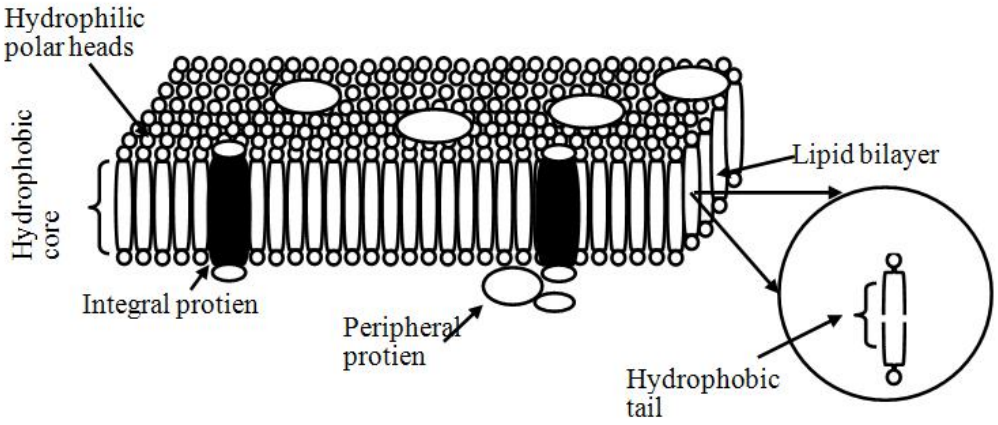

Figure 2.2: The structure of the cell membrane. A Section of the cell membrane consisting of a lipid bilayer and protein. Lipids have outer hydrophilic head groups in contact with water on either side of the membrane and the middle contains hydrophobic tails (inset). Lipids make up almost 50% of the membrane and the rest comprises of proteins.

2.2 Electrical Properties of the Membrane

Cell membranes store potential energy in the form of electrochemical gradients caused by ionic concentration differences across the lipid bilayer. This energy is used to drive various transport processes. The flow of ions through a channel is driven by the electrochemical gradient for that ion. If an ion is moving across the cell membrane, whose voltage inside the cell is V_i relative to the voltage outside the cell V_o, the energy change is given by

$$E_\mathrm{i} - E_\mathrm{o} = ze_0V \tag{2.1}$$

where z is the valency of the ion, e_0 is the charge of an electron, and V is the transmembrane voltage. A movement of the ions down the concentration gradient also generates an energy change given by

$$-kT \ln \frac{c_\mathrm{o}}{c_\mathrm{i}}$$

where c_o is the concentration of ions outside the cell membrane, c_i is the concentration of ions inside the cell membrane, k is the Boltzmann constant. At a voltage V_N, called the Nernst potential, there is a balance of the two energy gradients and no net flow of ions through the channels.

$$ze_0V - kT\ln\frac{c_o}{c_i} = 0 \tag{2.2}$$

$$V_N = \frac{kT}{ze_0}\ln\frac{c_o}{c_i} = \frac{RT}{zF}\ln\frac{c_o}{c_i} \tag{2.3}$$

where R is the gas constant, and F is the Faraday's constant. For every ion, there is a Nernst potential; for instance, the intracellular concentration of K^+ in most animal cells is 140 mM and the extracellular concentration is 5 mM and thus the equilibrium potential of potassium is about -90 mV. Similarly, there is a Nernst potential for sodium ions, for chloride ions, and for the various other ions in the cell.

The ionic solutions on either side of the insulating lipid bilayer form a capacitor. The specific capacitance of the biological membranes is about 8-10 $fF/\mu m^2$. The specific conductance of the membrane is 4 nS/cm^2 [2]. The plasma membrane area of many types of cells is 300-3000 μm^2, which corresponds to a conductance of 12-120 fS. Different ion channels add unique voltage-gated conductances to the cell membrane. The electromotive force that drives ions through a specific ion channel is the difference of the membrane voltage and the Nernst potential of that particular ion. The equivalent circuit of the cell membrane, deduced by Alan Hodgkin and Andrew Huxley by studying the membrane properties of a giant squid axon, called the Hodgkin-Huxley model is illustrated in Fig. 2.3(b). Different ionic channels are selective/permeable to different ions, but not perfectly selective. For example, Na^+ ion channel is slightly permeable to K^+ ions [6]. An important subset of K^+ ion channels, called K^+ leak channels are open even in an unstimulated state.

These leak channels serve the purpose of making the membrane more permeable to K^+ ions and maintaining the membrane potential across all plasma membranes. The reversal potential of the membrane or *zero current potential* is the voltage of the membrane at which the sum of currents in the ionic branches of Fig. 2.3(b) is zero. The reversal voltage at which the current reverses direction is given by the Goldman-Hodgkin-Katz equation [6–10] given by

$$E_{\text{rev}} = \frac{RT}{F} \ln \frac{P_{\text{K}}[K]_{\text{o}} + P_{\text{Na}}[Na]_{\text{o}} + P_{\text{Cl}}[Cl]_{\text{i}}}{P_{\text{K}}[K]_{\text{i}} + P_{\text{Na}}[Na]_{\text{i}} + P_{\text{Cl}}[Cl]_{\text{o}}} \tag{2.4}$$

where P_{S} is permeability of the ion S defined as

$$P_{\text{S}} = \frac{\beta_{\text{S}} D_{\text{S}}}{\Delta x}.$$

Permeability is dependent on the diffusion coefficient of the ion, D_{S}, in the membrane, the partitioning coefficient of the ion S (relative area of the membrane that is permeable), and the portion of the membrane. The equation is derived from the diffusion theory of ions and makes assumptions about the structure and shape of the pores in the membrane. The Goldman-Hodgkin-Katz equation resembles the Nernst equation; however, it describes the steady-state interdiffusion of several ions under non-equilibrium conditions. In resting neurons, the membrane is most permeable to K^+ ions, so the reversal potential is very close to the Nernst potential of K^+ ions. A compact electrical equivalent of the resting neuron is illustrated in Fig. 2.3. Changes in permeability of ion channels mediate the generation and propagation of action potentials.

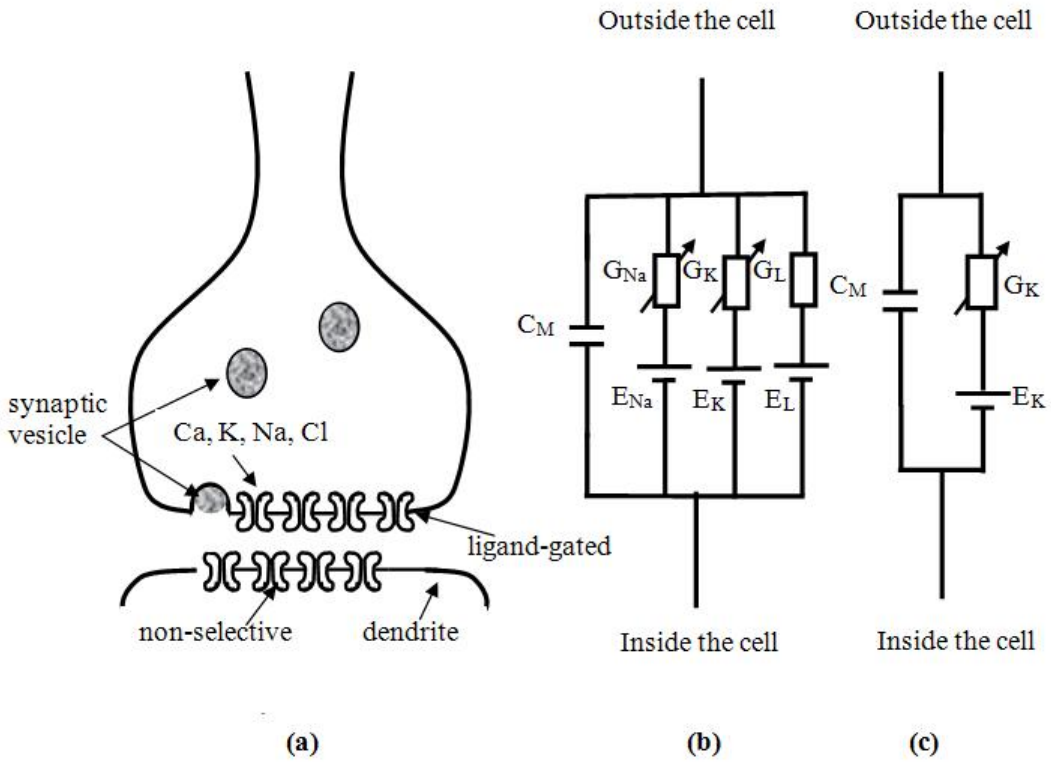

Figure 2.3: Hodgkin-Huxley equivalent circuit of the cell membrane. (a) The cell membrane of both the presynaptic cell and the postsynaptic cell consists of lipid bilayers and various ion channels. The lipid bilayers form an electrical capacitor while the fusion pore and the ion channels contribute to the membrane conductance. (b) The Hodgkin-Huxley model of the of the cell membrane along the length of the axon. G_{Na}, G_K, G_L are the conductance of the sodium, potassium and leak channels; E_{Na}, E_K, E_L are Nernst potentials of the Na^+, K^+, and leak channels respectively. The arrows indicate a nonlinear conductance arising from the opening and closing of voltage gated ionic channels. (c) Compact model of the resting cell membrane. The pores of the membrane in all excitable cells are highly permeable to K^+ ions. Therefore the resting potential of the membrane is close to the Nernst potential of the K^+ channel.

2.3 Action Potential

The concentrations and Nernst potentials of ions in most cells is given in Table 2.1. The measured resting potential of most cell membranes is about -70 mV. In response to a stimulus, the membrane potential is *depolarized*, i.e., the membrane potential is increased and the sodium channels open. There is a negative concentration gradient for sodium ions inside the cell with respect to the outside. Therefore, Na^+ ions flow into the cell and reduce the electrochemical gradient. This influx of positive ions depolarizes the membrane further and more Na^+ ions enter into the cell. This process continues until the Na^+ equilibrium potential of about +50 mV is reached. At this stage, the net electrochemical gradient of sodium ions is zero, causing the channels to inactivate while the cell membrane remains depolarized. The cell returns to its resting state from this state through the delayed activation of potassium channels. There is a positive concentration gradient of K^+ ions across the membrane. Voltage gated K^+ channels open and an exodus of the K^+ ions *repolarizes* the membrane. The voltage gated potassium channels open before the Na channels are inactivated, but with slower kinetics. This electrical pulse of the membrane (Fig. 2.4), is called an action potential.

Table 2.1: Ionic concentrations and Nernst potentials of most animal cells.

Ion	**Intracellular Concentration (mM)**	**Extracellular Concentration (mM)**	**Nernst Potential (mV)**
$\mathbf{Na^+}$	5-15	140	84-56
$\mathbf{K^+}$	140	5	-84
$\mathbf{Ca^{2+}}$	10^{-4}	1-2	116-125
$\mathbf{Cl^-}$	5-15	110	(-78)-(-50)

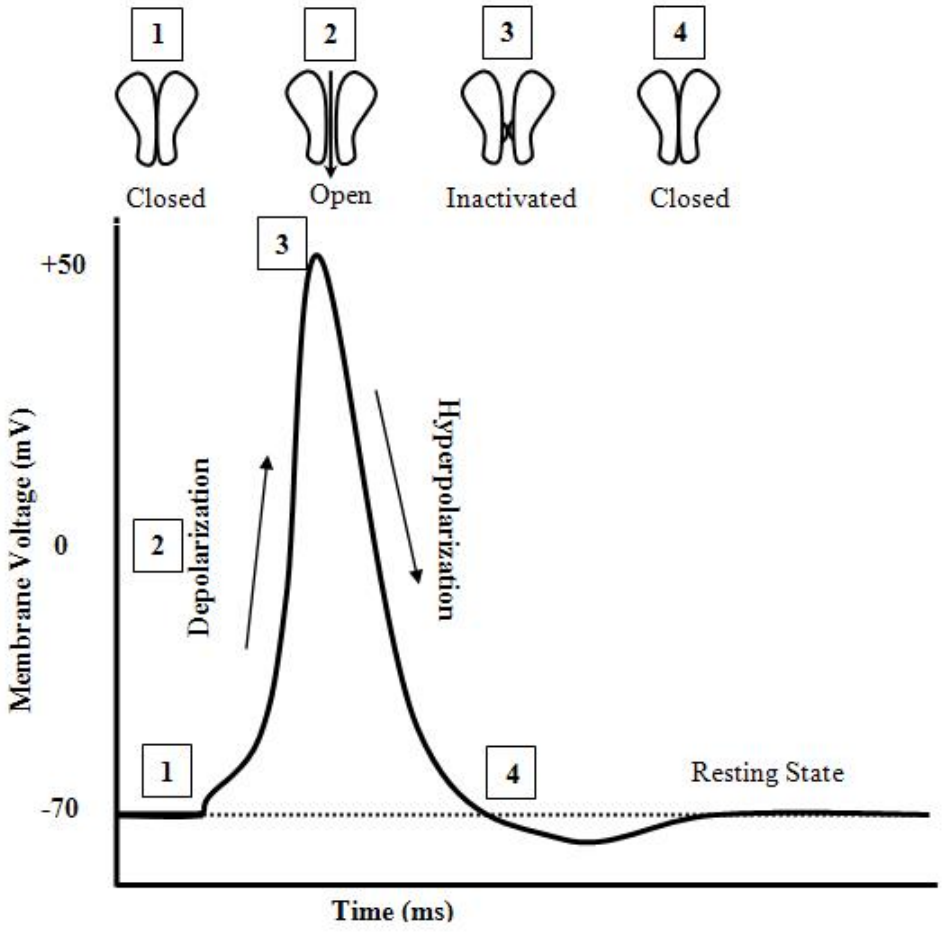

Figure 2.4: Action Potential. A action potential goes through four stages: 1-4. In the first stage, the membrane potential is increased from its resting potential of -70 mV triggered by a stimulus. After sufficient depolarization, the voltage gated sodium channels open depolarizing the membrane further, indicated by stage 2. In the third stage, upon reaching the equilibrium potential of Na^+ ions, the sodium channels are inactivated. The cell is at a new resting state. Potassium channels also respond to the same depolarization along with the sodium channels but have slower kinetics. The delayed opening of potassium channels in stage 4 drives the membrane back to its original resting potential of -70 mV. At this stage the sodium channels close. The undershoot indicates increased K^+ permeability, which deteriorates.

2.4 Exocytosis

Action potentials or *impulses* are the electrical signals that mediate cell-to-cell communication. Depolarization that starts in the cell body propagates to the terminal dendrites along the axon as illustrated in Fig. 2.5. The propagation of the action potential proceeds in only one direction because Na^+ channels are inactivated in the other direction. The signal is self-generating and propagates to the end of the nerve terminal, because sodium channels along the axon respond to membrane depolarization, before the potassium channels bring the membrane back to the resting state. At the end of the nerve terminal, the message is passed on to a post-synaptic cell such as another neuron or a muscle cell. The message is not simply passed on by a continuous process of electric excitation, but there is an intervention of chemical transmitter, involving the release of various substances. The final transduction always has the following pathway [11]. On reaching the nerve terminals the action potential causes an influx of Ca^{2+} through voltage-gated Ca^{2+} channels. The ultimate response is then triggered by the Ca^{2+} ions. The Ca^{2+} ions bind to specific sensors that trigger the secretory vesicles to fuse with the plasma membrane and release neurotransmitters, neurohormones, digestive enzymes, etc. to the extracellular space. The receptors in the post synaptic cell recognize the released neurotransmitters, causing the postsynaptic cell membrane to depolarize. Thus, action potentials travel from one nerve cell to another through chemical transmitters released by regulated exocytosis of the presynaptic cell. In the peripheral nervous system, the nerve terminals release acetylcholine, which leads to subsequent action of the muscle. In the adrenal medulla, adrenaline and noradrenaline are released in response to a stimulus, which causes the "flight or fight" response. In the human brain, about 10^{11} neurons form 10^{14} synapses enabling responses that include speech, movement, hearing, and thought.

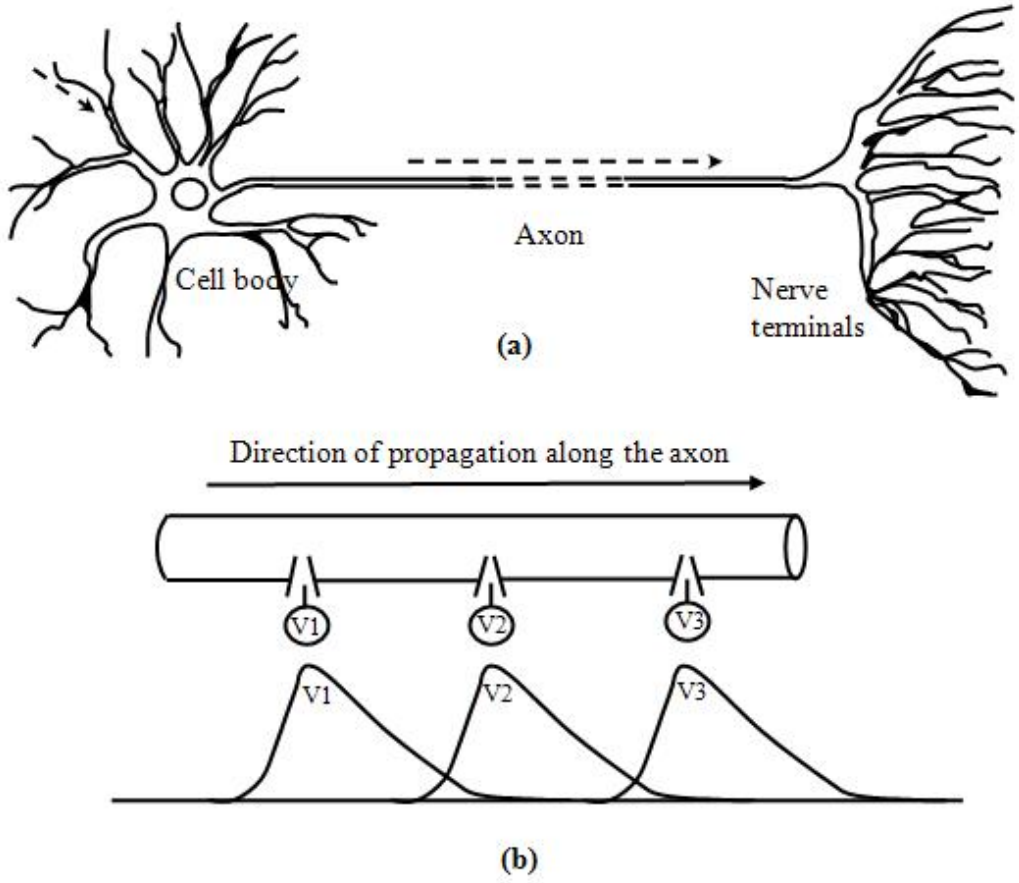

Figure 2.5: The progression of an action potential along a neuron. (a): A cartoon of a typical neuron. The axon of various cells varies from less than 1 mm to larger than 1 m in length. The action potential enters to the cell body through the dendrites of the cell near the cell body. (b): The arrow along the axon indicates the direction of propagation of the action potential. The action potential starts at the cell body and propagates to the dendrites/nerve terminal of the presynaptic cell along the axon. The direction of propagation is always along the axon to the nerve terminals because of the inactivation of the sodium channels in the direction of origin of the signal. Ionic currents immediately change the membrane potential, which makes the other voltage-gated channels in the membrane detect the change in membrane potential and in turn respond. Thus the action potential is regenerative and self-propagating.

2.5 Techniques for Observing Exocytosis

Cells that are specialized for secreting specific molecules store products in secretory vesicles, sometimes called dense-core vesicles. Neurotransmitter release occurs by the fusion of discrete, uniformly sized packets or quanta of transmitter molecules, that are stored in secretory vesicles [12]. Release occurs in multiples of unit quanta with quantal size being the response produced by the molecules from a single vesicle.

Molecules released by exocytosis are detected by several techniques. Biochemical approaches measure release response from populations of cells, providing great insights into the nature of the released molecules. Single-cell measurements provide spatial and temporal resolution, revealing a wealth of information about the fusion pore, the molecular machinery of exocytosis, and the release from single vesicles. There are three main experimental approaches that have been used to study exocytosis from single cells:

- Measurement of the post-synaptic response of the cell, such as the original work done by Katz et. al [12–14]
- Capacitance measurements: Membrane capacitance changes due to an increase in the membrane area during fusion of secretory vesicles are measured. The increase in capacitance of the whole membrane and of a single vesicle during fusion are measured under different configurations [15–17].
- Electrochemical detection: Currents generated by oxidation and reduction of released transmitter molecules when a polarizable electrode is placed in close vicinity are measured [18, 19].

- Optical techniques: Optical detection methods include total internal reflection fluorescence microscopy, membrane addition and pH changes [20].

In this section is a brief review of the technical aspects of the current techniques for observing exocytosis.

2.5.1 The Patch Clamp Technique

The patch clamp technique was developed by Erwin Neher and Bert Sakman, for which they received the Nobel Prize in 1991. The technique was subsequently employed in many laboratories worldwide to observe the properties of ion channels. The patch clamp technique also allows measurement of increased membrane area during the fusion event. Glass micropipettes of a few microns in diameter with fire-polished tips are used to patch the cell membrane. A pipette filled with salt solution is connected to a low-noise patch-clamp amplifier through an electrode. The bath solution in which the cell is immersed is grounded using an Ag/AgCl electrode. The pipette tip is brought to the cell surface and slight suction is applied to suck a portion of the cell membrane into the pipette. The suction forms an *omega patch* inside the pipette, as shown in Fig. 2.6(a). A seal is formed between the pipette interior and the bath solution. The formation of the seal leads to an increase of the electrical resistance between the electrode in the patch pipette and the electrode in the bath solution to several gigaohms, which is called *giga-seal*. This is the *cell-attached* configuration, which allows the measurement of the capacitance of the portion of the membrane patch inside the pipette. The patch may be broken by the application of increased vacuum force, leading to the *whole-cell configuration*, in which the pipette interior is connected to the cytoplasm and

the electrical properties of the entire cell membrane are measured. In addition to capacitance measurements, this configuration allows the cytoplasm to be diluted by altering the composition of the pipette solution, allowing the measurement of the effects of various solutes on exocytosis. In these recordings, the pipette access resistance contributes the largest component of noise in conjunction with the membrane capacitance. Thus, the noise in the cell attached recordings is significantly less than it is in the whole cell recordings. The electrical equivalent circuits of the cell-attached and whole-cell configurations are illustrated in Fig. 2.3(b)-(c). When a sine wave is applied to the pipette electrode, resistive and capacitive currents are detected by the patch clamp amplifier. Phase detection circuits separate the capacitive and the resistive elements of the current. True vesicle capacitance can be derived from these measurements [21]. During an exocytosis event, the cell membrane area is increased due to the addition of the vesicle membrane to the plasma membrane. Every fusion event produces a capacitance step, the size of which is determined by the fusion pore or area of the vesicle. Vesicles with diameters from 60 - 500 nm yield capacitance steps of 0.1 - 7 fF. The noise level of the recording equipment must be lower than the capacitance steps. The noise level in whole cell experiments is $\approx$2 - 3 fF rms [22], which makes measurement of single vesicle fusion difficult. Therefore, capacitance steps due to exocytotic fusion can be measured only using the cell-attached configuration. Several capacitance steps have been recorded successfully using the cell-attached configuration [15, 23, 24].

Two additional low-noise configurations are possible by pulling away the pipette from the cell in the cell-attached configuration and in the whole-cell configuration. A break of the patch from the cell attached configuration leads to the *inside-out* configuration, whereas a break of the patch from a whole-cell configuration leads to the it outside-out configuration. The outside-out configuration is similar to the

whole-cell configuration, but the noise is much lower because of the significantly reduced membrane area. In the inside-out configuration the interior of the cell is now replaced by the bath solution. A solution exchange of the bath or introduction of a different solution onto the patch by using a pipette facilitates the study of substance concentrations or of different ionic compositions on exocytosis. The patch clamp technique does not reveal the identity of the released molecules or provide spatial resolution. As we shall see, amperometry allows the detection of the released molecules.

2.5.2 Amperometry

In amperometry, the molecules released by the cell during exocytosis are electrochemically reduced or oxidized by a polarizable electrode and the current of the reaction is measured. From Faraday's law, we know that

$$Q = \int I dt = \frac{zFM}{N_{\mathrm{A}}} = zeM, \tag{2.5}$$

measurements can quantitatively reveal the number of molecules and the time dependence of their release. Here, Q represents the total charge involved in the redox reaction, which is obtained by integration of the current transient I; M represents the number of molecules reacted; z is the number of moles of electrons transferred per mole of compound reacted; F is Faraday's constant, 96,485 C/mol; N_{A} is Avogadro's number, 6.023×10^{23}; and e is the elementary charge 1.602×10^{-19} C.

A carbon-fiber electrode with a surface area of around 5 μm is a suitable polarizable electrode for recording amperometric currents from cells. Polarizable electrodes do not allow the free exchange of charge when immersed in a salt solution. Molecules that diffuse to the electrode held at the redox potential are

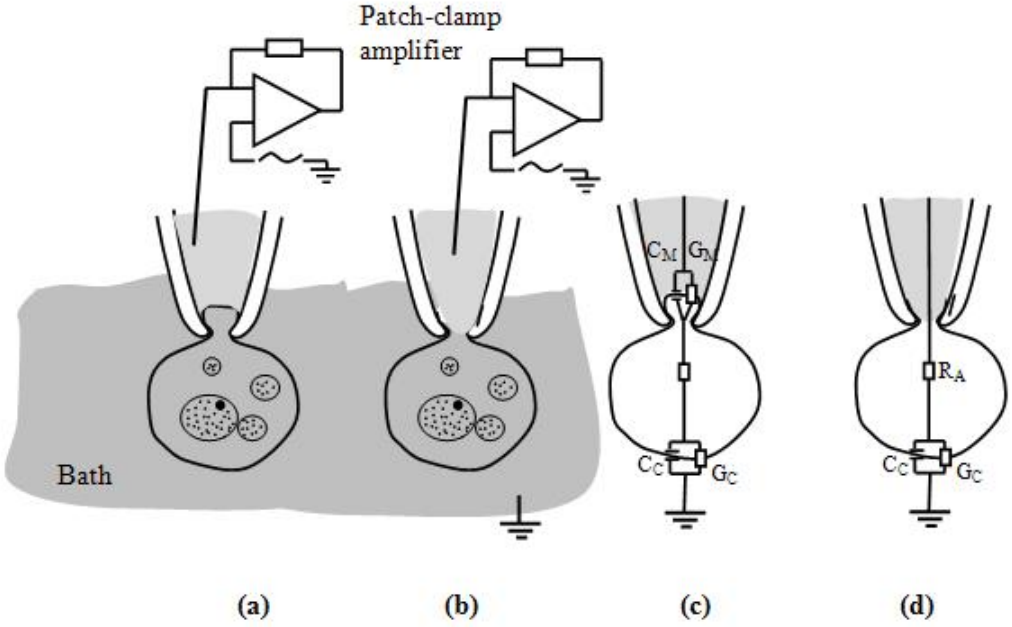

Figure 2.6: The patch clamp set-up. (a): The cell-attached configuration, where a pipette is placed on the cell and a gentle suction is applied. An omega patch is formed, as illustrated here. An electrode connected to a low-noise patch-clamp amplifier is placed inside the pipette. A Ag/AgCl electrode is placed in the bath solution and grounded. A sine wave is applied to the pipette electrode in reference to the bath electrode and the capacitive and resistive currents are recorded. (b): The whole-cell configuration, where the patch in the cell-attached configuration is broken and the cytoplasm of the cell is in contact with the pipette solution. Capacitance changes of the entire membrane are measured. (c): The equivalent circuit of a cell-attached setup. C_M is the membrane capacitance of the patch, G_M is the conductance of the patch, R_A is the pipette access resistance, G_C and C_C are the capacitance and conductance of the rest of the membrane. Membrane capacitance is much less than the rest of the capacitance, $C_M \ll C_C$, therefore C_C can be ignored. (d): The equivalent circuit of the whole cell setup is similar to the cell-attached setup, except for the components of the patch.

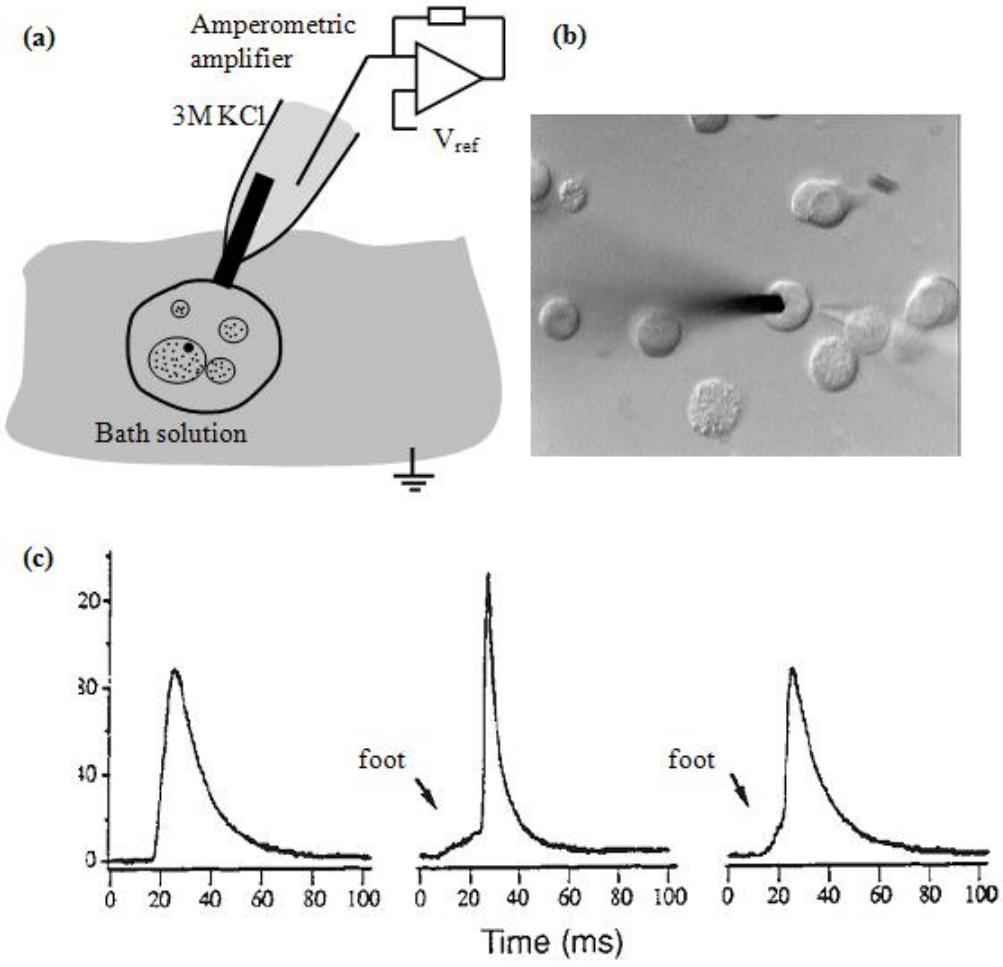

Figure 2.7: The amperometric set-up and recordings. (a): A carbon-fiber electrode (CFE) is placed against a cell sitting in a bath solution. The recording electrode is placed in a pipette is filled with 3M-KCl. The electrode is held at a reference potential of 700 mV by the amperometric amplifier. (b): An image of a CFE placed against a chromaffin cell. (c): Different amperometric transients, recorded from the secretion of chromaffin cells. The origin of the foot, the small transient increase preceding the spike shaped signal is not yet fully understood. The spike on the left has no detectable "foot" (recordings from [19]). The electrode must be placed in very close proximity to the cell inorder to measure the foot signal.

oxidized or reduced. Inorder for us to detect all the molecules that are rapidly released, the applied voltage must exceed the redox potential by at least 200 mV ("overpotential"). For catecholamines, a voltage of 700 mV in conjunction with a Ag/AgCl-electrode is sufficient. The experimental setup for amperometric recordings is shown in Fig. 2.7(a)-(b) and different transients recorded from chromaffin cells are shown in Fig. 2.7 (c). These recordings show amperometric transients that have a rapid rise of current and some recordings show a *foot* signal [19], which indicates the formation of the fusion pore [18]. A foot signal is characterized by small currents with a low rise time preceding the spike shaped transient current.

2.5.3 Total Internal Reflection Fluorescence (TIRF)-Microscopy

The capacitance and amperometric methods allow measurements of single-vesicle fusion with millisecond time resolution; however the spatial resolution of these methods is low. The capacitance and amperomteric measurements also do not reveal the pre-fusion and post-fusion movement of vesicles. Evanescent-wave microscopy [25] makes monitoring of individual vesicles possible. Evanescent-wave excitation of fluorescence is based on the decaying field generated near a dielectric field due to the total internal reflection of incident light, as illustrated in Fig. 2.8.

According to Snell's law, light incident on a medium of higher refractive index (n_1) to a medium of lower refractive index (n_2) undergoes total internal reflection back to the incident medium when the angle of incidence is grater than the *critical angle*. An evanescent field is created in the n_2 (denser) medium whose intensity

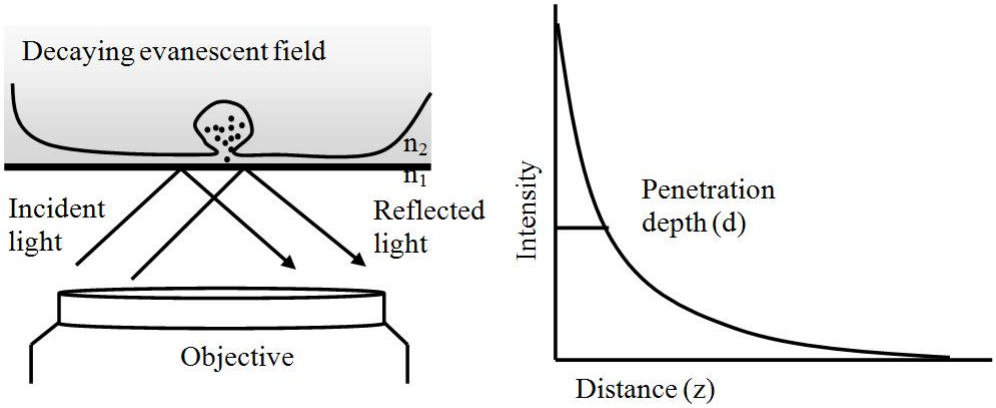

Figure 2.8: TIRF setup. Light incident on a medium of higher refractive index (n_1) to a medium of lower refractive index (n_2) is totally reflected back when the angle of incidence is grater than the critical angle. An evanescent field is created in the n_2 medium whose intensity decays exponentially. The highest intensity of evanascent light is very close to the dielectric interface making it ideal to observe absorption close to the surface. Cells with fluorescently labeled vesicles are placed atop a glass coverslip. The evanescent field excites the flurophores close to the surface and makes it possible to track the vesicles.

decays exponentially. The evanescent wave decays exponentially, according to

$$I(z) = I(0)e^{-z/d}$$

where I is the intensity , d is the penetration depth, and z is the distance. The penetration depth d is dependent on the incident angle, wavelength , polarization of light, and the refractive indices of the interacting media.

$$d = \frac{\lambda}{4\pi\sqrt{{n_1}^2 \sin\theta_1 - n_2^2}}.$$

The evanescent field typically penetrates to a depth of 100 nm providing a very low background.

Cells with fluorescently labeled vesicles are placed atop a glass coverslip. The evanescent field excites the flurophores close to the surface and makes it possible to

track the vesicles. When the cell is stimulated and exocytosis occurs, the vesicles release their contents and the flurophores disperse from their acidic compartments. Every event is recorded as a disappearing fluorescent spot in the recording or a fluorescence flash for dies that exhibit self quenching inside the vesicle, thus allowing the study of aspects of secretion including spatial relationships and dynamics of vesicles prior to and during exocytosis, and re-supply of vesicles. TIRF microscopy is much better than other fluorescence imaging methods because it reduces cellular photo damage and photo bleaching. TIRF imaging allows for longer observation times and spatial resolution.

2.6 The Need for Biosensors

The widespread interest in understanding quantal release is motivated by the importance of exocytosis in human health and disease. For example, changes in the release of the neurotransmitter *dopamine* underlie Parkinson's disease. The drug L-DOPA, a precursor of dopamine, provides symptomatic relief by increasing the amount of dopamine packaged into individual vesicles increasing vesicle size [26]. In contrast, drugs of abuse, such as amphetamines and cocaine block the uptake of transmitter into vesicles and thus decrease vesicle content (reviewed in [27]). Type D2-like dopamine auto receptors play important roles in the action of antipsychotic, psychostimulant drugs and in sexual behavior. Botulinum toxins exert their effects by inhibiting exocytosis through selective proteolysis of SNARE (an acronym for "soluble N-ethylmaleimide-sensitive factor attachment receptor") proteins that are known to be essential for exocytosis [28]. The inhibition of exocytosis and resulting paralysis of skeletal muscle by Botulinum toxin type A ("BoTox") has been used therapeutically to treat dystonias [28]. Complex psychological dis-

orders such as schizophrenia likely result from defects in multiple genes, including those involved in the regulation of exocytosis of neurotransmitter dopamine [29]. Changes in quantal size were observed in response to treatments that activate protein kinase C [30], protein kinase A [31], interference with dynamin [32], following overexpression of the R39C mutant of munc18 [33] or the protein complexion [34]. The current methods of detection of exocytosis suffer from significant drawbacks for use in pharmacological studies and for developing insights into the molecular machinery of exocytosis:

- In the electrochemical methods of measuring single-vesicle fusion, spatial resolution is low.
- Electrochemical techniques do not provide information on the events prior to vesicle fusion, on the events after vesicle fusion or on cell-cell interactions.
- Imaging techniques including TIRF provide spatial resolution, and shed light on events prior to fusion and the kinetics of fusion. However, the technique does not provide reliable information on the quantal size and does not facilitate studies involving the effects of various drugs on the fusion process.
- A major limitation in studying regulation of quantal size is the amount of data required to obtain statistically significant measurements. Quantal size can only be determined by measuring release from single cells. Therefore, a large number of single-cell experiments under tightly controlled experimental conditions are required to establish statistical significance and eliminate errors due to external factors.

One or more of the techniques mentioned earlier have been used in tandem to provide more insight into the molecular machinery and kinetics of exocytosis. Patch

amperometry allows the simultaneous measurements of increases in membrane capacitance along with detection of released molecules [35]. Electrochemical detector arrays combine TIRF imaging and amperomtry to study the kinetics of release [36]. Measurements of quantal release with conventional carbon-fiber microelectrodes from single cells under the microscope are slow and require skilled researchers, similar to most of the other techniques discussed here. It is thus vital to develop high-throughput techniques that allow measurements of many quantal events from a large number of cells under different experimental conditions.

The objective of this thesis is:

- to use technology derived from the semiconductor industry to develop micro devices for high-throughput electrochemical measurement of quantal exocytosis that will facilitate research and drug testing.
- to develop microfabricated arrays that will provide spatial resolution and improved time resolution.
- to design flexible electronic arrays that extend the capabilities of experimental methods including carbon fiber amperomtery, TIRF microscopy and planar electrode arrays on glass substrates, which are well equipped to study the molecular machinery of exocytosis.

The main conceptual difference when moving from a few electrodes to many is that it becomes increasingly difficult to connect individual electrodes in parallel to individual amplifiers and analog-to-digital converters (ADCs). This problem has been previously encountered in optical imaging devices, such as CCD cameras and CMOS imaging devices. In these devices, the individual pixels generate a current depending on incoming light intensity. The resulting charge is stored within

each individual pixel and subsequently transferred using matrix addressing to the readout, where it is sampled by a fast ADC. Optical CMOS imaging technology is well developed, relatively inexpensive, and flexible. The objective of this project is to develop and fabricate an electrochemical *potentiostat* array, where the charge injected from the oxidation current will be stored and transferred in an analogous way.

This research is about a device that will detect charges from simple metal electrodes and an electrochemical charge transfer of electrons that occurs during oxidation of biomolecules. Optical imaging devices with more than 1,000,000 pixels are now routinely made and it is thus conceivable that this electrochemical array may potentially allow parallel measurements of thousands of substances at the same time with a single chip. The impact on throughput in diagnostics and analysis would be revolutionary. In the following chapters, the design of such an electrochemical array will be discussed.

REFERENCES

[1] Katz, B., "The release of neural transmitter substances," *Sherrington lectures,* Springfield, Illinois: Thomas. ix, 1969.

[2] Alberts, B., *Molecular biology of the cell,* New York: Garland Science (4th ed.), 2002.

[3] Li, L. and L. S. Chin, "The molecular machinery of synaptic vesicle exocytosis," *Cell Mol Life Sci,* vol. 60, no. 5, pp. 942-960, 2003.

[4] Hille, B., *Ionic channels of excitable membranes,* Sunderland, MA: Sinauer Associates. xiii (2nd ed.), 1992.

[5] Shigeo Takamori, Matthew Holt, Katinka Stenius, Edward A. Lemke, Mads Grønborg, Dietmar Riedel, Henning Urlaub, Stephan Schenck, Britta Brügger,Philippe Ringler, Shirley A. Müller, Burkhard Rammner, Frauke Gräter, Jochen S. Hub, Bert L. De Groot, Gottfried Mieskes, Yoshinori Moriyama, Jürgen Klingauf, Helmut Grubmüller, John Heuser, Felix Wieland, and Reinhard Jahn "Molecular Anatomy of a Trafficking Organelle," *Cell,* vol. 127, no. 4, pp. 831-846, 2006

[6] Hodgkin, A. L., B. Katz, "The effect of sodium ions on the electrical activity of the giant axon of the squid," *J Physiol,* vol. 108, no. 1, pp. 37-77, 1949

[7] Goldman, D. E., "Potential, impedance, and rectification in membranes," *Journal of General Physiology,* vol. 27, no. 1, 0p. 37-60, 1944.

[8] Hodgkin, A. L., B. Katz, "The effect of sodium ions on the electrical activity of giant axon of the squid," *J Physiol,* vol. 108, no. 1, pp. 37-77, 1949.

[9] Hodgkin, A. L., A. F. Huxley, "A quantitative description of membrane current and its application to conduction and excitation in nerve," *J Physiol,* vol. 117, no. 4, pp. 500-44, 1952.

[10] Hodgkin, A. L., A. F. Huxley, and B. Katz, "Measurement of current-voltage relations in the membrane of the giant axon of Loligo," *J Physiol,* vol. 116, no. 4, pp. 424-48, 1952.

[11] Katz, B., "Quantal mechanism of neural transmitter release," *Science,* vol. 173, no. 992, pp. 123-6, 1971.

[12] Fatt, P. and B. Katz, "Spontaneous subthreshold activity at motor nerve endings," *J Physiol,* vol. 115, pp. 109-128, 1952.

[13] P. Fatt, B. Katz "Some Observations on Biological Noise," *Nature*, vol. 166, pp. 597-598, 1950.

[14] Gage, P. W., Armstrong, C. M. "Miniature end-plate currents in voltage clamped muscle fibres," *Nature,* vol. 218, pp. 363-365, 1968.

[15] Neher, E. and A. Marty, "Discrete changes of cell membrane capacitance observed under conditions of enhanced secretion in bovine adrenal chromaffin cells," *Proc Natl Acad Sci U S A,* vol. 79, no. 21, pp. 6712-6, 1982.

[16] Fernandez, J.M., E. Neher, and B.D. Gomperts, "Capacitance measurements reveal stepwise fusion events in degranulating mast cells," *Nature,* vol. 312, no. 5993, pp. 453-5, 1984.

[17] Lindau, M., "Time-resolved capacitance measurements: monitoring exocytosis in single cells," *Q Rev Biophys,*, vol. 24, no. 1, pp. 75-101, 1991.

[18] Wightman, R. M., Jankowski, J. A., Kennedy, R. T., Kawagoe, D. T., Schroeder,T. J., Leszczyszyn,D. J., Near,J. A., Diliberto jr.,E. J., Viveros,O. H., "Temporally resolved catecholamine spikes correspond to single vesicle release from individual chromaffin cells," *Proc Natl Acad Sci U S A,* vol. 88, no. 23, pp. 10754-8, 1991.

[19] Chow, R.H., L. von Ruden, and E. Neher, "Delay in vesicle fusion revealed by electrochemical monitoring of single secretory events in adrenal chromaffin cells," *Nature,* vol. 356, no. 6364, pp. 60-3, 1992.

[20] Oheim, M., Loerke, D., Chow, R. H., Stuhmer, W. "Evanescent-wave microscopy: a new tool to gain insight into the control of transmitter release," *Philos Trans R Soc Lond B Biol Sci,* vol. 354, no. 1381, pp. 307-18, 1999.

[21] Gillis, K. D., "Admittance-based measurement of membrane capacitance using the EPC-9 patch-clamp amplifier," *Pflugers Arch,* vol. 439, no. 5, pp. 655-64, 2000.

[22] Chow, R. H., Klingauf, J., Heinemann, C, Zucker, R. S., Neher,E., "Mechanisms determining the time course of secretion in neuroendocrine cells," *Neuron,* vol. 16, no. 2, pp. 369-76, 1996.

[23] Debus, K. and M. Lindau, "Resolution of patch capacitance recordings and of fusion pore conductances in small vesicles," *Biophys J,* vol. 78, no. 6, pp. 2983-97, 2000.

[24] Lollike, K., N. Borregaard, and M. Lindau, "The exocytotic fusion pore of small granules has a conductance similar to an ion channel," *J Cell Biol,* vol. 129, no. 1, pp. 99-104, 1995.

[25] Axelrod, D., "Cell-substrate contacts illuminated by total internal reflection fluorescence," *J Cell Biol,* vol. 89, no. 1, pp. 141-5, 1981.

[26] Gong, L. W., G. Alvarez De Toledo, and M. Lindau, "Secretory vesicles membrane area is regulated in tandem with quantal size in chromaffin cells," *Journal of Neuroscience,* vol. 23, no. 21, pp. 7917-7921, 2003.

[27] Sulzer, D. and E.N. Pothos, "Regulation of quantal size by presynaptic mechanisms," *Rev Neurosci,* vol. 11, no. 2-3, pp. 159-212, 2000.

[28] Pellizzari, R., Rossetto, O., Schiavo, G., Montecucco, C., "Tetanus and botulinum neurotoxins: mechanism of action and therapeutic uses," *Lond B Biol Sci,* vol. 354, no. 1381, pp. 259-68, 1999.

[29] Frankle, W. G., J. Lerma, and M. Laruelle, "The synaptic hypothesis of schizophrenia," *Neuron,* vol. 39, no. 2, pp. 205-16, 2003.

[30] Burgoyne, R.D., R.J. Fisher, and M.E. Graham, "Regulation of kiss-and-run exocytosis," *Trends Cell Biol,* vol. 11, no. 10, pp. 404-5, 2001.

[31] Pothos, E. N., "Regulation of dopamine quantal size in midbrain and hippocampal neurons," *Behav Brain Res,* vol. 130, no. 1-2, pp. 203-7, 2002.

[32] Graham, M. E., et al., "Dynamin-dependent and dynamin-independent processes contribute to the regulation of single vesicle release kinetics and quantal size," *Proc Natl Acad Sci U S A,* vol. 99, no. 10, pp. 7124-9, 2002.

[33] Fisher, R. J., J. Pevsner, and R. D. Burgoyne, "Control of fusion pore dynamics during exocytosis by Munc18.," *Science,*vol. 291, no. 5505, pp. 875-8, 2001.

[34] Archer, D. A., M. E. Graham, and R. D. Burgoyne, "Complexin Regulates the Closure of the Fusion Pore during Regulated Vesicle Exocytosis," *J Biol Chem,* vol. 277, no. 21, pp. 18249-52, 2002.

[35] Albillos, A., Dernick, G., Horstmann, H., Almers, W., Alvarez de Toledo, G., Lindau, M., "The exocytotic event in chromaffin cells revealed by patch amperometry," *Nature,* vol. 389, pp. 509-512, 1997.

[36] Hafez, I., Kisler, K., Berberian, K., Dernick, G., Valero, V., Yong, M. G., Craighead, and H. G. Craighead, Lindau, M. "Electrochemical imaging of fusion pore openings by electrochemical detector arrays," *Proc Natl Acad Sci U S A,* vol. 102, no. 39, pp. 13879-84, 2005.

CHAPTER 3

FUNDAMENTALS OF CIRCUIT DESIGN

Chip design is a complicated process that requires analysis and thinking at various levels of abstraction in the following hierarchy: device level, circuit level, architecture level and system level. Several textbooks focus on rigor at the device level, or circuit level small-signal analysis, neither of which help the student retain an intuitive instinct for circuit design. While experience, failure analysis, troubleshooting and breadboard testing are all important elements in the making of a good circuit designer, several non-textbook style books [1–5] aid the student in the right direction. In this chapter, I summarize the principles upon which I relied on to gain a circuit designer's point-of-view of a MOS transistor, which will introduce several concepts and parameters used throughout this thesis. I will also list some practical guidelines for successful chip design.

3.1 MOSFET Model

The MOSFET is a four-terminal device. It is the basic building block of CMOS devices. Fig. 3.1(a) is a schematic representation of the *p*MOS and the *n*MOS device, with their labeled terminals. A cross-sectional view of the MOS devices is illustrated in Fig. 3.1(b). A thin oxide layer separates the polycrystalline gate and the substrate, forming a capacitance $C_{\rm ox}$. When a positive voltage is applied to the gate of an *n*MOS transistor, a depletion region is formed from the lightly-doped p-type substrate to balance the positive charge on the gate. When the gate voltage is increased beyond the flatband voltage of silicon, $V_{\rm fb}$, the difference between the applied gate voltage and $V_{\rm fb}$, is partially dropped across the gate oxide

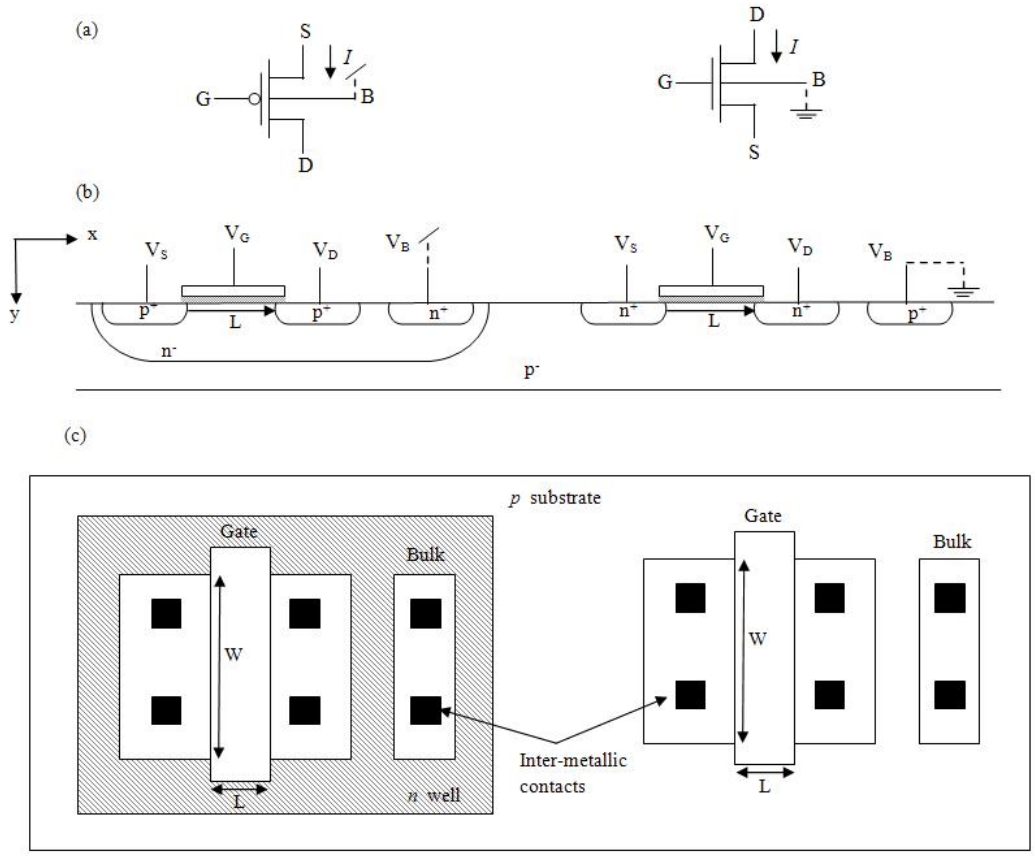

Figure 3.1: (a) Schematic representation of MOS transistors. The four terminals are the gate(G), source(S), drain(D) and bulk(B). The voltages applied to the gate(V_G), drain(V_D), source(V_S) in reference to the bulk voltage (V_B), controls the flow of channel current I. (b) The CMOS process technology used throughout the thesis is a n-well technology. In the n-well technology the substrate is a lightly doped p-type silicon wafer. The pMOS devices sit in a lightly-doped n well. The n well is connected to the highest possible voltage, usually the power supply to reverse bias the p-n junction diodes and to ensure no flow of current in the y direction. The p-type substrate is connected to the lowest power rail, usually the ground. (c) The top view of the physical layout of the device is source/drain-symmetric. The voltage at the terminals distinguishes source from drain. L indicates the gate length and W indicates the gate width.

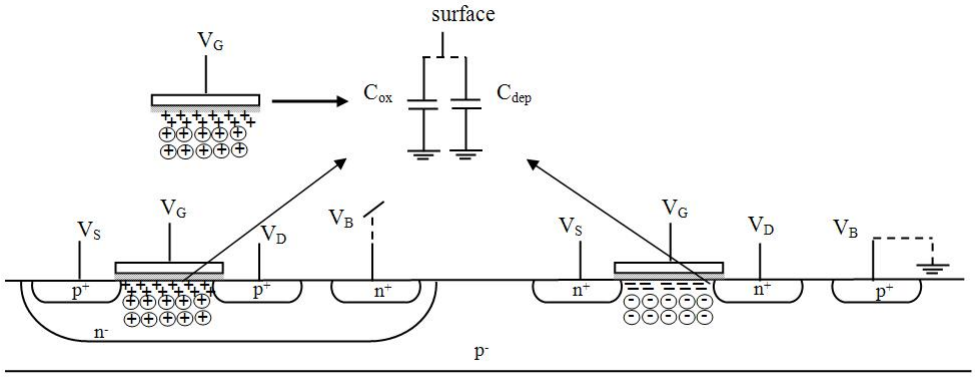

Figure 3.2: Schematic representation of the depletion layer formed from deep within the silicon, and the inversion layer. The total capacitance a combination of capacitance formed due to $Q_{\rm dep}$, charge per unit area in the depletion layer beneath the gate oxide, and $Q_{\rm m}$, the mobile charge per unit area in the channel.

and the depletion region. When the gate voltage is further increased, an inversion layer of mobile charges ($Q_{\rm m}$) is formed close to the surface of silicon, as shown in Fig. 3.2. This inversion layer acts as a bottom plate of a capacitor. The effective incremental capacitance per unit area of the channel (i.e., the silicon surface just beneath the oxide), comprises two capacitances in parallel, that of the gate and that of the depletion region. The capacitance per unit area between the gate and the substrate would be C, defined as $C \equiv C_{\rm ox} + C_{\rm dep}$, where $C_{\rm dep}$ is the capacitance due to the depletion layer. The expression for the spatial derivative of the mobile charge per unit area in the channel along the length of the channel

$$\frac{\partial Q_{\rm m}}{\partial x} = \left(C_{\rm dep} + C_{\rm ox}\right) \frac{\partial \psi_{\rm s}}{\partial x} = C \frac{\partial \psi_{\rm s}}{\partial x}, \tag{3.1}$$

where $\psi_{\rm s}$ is the potential drop across the depletion region beneath the gate. The channel current I flows due to a combination of drift and diffusion of carriers in the channel. In some operating regimes, drift current ($I_{\rm drift}$) dominates, in other regimes diffusion current ($I_{\rm diff}$) dominates. In many cases, the current is a

combination of both components. The channel current can be expressed as

$$I(x) = I_{\text{drift}}(x) + I_{\text{diff}}(x). \tag{3.2}$$

The drift component of the channel current is given by

$$I_{\text{drift}}(x) = (WQ_{\text{m}})\,\mu\xi_x = -W\mu Q_{\text{m}}\frac{\partial\psi_s}{\partial x}. \tag{3.3}$$

where μ is the effective low-field mobility of electrons in the channel, and ξ_x is the component of the electric field parallel to the channel, and W is the width of the channel. The diffusion component of the channel current is given by

$$I_{\text{diff}}(x) = D\frac{\partial\,(Q_{\text{m}})}{\partial x} = W\mu U_T\frac{\partial\,(Q_{\text{m}})}{\partial x} \tag{3.4}$$

where U_T is the thermal voltage $\frac{kT}{e_0}$. The expression for channel current that is independent of the position along the channel is obtained by integrating the channel current along the length of the channel

$$\begin{aligned}\int_0^L I(x)dx &= W\mu\int_0^L \left(I_{\text{drift}}(x) + I_{\text{diff}}(x)\right)dx \\ &= W\mu\int_0^L \left(-Q_{\text{m}}\frac{\partial\psi_s}{\partial x} + U_T\frac{\partial\,(Q_{\text{m}})}{\partial x}\right)dx\end{aligned} \tag{3.5}$$

Expressing Eq. 3.5 in terms of charge using Eq. 3.1,

$$I = \frac{W}{L}\mu\int_{Q_{\text{S}}}^0 \left(-\frac{Q_{\text{m}}}{C} + U_T\right)\partial Q_{\text{m}} - \frac{W}{L}\mu\int_{Q_{\text{D}}}^0 \left(-\frac{Q_{\text{m}}}{C} + U_T\right)\partial Q_{\text{m}}, \tag{3.6}$$

where Q_{S} is the mobile charge per unit area at the source end of the channel and Q_{D} is the mobile charge per unit area at the drain end of the channel.

To evaluate the integrals in closed form, the channel capacitance per unit area, C, is approximated to be a constant along x [7]. With this approximation, the channel current can be expressed as

$$I = \frac{S\mu}{2C}\left(Q_{\text{S}}^2 - 2CU_{\text{T}}Q_{\text{S}}\right) - \frac{S\mu}{2C}\left(Q_{\text{D}}^2 - 2CU_{\text{T}}Q_{\text{D}}\right) \tag{3.7}$$

where $S = W/L$ is the *strength ratio* of the device. The quadratic term in this equation originates from the drift component of channel charge and the linear term originates from the diffusion component of the channel charge.

3.1.1 MOS Transistor Characteristics

A complete set of MOS transistor characteristics can be derived from Eq. 3.7, by expressing the charge at the source and drain in terms of known voltages V_{G}, V_{D}, V_{S}, as defined in Fig. 3.1. For rigorous mathematical treatment, see [8–10]. In this section, an overview of the MOS transistor characteristics is presented.

3.1.2 Weak-Inversion Operation

In the weak-inversion mode of operation, the channel charge is primarily contributed by the depletion layer. In this regime, the electrostatics are determined only by the potential of the gate and the substrate. The surface potential being constant implies that the spatial derivative of the surface potential along the channel is zero, which means that there is no electric field along the length of the channel. Thus, the current cannot flow by drift and must flow by diffusion. The channel current is dominated by diffusion of carriers, therefore, the quadratic term in Eq. 3.7 can be ignored. In weak inversion, the carriers that have the sufficient energy to cross the source/drain-channel barrier follow the Boltzmann distribution. Thus, the mobile charge at the source and the drain end of the channel is,

$$Q_{\mathrm{S}} \propto e^{(\psi_{\mathrm{s}}-V_{\mathrm{S}})/U_{\mathrm{T}}} \quad \text{and} \quad Q_{\mathrm{D}} \propto e^{(\psi_{\mathrm{s}}-V_{\mathrm{D}})/U_{\mathrm{T}}}.$$

For small changes around some operating point, ψ_s is expanded to a Taylor series and truncated after the linear term. We choose to expand the surface potential ψ_s, at a gate voltage V_{T0}, referred to as the *zero-bias threshold* voltage, when both the source and the drain are grounded. At this gate voltage, the mobile charge densities at the source end and the drain end of the channel are equal to $-2CU_T$, i.e., $Q_S = Q_D = -2CU_T$. Thus, the mobile charge densities at the source and the drain end of the channel are approximated by

$$Q_S \approx -2CU_T e^{(\kappa(V_G - V_{T0}) - V_S)/U_T} \quad \text{and} \quad Q_D \approx -2CU_T e^{(\kappa(V_G - V_{T0}) - V_D)/U_T},$$

where $\kappa \equiv C_{ox}/(C_{ox} + C_{dep})$, is a capacitive divider ratio. Substituting the mobile charge per unit area in Eq. 3.7, and neglecting the quadratic terms, the complete weak inversion characteristic can be expressed as

$$I = I_s e^{(\kappa(V_G - V_{T0}) - V_S)/U_T} \left(1 - e^{-V_{DS}/U_T}\right) \tag{3.8}$$

where $I_s \equiv 2S\mu C_{ox} {U_T}^2/\kappa$. Eq. 3.8 represents a complete model for the nMOS transistor operation in ohmic and saturation regions, as shown in Fig. 3.3. The term, $I_s e^{(\kappa(V_G - V_{T0}) - V_S)/U_T}$, is the asymptotic saturation current I_{sat} for high V_{DS}. The current in the ohmic region can thus be expressed as

$$I = I_{sat}\left(1 - e^{-V_{DS}/U_T}\right) \qquad \text{ohmic region}$$

For $V_{DS} > 4U_T$ to $5U_T$, the channel current approaches I_{sat}

$$I \approx I_{sat} \qquad \text{saturation region}$$

3.1.3 Strong-Inversion Operation

In the strong inversion region, the mobile charge density in the channel exceeds the charge density in the depletion layer. The channel current in this case is

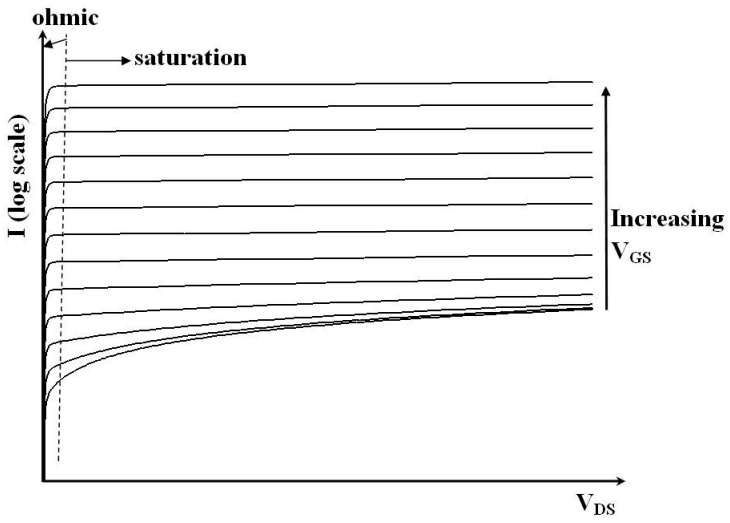

Figure 3.3: The channel current in weak inversion as V_{DS} is swept. The channel current is shown in logarithmic scale as the . The onset of saturation is at a constant voltage of 4-5U_T

predominately due to drift. In this regime, only the quadratic terms of Eq. 3.7 are considered. In this regime, the source/drain-channel energy barrier is reduced such that additional charges on the gate are balanced by additional mobile charges in the channel. Thus the inversion layer operates as a bottom plate of a capacitor, supplying all additional charges placed on the gate. The capacitance per unit area of the channel is C_{ox}. The mobile charge densities are

$$Q_S = -C_{ox}\left(V_G - V_T(V_S)\right) \quad \text{and} \quad Q_D = -C_{ox}\left(V_G - V_T(V_D)\right).$$

Substituting the charge densities in the quadratic terms of Eq. 3.7, the strong inversion characteristic, illustrated in Fig. 3.4, is given by

$$I = I_{sat}\left(1 - \left(1 - \frac{V_{DS}}{V_{DSsat}}\right)^2\right), \tag{3.9}$$

where

$$V_{DSsat} \equiv \kappa\left(V_G - V_{T0}\right) - V_S$$

and

$$I_{sat} \equiv \frac{S\mu C_{ox}}{2\kappa} V_{DSsat}^2.$$

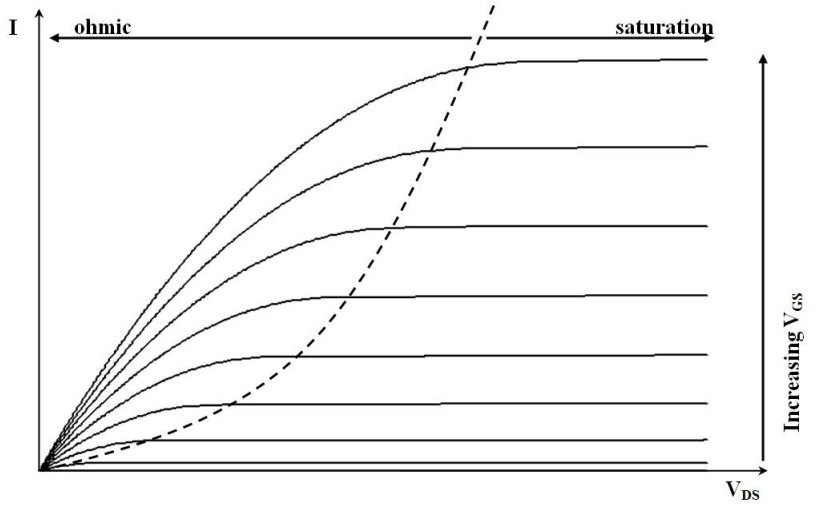

Figure 3.4: The channel current in strong inversion as V_{DS} is swept from rail-rail voltage. The saturation voltage in strong inversion region varies with the gate voltage.

The *p*MOS transistor channel current can be obtained by replacing the V_G with $(V_{DD} - V_G)$, V_D with $(V_{DD} - V_D)$ and V_S with $(V_{DD} - V_S)$ in Eq. 3.9 and Eq. 3.8, as the substrate is connected to the power supply voltage, V_{DD}.

3.1.4 Incremental MOS Transistor Characteristics

In order to design circuits, it is important to understand the incremental behavior of a circuit about a DC operating point, i.e., how the circuit responds if a *small* signal is applied to the input of the circuits, such that the circuit acts as a linear system. In this section, we shall examine several important *small-signal parameters* that factor into gain, bandwidth, noise performance, input and output impedances. Most MOS transistors are biased in the saturation region in a majority of analog circuits. Therefore, small signal parameters are derived for transistors operating

in saturation region. All the parameters are derived from the channel current expression.

The *transconductance gain* of a MOS transistor is a measure of how the channel current changes in response to changes in the gate voltage. Therefore,

$$\begin{aligned} g_{\mathrm{m}} &= \frac{\partial I_{\mathrm{sat}}}{\partial V_{\mathrm{G}}} \\ &\approx \frac{\kappa}{U_{\mathrm{T}}} I_{\mathrm{sat}} \qquad \text{weak inversion} \\ &\approx \frac{\kappa}{U_{\mathrm{T}}} \sqrt{I_{\mathrm{s}} I_{\mathrm{sat}}} \quad \text{strong inversion} \end{aligned}$$

The *source transconductance gain* of a MOS transistor is a measure of how the channel current changes in response to changes in the source voltage. The saturation current flows out of the source terminal, so a negative current $-I_{\mathrm{sat}}$ is used.

$$\begin{aligned} g_{\mathrm{s}} &= -\frac{\partial I_{\mathrm{sat}}}{\partial V_{\mathrm{S}}} \\ &\approx \frac{I_{\mathrm{sat}}}{U_{\mathrm{T}}} \qquad \text{weak inversion} \\ &\approx \frac{1}{U_{\mathrm{T}}} \sqrt{I_{\mathrm{s}} I_{\mathrm{sat}}} \quad \text{strong inversion} \end{aligned}$$

The *bulk transconductance gain* of a MOS transistor is a measure of how the channel current changes in response to changes in the bulk voltage.

$$\begin{aligned} g_{\mathrm{mb}} &= \frac{\partial I_{\mathrm{sat}}}{\partial V_{\mathrm{B}}} \\ &\approx \frac{1-\kappa}{U_{\mathrm{T}}} I_{\mathrm{sat}} \qquad \text{weak inversion} \\ &\approx \frac{1-\kappa}{U_{\mathrm{T}}} \sqrt{I_{\mathrm{s}} I_{\mathrm{sat}}} \quad \text{strong inversion} \end{aligned}$$

3.1.5 The Early Effect/Channel length Modulation

Drain characteristics of real MOS transistors in the saturation exhibit a finite slope instead of the ideal flat characteristic shown in the Fig. 3.4. This effect results from an increase in the width of the depletion region under increasing drain voltage, thus reducing the effective length of the channel, as depicted in Fig. 3.5 and is referred to as the *Early effect* (modeled by Jim Early) or *channel-length modulation*. This effect is represented as a resistance (Early-effect resistor across the source and drain), as illustrated in Fig. 3.6(a), and is expressed as

$$r_{\mathrm{o}} = \frac{V_{\mathrm{A}}}{I_{\mathrm{sat}}}, \tag{3.10}$$

where V_{A} is known as the *Early voltage*, derived by extrapolating the channel current, as shown in Fig. 3.6(b). The channel current expression in saturation is expressed as

$$I = I_{\mathrm{sat}} + \frac{V_{\mathrm{DS}}}{r_{\mathrm{o}}} = I_{\mathrm{sat}} \left(1 + \frac{V_{\mathrm{DS}}}{V_{\mathrm{A}}} \right). \tag{3.11}$$

The Early voltage is proportional to the channel length ($V_{\mathrm{A}} \propto L$), consequently, making the effect negligible in long-channel transistors, and predominant in short-channel devices.

The small signal parameters $g_{\mathrm{m}}, g_{\mathrm{s}}, g_{\mathrm{mb}}$ factor directly to gain, bandwidth, noise performance. These parameters are all set by the quiescent channel current. The charge-based MOS model described in this chapter is a more intuitive one for a circuit designer than other models, routinely described in textbooks. For example, from a circuit designer's perspective, if a high-gain amplifier is desirable, it is immediately evident that in weak inversion, the channel current increases exponentially with the gate voltage, and hence the transconductance gain is very high. Additionally, it is also evident that the channel current in weak inversion regime is

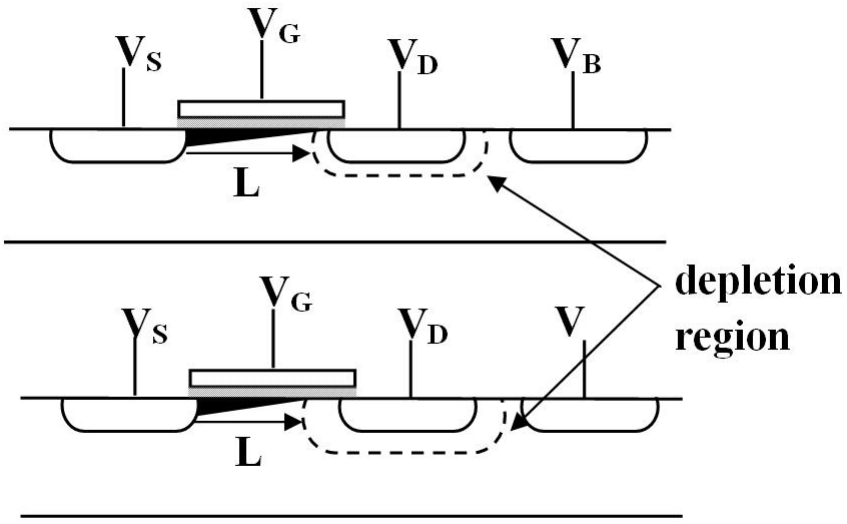

Figure 3.5: Early effect is defined as the reduction of channel length as the drain voltage is increased from the top trace to the bottom trace.

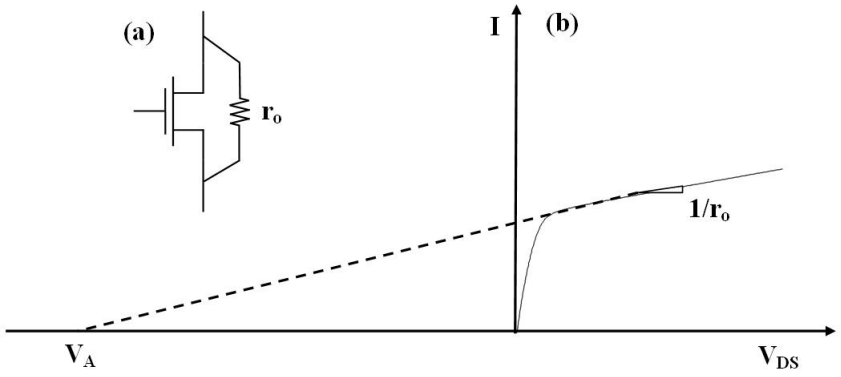

Figure 3.6: (a) Schematic of a transistor with the Early effect resistor across the source and drain terminals. (b) Early voltage is the V-axis intercept of the extrapolated linear fit. The Early voltage is proportional to gate length.

driven by diffusion, and hence the device will operate relatively slowly. This kind of design perspective is lost in other MOS device models.

3.2 Practical Guidelines

A handle on device-level, circuit-level and system-level abstraction is not sufficient to design, fabricate and test successful chips. Many first-time designs are doomed to fail or malfunction, for a wide variety of reasons. In this section, I enlist some practical guidelines to avoid common mistakes, and practices that make "fixing" easier.

- While the trend of the day is smaller, faster and cheaper, at the beginning of a new project, it is a wise idea to start with intermediate device sizes to avoid failure due to second-order effects in short-length and/or narrow-width devices. If layout area is an important design criteria, it is important to recognize that the main limitation to the layout area reduction is interconnect width and not the actual size of the transistor.
- Most MOSFET model parameters supplied by foundries are suitable for simulation of digital circuits and are not accurate models for analog and mixed-mode circuit simulation. In order to accurately simulate the design, an appropriate device model and device parameters are necessary. The Enz-Krummenacher-Vittoz (EKV) model [12] of the MOS transistor provides a simple approximate closed-form expression for channel currents that are valid in all regions of MOS transistor operation, transitioning smoothly from weak inversion to strong inversion. The EKV model also has the advantage of a relatively small number of parameters to accurately model the channel cur-

rent. All foundries include *process monitors* or transistor arrays to extract models for transistors. EKV model parameters can be extracted with relative ease from the such transistor arrays [13, 14]. In this work, process monitors (AMIS CF5 0.5 μm CMOS process) were requested from MOSIS and EKV model parameters were extracted for circuit simulation using Tanner Tools (Appendix A).

- For accurate simulations, it is important to understand the simulation tool and the circuit solving algorithms in some detail. DC operating point failures can be avoided by setting proper tolerance options for the circuit solver [11].
- While a layout that passes the layout vs. schematic test generally does not fail to operate, poor layout design can affect the matching of similar circuits in large-scale arrays. Good layout designs and floor plans [15] also reduce the effects of power line noise and other sources of noise coupling onto sensitive signal lines.
- The output measurement system and its *loading* effect on the device under test must be taken into consideration when designing the circuits.
- Finally, important nodes should be brought out to bonding pads to probe them in case of failure. Low-impedance nodes can be brought to the pads directly, while high impedance nodes must be buffered.

REFERENCES

[1] Jim Williams (edited by) *The Art and Science of Analog Circuit Design, EDN Series for Design Engineers,* Butterworth-Heinemann Publications: MA, 1998.

[2] Jim Williams (edited by) *Analog Circuit Design, Art, Acience and Personalities, EDN Series for Design Engineers,* Butterworth-Heinemann Publications: MA, 1991.

[3] C. Toumazou, F. J. Lidgey and D. G. Haigh, *Analogue IC Design: The Current-Mode Approach,* Peter Peregrinus Ltd.(IEE): London, 1990.

[4] B. Razavi, *Design of Analog CMOS Integrated Circuits,* McGraw-Hill Higher Education, 2000.

[5] B. A. Minch, "ECE 453: Intoduction to Microelectronics," Cornell University, Lecture Notes, 2002.

[6] Zeng, F.-G., Rebscher, S., Harrison, W., Sun, X., Feng, H., "Cochlear Implants: System Design, Integration, and Evaluation," *IEEE Reviews in Biomedical Engineering,* vol.1, pp.115-142, 2008.

[7] M. A. Maher and C. A. Mead, *A Physically Charge-Controlled Model fror MOS Transistors, ARVLSI: Proceedings of the Stanford Conference,* P. Losleben, Ed., MIT Press, Cambridge, MA, pp. 211-229, 1987.

[8] C. A. Mead, *Analog VLSI and Neural Systems,* Addison-Wesley, Reading, MA, 1989.

[9] E. A. Vittoz, "Micropower Techniques," *Design of Analog-Digital Circuits for Telecommunications and Signal Processing,* J. E. Franca and Y. Tsividis, Eds., pp. 53-96. Prentice-Hall, Englewood Cliffs, NJ, 1994.

[10] K. Bult, "Basic CMOS Circuit Techniques," *Analog VLSI Signal and Information Processing,* M. Ismail and T. Feiz., pp. 12-56. McGraw-Hill, New York, 1994.

[11] Ron Kielkowski, *Inside SPICE,* NewYork : McGraw-Hill, 1998.

[12] Enz, C. C.; Krummenacher, F.; Vittoz, E.A., "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and

Low-Current Applications", *Analog Integrated Circuits and Signal Processing Journal on Low-Voltage and Low-Power Design* , vol. 8, pp. 83-114, July 1995.

[13] M. Bucher, C. Lallement, C. Enz, F. Thodoloz, F. Krummenacher, "The EPFL-EKV MOSFET Model Equations for Simulation, Model Version 2.6," *Technical Report, Electronics Laboratories, Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland,* June, 1997.

[14] M. Baucher, C. Lallement and C. Enz, "An efficient parameter extraction methodology for the EKV MOST Model," *Proc. IEEE Int. conf. on Microelectronic Test Structures (ICMTS), Trent, Italy,* March 25-28, 1996.

[15] A. Hastings, *The Art of Analog Layout,* Prentice Hall, 2001.

CHAPTER 4

DESIGN OF A CMOS POTENTIOSTAT CIRCUIT FOR ELECTROCHEMICAL DETECTOR ARRAYS

In Chapter 2, it has been described that amperometric techniques can detect quantal release of oxidizable transmitters, by using a carbon fiber or a platinum microelectrode that is positioned close to the cell surface and held at a constant potential that is sufficiently high to oxidize the released molecules.

In this chapter, I will describe the design of a novel *potentiostat* circuit that measures astrometric currents, while maintaing the electrode at a constant potential. I will also describe a CMOS electrochemical detector array for high-throughput characterization of quantal events. The detector array comprises a two-dimensional array of electrodes, each of which is connected to a novel regulated-cascode amplifier (RCA). To achieve cellular dimensions, each detector unit should be on the order of 10-20 μm on a side, which constrains the number of transistors per detector. The electrode potential must be stable, because an unstable electrode voltage leads to charging and discharging of the liquid junction capacitance creating excessive baseline fluctuations in current measurements. The half-width of the release events is typically a few milliseconds, which implies that the readout rate should be at least in the kHz range. The amperometric spikes are often preceded by a small foot signal of a few picoamperes in amplitude [1] that contains valuable information on the properties of the fusion pore [2]; this consideration implies that the input-referred noise current of a potentiostat detector should be less than 1 pA.

Some CMOS potentiostat designs have been proposed earlier [3, 4]. These designs employ current mirrors to amplify currents to the μA range, increasing

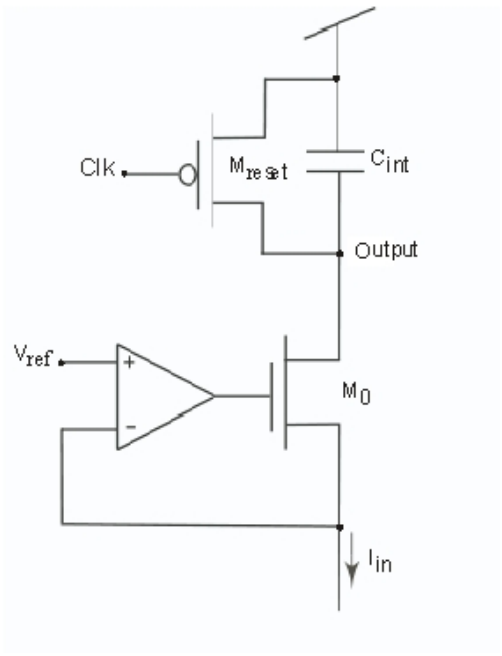

Figure 4.1: Schematic view of a potentiostat circuit comprising the integration capacitor C_{int}, the feedback amplifier and reset switch M_{reset}.

power consumption. The regulated-cascode amplifier (RCA) detector array is capable of measuring small currents without increasing the power consumption and layout area by eliminating amplifying circuitry. An approach discussed in [5] involves a *p*MOS, *n*MOS OTA and a dual-slope comparator. Recently, time-base VLSI potentiostats [6–8], were proposed. These designs employ a pF integration capacitor and an OTA that occupies a large area. With the shared amplifier stage, similar performance was achieved while maintaining a small area. Previously, some proposed multichannel potentiostat circuits [9]. In these designs a standard differential amplifier is used to keep the potential of the electrode constant, while the readout is done using a a current-mode sigma-delta ADC with a variable oversampling ratio. While these designs are suitable for a small array, the RCA design achieves better spatial resolution with the shared amplifier structure.

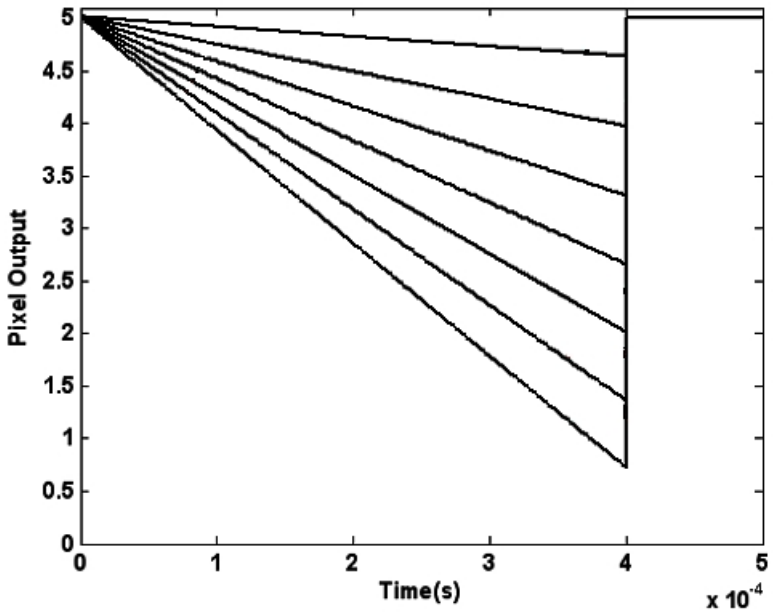

Figure 4.2: Simulation results of the RCA circuit. The output voltage varies linearly with various input current values.

In this chapter, I will describe the design and implementation of the RCA potentiostat and report experimental results from a small test array that was fabricated in a 0.5-μm, 5-V CMOS process through MOSIS. In Section 4.1, I will explain the circuit operation. In Section 4.2, I will derive the noise analysis and compare the performance of the amplifier with that of a folded-cascode amplifier. In Section 4.3, I will present the schematics and operation of the output stage. Finally, in Section 4.4, I will present the measurement results.

4.1 Circuit Operation

Fig. 4.1 shows a schematic of a single potentiostat detector circuit. The circuit comprises a cascode transistor and a feedback amplifier that maintains the electrode at a stable reference voltage, V_{ref}. The operation of the potentiostat is straightfor-

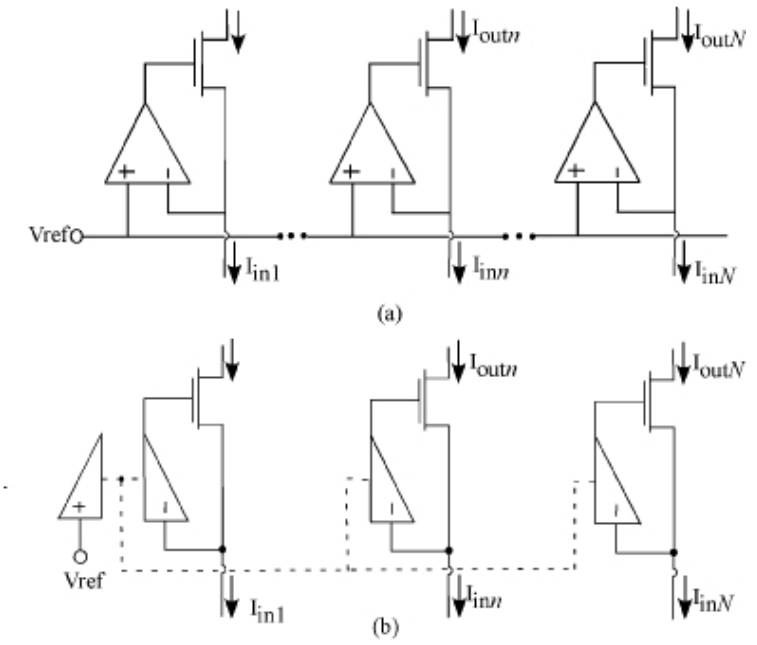

Figure 4.3: An array of regulated cascode circuits (a) with independent op-amp circuits and (b) with the proposed scheme in which all amplifiers share a common half circuit.

ward. The current I_{in}, produced as a result of oxidation events on the electrode surface, is buffered by the cascode transistor to the node labeled "Output" where it is integrated by a 50-fF integration capacitor, C_{int}, to produce an output voltage. Periodically, the output voltage is reset to the positive power supply rail, V_{dd}, through a reset transistor, M_{reset}. Fig. 4.2 shows simulation results of the potentiostat for an integration time of $400\,\mu s$. As the input current was varied from 50 pA to 650 pA in 100 pA increments, the output voltage varied linearly with the input current. The input impedance of the cascode, g_{s0}, is relatively low. When high-gain amplifier is used, as shown in Fig. 4.1, to produce a regulated cascode, the input impedance is further reduced by the gain of the amplifier. In this application, a low input impedance was required in order to maintain a high injection efficiency. Injection efficiency is defined as the fraction of the electrode current that is buffered by the cascode transistor to the output node. The low-frequency

input impedance of the potentiostat is given by,

$$R_{\text{in}} = \frac{1}{g_{\text{s0}}\,(1 + \kappa A_0)}, \tag{4.1}$$

where g_{s0} is the incremental source conductance of the cascode transistor M_0, κ is the reciprocal subthreshold slope factor, a constant with a typical value between 0.5-0.9, and A_0 is the low-frequency gain of the regulation amplifier. For a typical input current level of tens to hundreds of picoamperes, this input resistance can be as low as hundreds to tens of kiloohms, which is much less than the impedance of the effective shunt capacitance formed at the liquid-solid interface of the electrode over the frequency range of interest, resulting in a very high injection efficiency.

In order to keep each detector as small as possible, a shared amplifier structure was used in which all regulation amplifiers in a given row share a common half circuit. Fig. 4.3(a) shows a one-dimensional array of regulated cascode circuits, in which each regulated cascode circuit has its own amplifier. However, because the noninverting input of each op-amp in the array is connected to a common potential, V_{ref}, a common half circuit can be shared among all of the amplifiers in the array, as shown conceptually in Fig. 4.3(b). In this scheme, each amplifier requires only half the layout area and half the power consumption as would its counterpart in the array of Fig. 4.3(a) for a given unity-gain bandwidth and low-frequency gain. Such a scheme has been employed successfully in infrared imaging systems, in which context it is called *share-buffered direct injection* (SBDI) [10–12]. The shared half amplifier in the SBDI circuit, shown in Fig. 4.4(a), comprises transistors M_1, M_3, M_5. The independent half circuits comprise of transistors M_{2n}, M_{4n}, M_{5n}, where n ranges from 1 to N. The design of a new shared amplifier circuit, shown in Fig. 4.4(b), is based on the folded-cascode op-amp topology.

Fig. 4.4(b) shows a transistor-level schematic of the shared amplifier circuit.

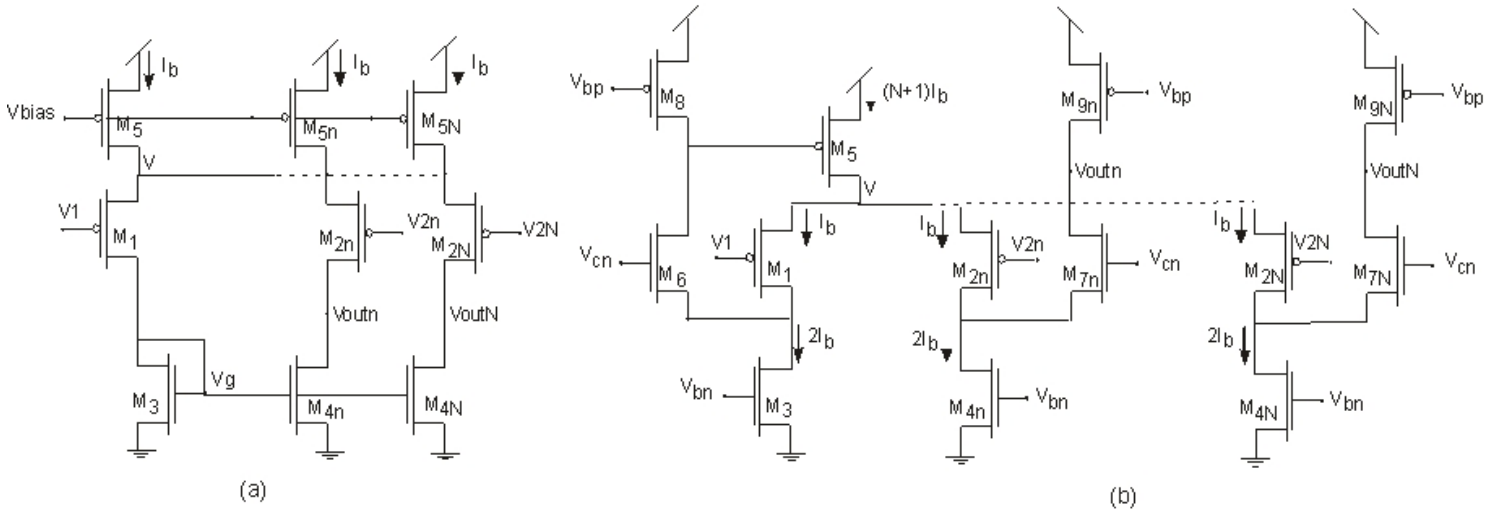

Figure 4.4: Transistor-level schematics of (a) SBDI circuit proposed by Wu and Hsieh [10–12] (b) the proposed scheme in which we share a common half circuit (i.e., stage 1), between all of the amplifiers (i.e., amplifiers n and N shown) in the array shown in Fig. 4.3(b).

The shared half circuit (i.e., stage 1, shown on the left in Fig. 4.4(b)) comprises M_1, M_3, M_5, M_6, and M_8. N independent half circuits are added to stage 1 at the node V. The n^{th} independent half circuit (i.e., stage n) comprises M_{2n}, M_{4n}, M_{7n}, and M_{9n}, where n ranges from 1 to N. To generate the bias voltages V_{bp}, V_{cn} and V_{bn}, a low-voltage cascode bias circuit described in [13], was used. The shared half circuit contains a negative feedback loop that maintains V just far enough above the common noninverting input voltage, V_1, so that transistor M_1 passes the bias current, I_{b}.

The operation of a single amplifier is described here by considering the shared half circuit, stage 1, and the independent half circuit, stage n. If the inverting input voltage to stage n, V_{2n}, is equal to V_1, then transistor M_{2n}, which is nominally identical to M_1, also passes I_{b}. Consequently, by Kirchhoff's current law (KCL), transistor M_{7n} will also pass I_{b}, which matches the saturation current of M_{9n}, so the amplifier will be in its high-gain region in which M_{7n} and M_{9n} are both saturated. If V_{2n} is slightly below V_1, then transistor M_{2n} will pass substantially more current than I_{b}, reducing the current flowing in M_{7n} causing $V_{\text{out}n}$ to rise until M_{9n} is in its ohmic region. On the other hand, if V_{2n} is slightly above V_1, then transistor M_{2n} will pass substantially less current than I_{b}, increasing the current flowing in M_{7n} causing $V_{\text{out}n}$ to fall until M_{7n} is in its ohmic region. In a small range of voltages around the point at which, $V_1 \approx V_{2n}$ it can be shown that the incremental output voltage of the shared amplifier is given by,

$$\delta V_{\text{out}} = A_0 \left(V_1 - V_{2n}\right) = g_{\text{m}2n} r_{\text{o}9n} \left(V_1 - V_{2n}\right), \tag{4.2}$$

where A_0 is the low-frequency gain of the amplifier, $g_{\text{m}2n}$ is the incremental transconductance gain of each input transistor M_{2n}, and $r_{\text{o}9n}$ is the incremental output resistance of the pMOS transistor M_{9n}.

Next, I will describe feedback regulation of node V by the common half circuit that is shared by the N amplifiers. If the inverting voltages V_{22}-$V_{2N} = V_1$, then the inverting input transistors M_{22}-M_{2N}, that are equivalent to M_1 also pass a current of I_b. According to KCL,

$$I_5 = I_1 + I_{22} + ...I_{2N} = (N+1)I_\mathrm{b}. \tag{4.3}$$

The feedback loop adjusts the gate voltage of M_5 to pass a current of $(N+1)\,I_\mathrm{b}$ and the common node V just enough to allow M_1 to pass I_b. The capacitance at node V is the sum of the N source capacitances contributed by N input stages. Thus the capacitive load on node V is proportional to N. However, from Eq. (4.3), the bias current of M_5 is also proportional to N.

The new shared amplifier represents an improvement over the SBDI circuit, in terms of low-frequency gain, the shared half circuit's ability to drive the capacitive load imposed by the common line V, that couples the amplifiers together and stability, isolation between neighboring amplifiers and each amplifier's output swing. I will discuss each of these improvements in turn in the following subsections.

4.1.1 Low-Frequency Gain

The low-frequency gain of our amplifier is given by $g_{\mathrm{m}2}r_{\mathrm{o}9}$. The output impedance and the transconductance gain are provided by different transistors M_9 and M_2 respectively. The gain of the RCA amplifier can be optimized by making the transistor M_9 longer. The gain of the RCA circuit is a 6 dB improvement over the gain of the SBDI amplifier [10–12], which is $g_{\mathrm{m}2}(r_{\mathrm{o}2} \parallel r_{\mathrm{o}4})$, provided the output impedance of the pMOS and nMOS transistors are comparable. In this circuit, the transconductance gain and the output impedance depend on the small-signal

parameters of the same transistor M_2; g_{m2} and r_{o2} trade off with each other making it difficult to optimize the gain.

4.1.2 Stability and Bandwidth

The negative feedback loop also greatly reduces the incremental resistance through which the half circuit drives node V. The incremental resistance seen looking back into the shared half circuit, stage 1, is given by,

$$R_V = \frac{1}{g_{s1}(1 + g_{m5}r_{o8})}. \tag{4.4}$$

Analysis of the frequency response of the RCA reveals that the nondominant pole of the amplifier is at node V. The nondominant pole is $[R_V C_V]^{-1}$, where C_V is the total capacitance at node V. Due to the reduced impedance given in Eq. 4.4, the nondominant pole is pushed farther away from the dominant pole, by the gain $(1 + g_{m5}r_{o8})$, providing wider bandwidth and stability.

4.1.3 Isolation Between Amplifiers

When there is an incremental change in the input voltage of stage n, δV_{2n}, and stage $(n+1)$, $\delta V_{2(n+1)}$, an incremental current $g_{m2n}\delta V_{2n}$, $g_{m2n}\delta V_{2(n+1)}$ flows through M_{7n} and $M_{7(n+1)}$ respectively, changing their output voltages. The incremental output voltages of stages n and $(n+1)$ are,

$$\delta V_{outn} = -g_{m2n}r_{o9n}\left(\delta V_{2n}\right), \tag{4.5}$$

$$\delta V_{out(n+1)} = -g_{m2(n+1)}r_{o9(n+1)}\left(\delta V_{2(n+1)}\right), \tag{4.6}$$

The outputs $\delta V_{\text{out}n}$ and $\delta V_{\text{out}(n+1)}$ are only dependent on their own input voltages. The node V remains unchanged so long as the noninverting input V_1 is held constant. The gain from node V to each output of the circuit of Fig. 4.4(a) is $g_{\text{s}2}(r_{\text{o}2} \parallel r_{\text{o}4})$ and to each output of the circuit of Fig. 4.4(b) is $g_{\text{s}2}r_{\text{o}9}$. Any movement of node V induced by the inverting input of one amplifier would couple into the other outputs. In the RCA circuit, the common source line, V, is better regulated by the negative feedback loop, which lowers the effective resistance through which V is driven by a factor of $g_{\text{m}5}r_{\text{o}8}$.

4.1.4 Output Swing

Many applications require varying the reference voltage to observe redox currents at the electrode surface. With the RCA shared amplifier scheme, potential of the electrode can be set anywhere in the range of 0 V to 3.2 V, which may be required in such applications. The output swing of the amplifier is an improvement over [10–12], extending from two saturation voltage drops above ground to one saturation voltage drop short of V_{dd}. In subthreshold, the saturation voltage drop is approximately 100-130 mV, which translates to an almost rail-to-rail output voltage swing. The SBDI circuit was used to regulate the source of a pMOS transistor. If this amplifier was used to regulate an nMOS transistor, as shown in Fig. 4.1, complementary version of the shared amplifier would be used. In that case for transistor $M_{2\text{n}}$ to remain in saturation, the output voltage has to be substantially higher than the inverting input voltage. This means that the regulated electrode node can have a limited range of voltages or that the power supply voltage has to be increased by 1.2-1.5 V. The RCA circuit can regulate both pMOS and nMOS transistors without loosing output swing.

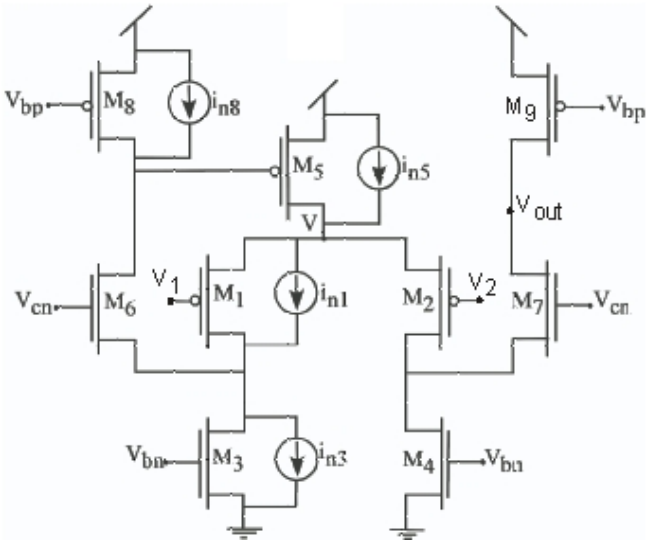

Figure 4.5: Schematic of the amplifier with equivalent thermal noise current sources $i_{\mathrm{n}1}, i_{n3}, i_{n5}, i_{n8}$ of the transistors M_1, M_3, M_5, M_8, that contribute to the output.

These improvements over the SBDI circuit come at the cost of power consumption. The power consumption of each RCA unit is $2I_{\mathrm{b}}V_{\mathrm{dd}}$ as compared to $I_{\mathrm{b}}V_{\mathrm{dd}}$ of the SBDI unit. This scheme allows the achievement of a performance similar to the folded-cascode amplifier at a cost of fewer than half the number of transistors in each potentiostat. The amplifier can have a low-frequency gain in the thousands and effectively maintain a stable reference voltage at each electrode.

4.2 Noise Analysis

The noise performance of the RCA amplifier is comparable to that of a folded-cascode amplifier, for a given bias level and set of transistor dimensions. The thermal noise sources corresponding to each transistor of our amplifier are shown in Fig. 4.5. The folded-cascode amplifier shown in Fig. 4.4(a) has similar noise sources associated with each corresponding transistor. These sources represent the thermal current noise per unit bandwidth of a subthreshold MOS transistor, the

variance of which is given by [16, 17]

$$\overline{i_{\mathrm{n}}^2} = \frac{2kT}{\kappa} g_{\mathrm{m}}, \tag{4.7}$$

where the transconductance $g_{\mathrm{m}} = \kappa I_{\mathrm{D}}/U_{\mathrm{T}}$ and κ is the reciprocal subthreshold slope factor. The right half of the regulated-cascode amplifier is similar to that of a regular folded-cascode amplifier, resulting in the same effect by each corresponding transistor on the output node. It can be shown that the corresponding transistors in the left half of the amplifiers have a similar effect on their output nodes. The noise current source i_{n5} of the folded-cascode amplifier in Fig. 4.4(a) flows symmetrically through the two paths and cancels at the output node. In the RCA amplifier, the source i_{n5} sees a current divider between the two paths. The output thermal noise contribution of transistor M_5 is i_{no5}, given by

$$i_{\mathrm{no5}} = \frac{i_{\mathrm{n5}}}{g_{\mathrm{m5}} r_{\mathrm{o8}} + 2}.$$

For typical bias currents, the loop gain $g_{\mathrm{m5}} r_{\mathrm{o8}} \gg 1$. Further, the amplifier is shared among N potentiostats in a row. Since g_{m5} is proportional to bias current, which is $(N+1)\, I_{\mathrm{b}}$, the loop gain $g_{\mathrm{m5}} r_{\mathrm{o8}}$ is increased N-fold. The increase in g_{m5} also leads to an N-fold increase in the noise current source i_{n5}. However, the resulting noise current is shared by N half-amplifiers contributing negligible noise currents to each amplifier's output. Thus, it can concluded that i_{no5} is negligible. The noise sources i_{n8} and i_{n3} in Fig. 4.4(a) are mirrored to the output node. In regulated-cascode amplifier, the effect of i_{n8} on the output is

$$i_{\mathrm{no8}} = i_{\mathrm{n8}} \frac{g_{\mathrm{m5}} r_{\mathrm{o8}}}{g_{\mathrm{m5}} r_{\mathrm{o8}} + 2} \approx i_{\mathrm{n8}}.$$

Similarly the effect of M_3 is,

$$i_{\mathrm{no3}} \approx i_{\mathrm{n3}}.$$

A complete noise analysis revealed that the total input referred voltage noise per unit bandwidth, $\overline{v_{\rm ni}^2}$ is,

$$\overline{v_{\rm ni}^2} = \frac{4kT}{\kappa}\left(\frac{1}{g_{\rm m1}} + \frac{g_{\rm m3}}{g_{\rm m1}^2} + \frac{g_{\rm m8}}{g_{\rm m1}^2}\right). \tag{4.8}$$

The input referred noise is approximately equal to that of a folded-cascode amplifier, although in the RCA scheme, the amplifier occupies half the layout area and consumes half the power per amplifier.

Flicker (or $1/f$) noise is an important consideration in low-frequency measurements. In most CMOS technologies, pMOS transistors have one or two orders of magnitude lower $1/f$ noise than do nMOS transistors [18]. In the regulated-cascode amplifier amplifier, by using pMOS input transistors, the $1/f$ noise is reduced. Flicker noise is inversely proportional to the gate area. Maximizing the area of the transistors, however, would increase the pixel area. Here, the choice of minimum-width transistors degraded the $1/f$ noise. Further reduction of the $1/f$ noise was achieved by using a correlated double sampling circuit [19, 20], which I will describe in the following section.

In addition to the noise contributed by the feedback amplifier, the reset transistor $M_{\rm reset}$ contributes noise due to clock feedthrough, charge injection, and thermal noise of the on-resistance of the reset switch. When the signal goes from on to off (i.e., from low to high), the clock signal feeds through the gate-drain capacitance $C_{\rm gd}$, and appears across the integration capacitance $C_{\rm int}$. The clock feedthrough is quantified as,

$$v_{\rm nclk} = \frac{C_{\rm gd}V_{\rm dd}}{C_{\rm gd} + C_{\rm int}}. \tag{4.9}$$

Another form of noise due to the reset transistor is charge injection. When the switch is turned off, the charge under the gate oxide is injected into the integration capacitor. However, these effects are offsets and can be corrected through calibra-

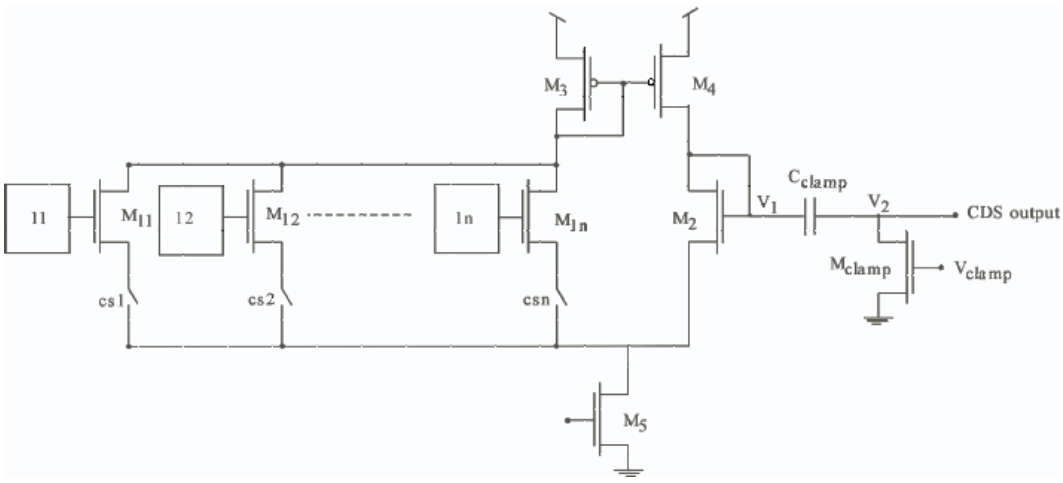

Figure 4.6: Schematic block diagram of the common output stage, where an output stage of row_1 is shared by n columns. Each column is sequentially switched through $c_{\text{s}1}, ...c_{sn}$ to the output buffer to sample the output at the end of the integration period.

tion and double sampling. The on-resistance of the switch introduces thermal noise on the output node and when the switch is turned off, this noise is sampled onto the integration capacitor. This noise scales as,

$$\overline{v_{\text{nth}}^2} = \frac{kT}{C_{\text{int}}}. \tag{4.10}$$

This noise can be reduced by increasing the integrating capacitor which would also increase the layout area and decrease the transimpedance gain for a given switching frequency. In order to optimize the size of the integration capacitor, the trade off between noise, layout area, frequency and gain must be considered.

4.3 Output Stage

The source follower, which is used to buffer the detector output to the readout circuitry in infrared imagers and active pixel sensors [12, 14, 15], suffers from many shortcomings. The source follower has limited output voltage swing. The gain

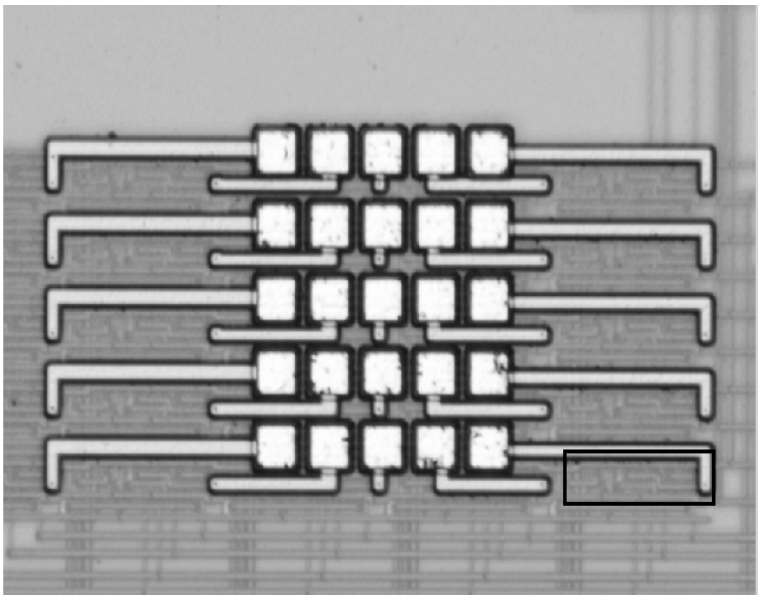

Figure 4.7: Micrograph of the die showing the 5×5 array of electrodes. The electrodes are $10\,\mu$m on each side.The area enclosed by the solid lines is a single potentiostat circuit.

of the source follower is κ, which has a dependence on its input voltage, so the source follower is nonlinear. The temperature dependance of κ affects the gain [21]. However, the source follower is widely used because of its simplicity and small layout area. In this scheme, an almost rail-to-rail differential amplifier was used, that has uniform gain of unity across the chip. The schematic of the first row of potentiostat detector circuits and the common output stage is shown in Fig. 4.6. The buffer is shared by all the detectors in a row. The detectors 11 through $1n$ are sequentially switched to complete the buffer by turning on the column switches cs_1 through cs_{n}. The noninverting input and the access switch are a part of the detector, while the remaining transistors are outside the detector. By using this architecture, better performance than the source follower was achieved without increasing the layout area of the potentiostat circuit. This kind of architecture is used in active pixel imagers for high-speed readout [22]. The buffered output is then fed to the correlated-double sampling (CDS) circuit shown in Fig. 4.6. At the

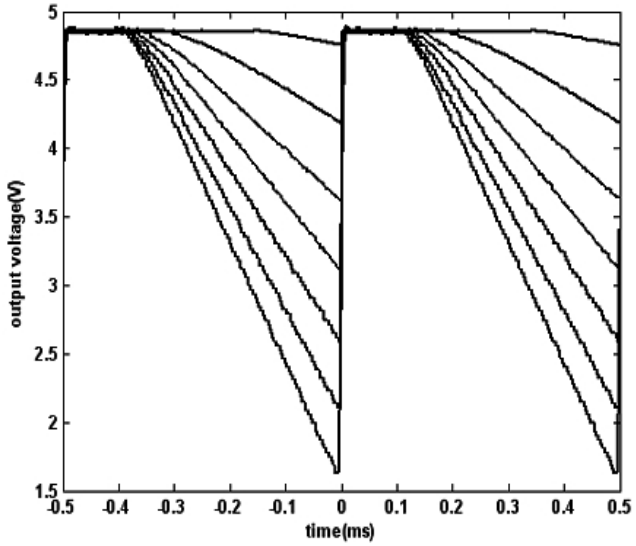

Figure 4.8: Measurement results showing the output voltage of the unit potentiostat for two clock periods.

end of the integration period, M_{clamp} and c_{s1} are closed, and the node V_1 is set to a voltage of $(V_{\text{dd}} - V_{\text{sig}} + V_{\text{n}})$, where V_{sig} the output voltage of potentiostat$_{11}$, and V_{n} is the $1/f$ noise. During this time, V_2 is held at ground by M_{clamp}. At reset, when the integrating capacitor C_{int} is reset to V_{dd}, the switch M_{clamp} is opened pulling V_1 to $(V_{\text{dd}} + V_{\text{n}})$. The voltage V_2 is the difference of the two samples, $(V_{\text{dd}} + V_{\text{n}}) - (V_{\text{dd}} - V_{\text{sig}} + V_{\text{n}})$=$V_{\text{sig}}$, which is buffered onto a multiplexed common bus. The CDS circuit thus reduces the $1/f$ noise.

4.4 Results

A test chip containing a 5×5 detector array was fabricated in a 0.5-μm, 5-V CMOS process through MOSIS in order to verify the basic operation of the detector and the shared amplifier circuit technique, shown in Fig. 4.7. The area of a single detector was 525 μm^2 and the pitch was 15 μm. Fig. 4.8 shows the test results from

a single detector. Each unit contained a 50-fF integration capacitor. The amplifier bias current was set to 100 nA for these measurements. The power consumption of each unit is 1 μW. For these tests, the input current was supplied through an nMOS current mirror. The input current was varied from 10 pA-600 pA and an integration time of 400 μs was used. Throughout, the reference voltage was held constant at 0.7 V, which is a typical electrode potential for amperometric experiments. It should be noted that the output voltage does not extend all the way to the positive supply rail, because it was buffered by an amplifier whose maximum output voltage was 4.85 V. Thus for the smallest input currents, the final output voltage is not discernable. A rail-to-rail buffer design would make measuring small currents possible. As the input current increases, the final output voltage increases linearly. With a 50-fF integration capacitor and a 400-μs integration time, the output voltage saturates at about 0.8 V for an input current of 500 pA. An improved buffer design will make it possible to record smaller currents down to the noise limit, such a design is required to record amperometric foot signals. Fig. 4.9 shows the current-voltage characteristic of a unit detector after the correlated double sampling circuit. The fit and the measured data are in good agreement verifying the linear behavior of the potentiostat. The transimpedance gain of the potentiostat detector is 9.3 mV/pA. The coefficient of determination of the current-voltage characteristic is 0.99 in the current range of 20 pA-400 pA.

The charge resolution is set by the noise. The noise at the output of the detector, for measurements at input current of 20 pA is shown in Fig. 4.10. The figure shows a thousand superimposed measurements of the output voltage. The rms noise of the measurements is $\approx$ 110 fA or 274 electrons. The maximum charge storage capacity is approximately 1.26×10^6 electrons. Current commercially available amplifiers used for amperometry include the VA10 (NPI Electronics), which

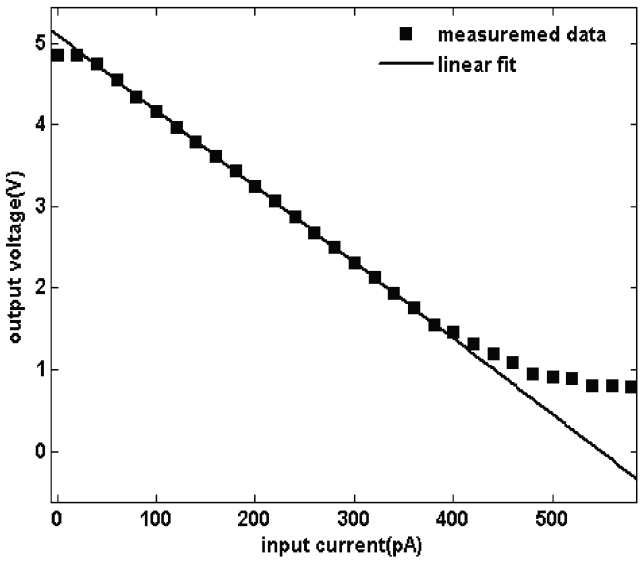

Figure 4.9: I-V characteristic of the potentiostat, showing a linear behavior. Here the input current is varied from 10 pA to 600 pA and an integration capacitance of 50 fF was used.

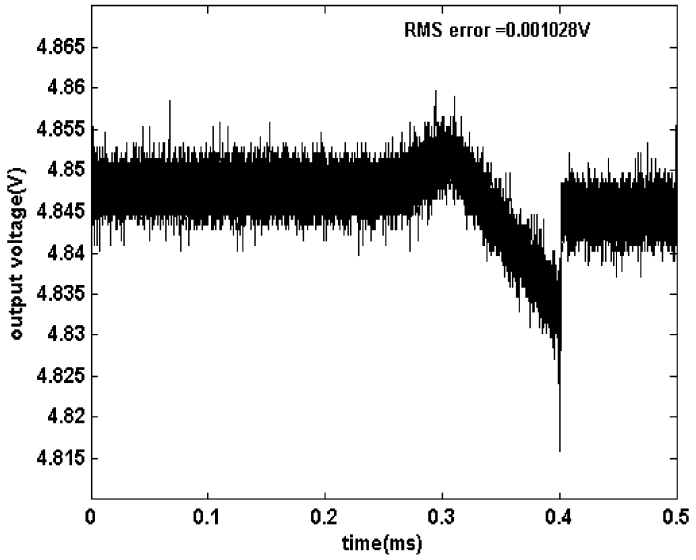

Figure 4.10: Measured data showing the output noise of the potentiostat circuit for an input current of 20 pA. The rms error is equivalent to 0.1095 pA or 274 electrons.

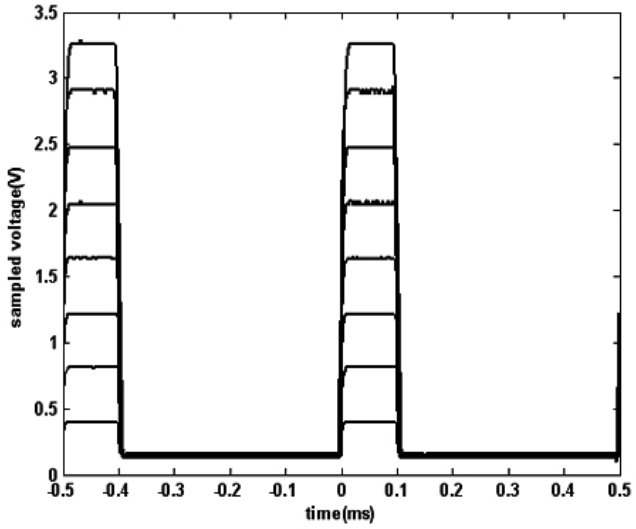

Figure 4.11: Measured data showing the output of the correlated double sampling circuit for an input current of 10 pA-400 pA.

specifies current noise less than 1 pA as well as the high-end low-noise patch clamp amplifiers EPC7/8 (HEKA Electronics) and Axopatch 200B (Molecular Devices). For the EPC7/8 noise less than 0.1 pA is specified at 3 kHz bandwidth, which is close to the 0.11 pA at 2 kHz bandwidth of the RCA circuit. The lowest noise is achieved by the Axopatch 200B (0.06 pA at 5 kHz). The RCA circuit uses very few components and incorporates a scalable array of amplifiers and compares favorably with current state-of-the-art instruments. The noise performance of the RCA circuit may be further optimized eventually approaching that of the Axopatch 200B amplifier.

Fig. 4.11 shows the output of the CDS circuit of a single detector in the prototype 5×5 array. Here again, the CDS output is seen to vary linearly with the input current. The transimpedance gain of the detector circuit after the CDS stage is 9 mV/pA. The I-V characteristic of the CDS output of several pixels in a row is shown in Fig. 4.12. Experimental data and linear fit are in good agreement verifying linear operation. The mismatch between potentiostats in a row varied

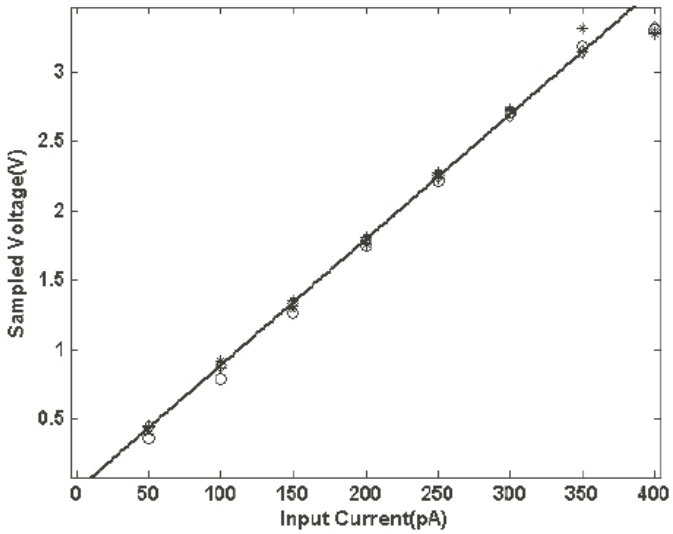

Figure 4.12: Measured data showing the I-V characteristic of several potentiostats after the correlated double sampling stage. The solid line indicates a linear fit of the data.

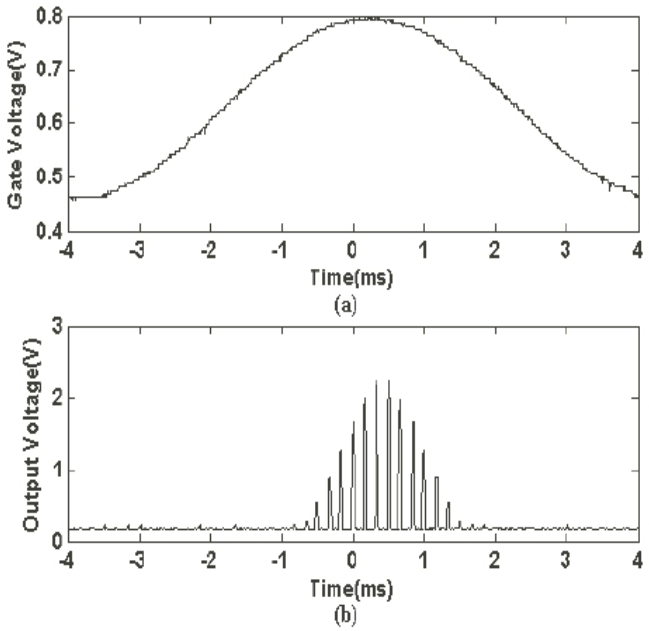

Figure 4.13: Measured data showing (a) The varying voltage applied to the gate of the current mirror. (b) The sampled output voltage.

from 6%-14%. However, after characterization, the mismatch can be digitally calibrated. It is important to note that one of the factors that contributes to the mismatch is the use of current mirrors of minimum dimensions to inject current. Current mirrors would not be necessary in the electrochemical setup, which would reduce the mismatch. Dynamic current measurements are shown in Fig. 4.13. A slow moving sine wave is applied to the gate of the current mirror. At sampling frequency of 6 kHz, the output follows the input voltage above the threshold voltage of the nMOS transistor.

REFERENCES

[1] R. H. Chow, L. V. Rüden, and E. Neher, "Delay in Vesicle Fusion Revealed by Electrochemical Monitoring of Single Secretory Events in Adrenal Chromaffin Cells," *Nature,* vol. 356, pp. 60-63, 1992.

[2] A. Albillos, G. Dernick, H. Horstmann, W. Almers, G. Alvarez de Toledo, and M. Lindau, "The Exocytotic Event in Chromaffin cells Revealed by Patch Amperometry," *Nature,* vol. 389, pp. 509-512, 1997.

[3] R. F. B. Turne, D. J. Harrison, and H. P. Baltes, "A CMOS Potentiostat for Amperometric Chemical Sensors," *IEEE Journal of Solid-State Circuits,* vol. SC-22, no. 3, pp. 473-478, 1987.

[4] A. Bandopadhyay, G. Mulliken, G. Cauwenberghs, and N. V. Thakor, "VLSIpotentiostat Array for Distributed Electrochemical Neural Recording," *Proceedings of IEEE International Symposium on Circuits and Systems*, pp. II-740-II-743, Phoenix,AZ, 2002.

[5] M. Breten, T. Lehmann, and E. Braun, "Integrating Data Converters for Picoampere Currents from Electrochemical Sensors," *Proceedings of the 2000 IEEE International Symposium on Circuits and Systems,* Geneva, Switzerland, vol. V, pp. 709-712, 2000.

[6] H. S. Narula and J. G. Harris, "VLSI Potentiostat for Amperometric Measurements for Electrolytic Reactions," *Proceedings of the 2004 IEEE International Symposium on Circuits and Systems,* vol. I, pp. 457-460, Vancouver, Canada, 2004.

[7] H. S. Narula and J. G. Harris, "A Time-Based VLSI Potentiostat for Ion Current Measurements," *IEEE Sensors Journal*, vol. 2, pp. 239247, April 2006.

[8] H. S. Narula, J. G.Harris, "Integrated VLSI Potentiostat for Cyclic Voltammetry in Electrolytic Reactions," *Proceedings of the IEEE Computer Society Annual Symposium on VLSI Emerging Trends in VLSI Systems Design (ISVLSI'04)*, pp. 268-270, 2004.

[9] K. Murari, M. Stanacevic, N. V. Thakor, and G. Cauwenberghs, "Wide-range,Picoampere-Sensitivity Multichannel VLSI Potentiostat for Neurotransmitter Sensing," *Proceeding of the 26th Annual International Conference of the IEEE EMBS,* pp. 4063-4066, San Francisco, CA, 2004.

[10] C. C. Hsieh, C. Y. Wu, F. W. Jih, and T. P. Sun, "Focal-Plane-Arrays and CMOS Readout Techniques of Infrared Imaging Systems," *IEEE Transactions on Circuits and Systems for Video Technology,* vol. 7, pp. 594-605, 1997.

[11] C. Y. Wu and C. C. Hsieh, "New Design Techniques for a Complementary Metal-Oxide Semiconductor Current Readout Integrated Circuit for Infrared Detector Arrays," *Optical Engineering,* vol. 34, pp. 160-168, 1995.

[12] C. Y. Wu, C. C. Hsieh, F. W. Jih, T. P. Sun, and S. J. Yang, "A New Share-Buffered Direct-Injection readout Structure for Infrared Detector Arrays," *SPIE*, vol. 2020, pp. 57-64, 1993.

[13] B. A. Minch, "A Low-Voltage MOS Cascode Bias Circuit for All Current Levels," *IEEE International Symposium on Circuits and Systems*, vol. 3, pp. 619-622, 2002.

[14] H. Kulah and T. Akin, "A Current Mirroring Integration Based Readout Circuit for High Performance Infrared FPA Applications," *IEEE Transactions on Circuits and Systems-II : Analog and Digital Signal Processing*, vol. 50, no. 4, pp. 181-186, 2003.

[15] C. C. Hsieh, C. Y. Wu and, T. P. Sun, "A New Cryogenic CMOS Readout Structure for Infrared Focal Plane Array," *IEEE Journal of Solid-State Circuits,* vol. 32, no. 8, pp. 1192-1199, 1997.

[16] R. Sarpeshkar, T. Delbrück, and C. A. Mead, "White Noise in MOS Transistors and Resistors," *IEEE Circuits and Devices,* vol. 9, no. 6, pp. 23-29, 1993.

[17] S. -C. Liu, J. Kramer, G. Indiveri, T. Delbrück, and R. Douglas, *Analog VLSI Circuits and Principles,* Cambridge, MA : MIT Press, pp. 313-340, 2002.

[18] C. Jakobson, I. Bloom, and Y. Nemirovsky, "1/f Noise in CMOS Transistors for Analog Applications from Subthreshold to Saturation," *Solid-State Electronics,* vol. 42, no. 10, pp. 1807-1817, 1998.

[19] R. J. Kansy, "A Response of a Correlated Double Sampling Circuit to 1/f Noise," *IEEE Journal of Solid-State Circuits,* vol. SC-15, pp. 373-375, 1980.

[20] H. M. Wey and W. Guggenbühl, "An improved Correlated Double Sampling Circuit for Low Noise Charge-Couple Devices," *IEEE Journal of Solid-State Circuits,* vol. 37, pp. 1559-1565, 1990.

[21] H. C. Card and R. W. Ulmer, "On the Temperature Dependence of Subthreshold Currents in MOS Electron Inversion Layers," *Solid State Electronics,* vol. 22, pp. 463-465, 1979.

[22] C. Boemler and J. Zarnowski, "Image Sensor ADC and CDS per Column," US6965407 B2, 2005.

CHAPTER 5

ON-CHIP AMPEROMETRIC RECORDINGS OF TRANSMITTER RELEASE USING A CMOS POTENTIOSTAT CIRCUIT

In recent years, several CMOS devices have been developed for applications to such diverse fields of study as drug design, neurobiology, DNA sequence analysis, and cellular metabolism [1–4]. CMOS potentiostats for the electrochemical detection of biomolecules, for measuring ion-channel current, and for cyclic voltammetry using off-chip transducers have been developed [5–10]. In Chapter 4, a CMOS potentiostat design that was described here is scalable to an array that allows simultaneous on-chip measurement of exocytosis from a large number of cells [11].

In this chapter, I will describe the post-CMOS deposition of polarizable electrode material on the on-chip aluminum electrodes and the packaging of the chip to enable on-chip experiments. Using a single potentiostat circuit, the ability of the potentiostat circuit to measure electrochemical reactions and cellular exocytotic events with high sensitivity will be demonstrated. In Section 5.1, the experimental setup, materials, and methods used to conduct on-chip electrochemical measurements will be described. In Section 5.2, the post-CMOS fabrication techniques employed to incorporate the transducer onto the potentiostat circuit will be described. In Section 5.3, experimental results will be presented.

5.1 Materials and Methods

A schematic of the experimental setup is shown in Fig. 5.1. This schematic represents a single element of the proposed sensor array. In contrast to a conventional

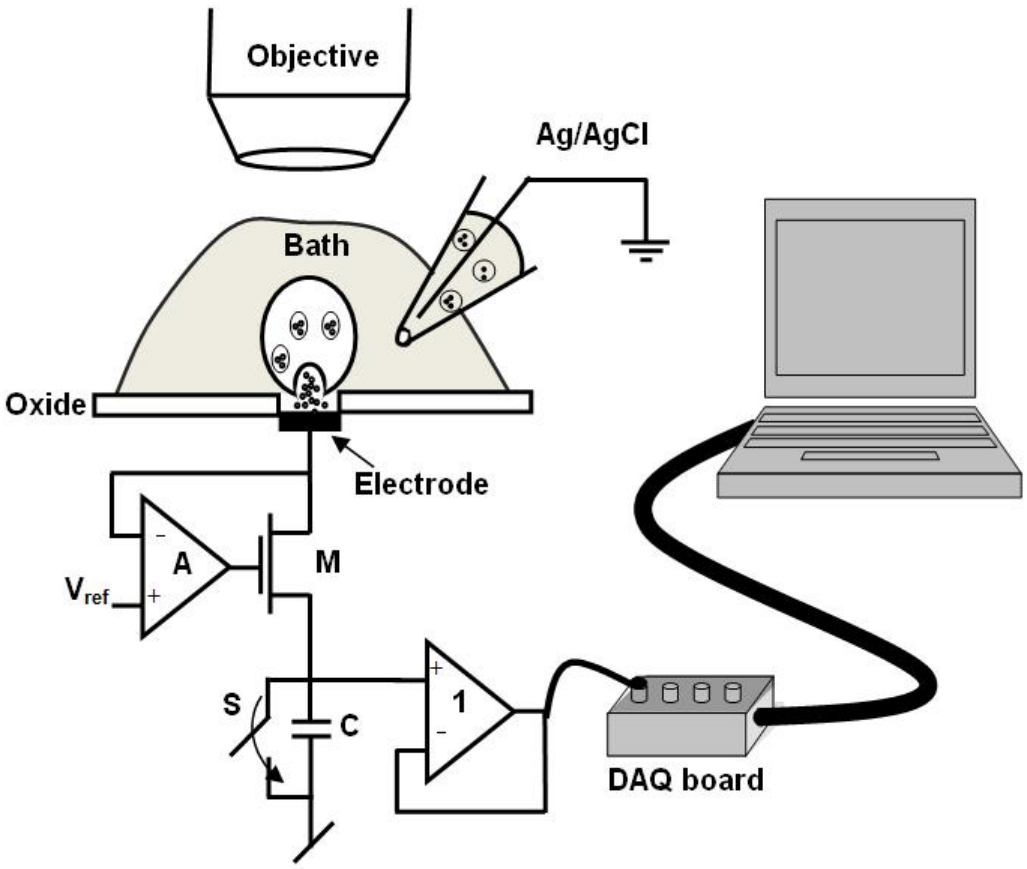

Figure 5.1: Schematic of the experimental setup: The printed circuit board is mounted on an adjustable microscope stage. A pipette holder is placed on another adjustable microscope stage to position the pipette near the electrode. The microscope along with the adjustable holders is housed in a properly grounded faraday cage to eliminate power line noise. The output is connected to a 16-bit A/D converter, clocked externally to sample data at the end of the integration period. The A/D converter is connected to a computer where the data is acquired and analyzed.

carbon-fiber apparatus, this device includes sensor circuits at the site of detection for improved sensitivity. A high-gain amplifier A holds the electrode at the oxidation potential of the target molecule and the transistor M conveys the electrons to the capacitor C, which is periodically reset by switch S. At the end of the integration period, the voltage on the capacitor is buffered to the data acquisition board (National Instruments PCI-6251). The printed circuit board, along with the

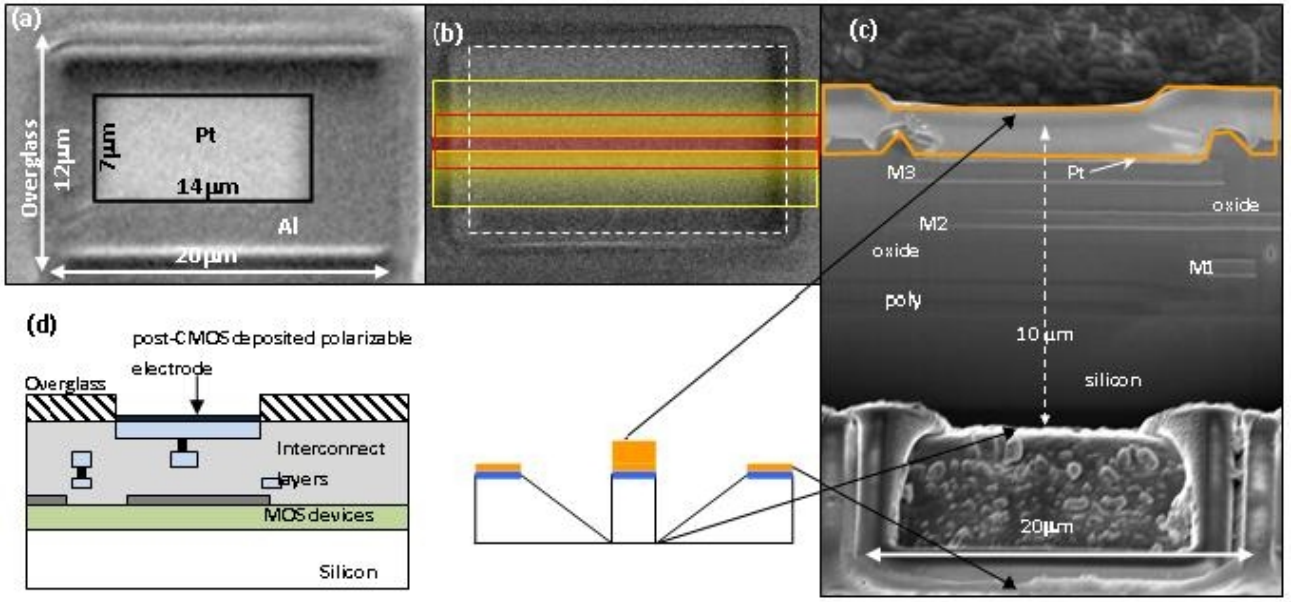

Figure 5.2: (a) Platinum deposition using the focused electron beam. Post-CMOS processing includes removal of the native oxide layer and deposition of Pt. Only a portion of the Al electrode is covered with platinum to illustrate the contours and resolution of the deposited layer. (b) Aluminum electrode completely covered with 200-nm Pt. Fully covered electrodes are used for on-chip electrochemical detection. The dashed-line box indicates area covered with Pt. The two solid line boxes indicate the area removed to expose a cross-sectional face. (c) A FIB image of a cross-sectional face of the CMOS die, depicting the platinum layer, interconnect layers (M1-M3), poly and the substrate. The crosshashed layer indicates extra layer of platinum that was deposited to protect the sample from ion damage during the imaging processes. (d) A schematic of the CMOS die prior to post-CMOS fabrication. Openings in the overglass layer are made at the CMOS foundry.

CMOS chip is mounted on an adjustable microscope (Ziess Axioskop 2) stage. The whole setup is housed in a properly grounded Faraday cage placed on a vibration table.

5.1.1 Cell and Bath Solution Preparation

Bovine adrenal glands obtained from a local slaughterhouse were prepared according to established protocols [12]. The resulting chromaffin cells were suspended in the tissue culture medium and stored in a T-25 flask in a 10% CO_2 incubator at 37 °C. Cells were used on days 1-3 in culture. On the day of the experiment, cells in the medium were transferred to a 15-mL tube and pelleted in a centrifuge at 5000 rpm for 10 minutes, and resuspended in 1-2 mL of bath solution. The bath solution contains 150-mM NaCl, 5-mM $CaCl_2$, 5-mM KCl, 2-mM $MgCl_2$, 10-mM HEPES buffer and 20-mM glucose. The osmolarity of the solution was measured to be 300-310 mOsm and the pH was 7.25.

5.1.2 Experimental Setup

A wide-mouthed pipette was filled with cell solution. During experimentation, light pressure was applied to the pipette and cells were ejected onto the detection electrode filled with the bath solution. A grounded Ag/AgCl electrode was placed in the pipette, as shown in Fig. 5.1. For electrochemical measurements of dopamine, the wide-mouthed pipette was replaced with a 5-μm-tip-diameter pipette. Pulses of pressure were applied to the pipette using a picospritzer (Picospritzer III, Parker Hannifin Corp., Fairfield, NJ), to eject picoliters of dopamine onto the electrode.

5.2 Post-CMOS Fabrication

Several biomolecules and neurotransmitters are oxidizable, and therefore can be measured as an amperometric current trace. In order to oxidize these molecules, an appropriate transducer electrode is required. Typical transducer electrode materials include carbon, platinum and gold. The CMOS chip was fabricated using AMIS C5F 0.5-μm technology. The interconnect material used in this technology is Al, and thus the on-chip electrodes are Al electrodes. Aluminum is not a suitable material for electrochemistry. A transducer electrode that facilitates electrochemical reactions is called a polarizable electrode [13]. When a polarizable electrode is immersed in salt solution, no current flows through the electrode-liquid interface. When a voltage is applied to the polarizable electrode, excess charge accumulates on the electrode surface, and is counter balanced by the ionic charge in the solution at a finite distance called the Debye length [14]. Current does not flow through the interface at equilibrium. However, when oxidizable molecules diffuse to the surface of the electrode, electrons are transferred. Therefore, the surface of the Al electrode must be covered with a polarizable electrode material. Here, we describe polarizable material deposition using two methods: focused-electron-beam deposition of platinum and physical vapor deposition of gold/platinum using photolithography.

5.2.1 Focused-Electron-Beam Deposition

During the development phase of new CMOS circuit techniques, small-geometry dies are preferred because they are economical. However, post-CMOS fabrication of small-geometry dies present several challenges including handling the chips. On

small geometry CMOS dies, platinum can be deposited with relative ease using the focused-ion-beam (FIB) or focused-electron-beam techniques. The FIB system is generally used by circuit designers to make device/circuit edits on prototype integrated circuits, in order to correct/troubleshoot and subsequently test design of CMOS circuits. This system facilitates making metal connections, disconnections and probe pads. The metal that can be deposited using the FEI strata 400 Dual Beam FIB system at the Cornell Center for Materials Research (CCMR) is platinum. Using a low-current (<100 pA) focused ion beam, the native oxide layer on aluminum is milled away. Precursor gases flowing over the chip interact with the electron column. The electron-beam-induced chemical reaction results in the deposition of Pt with sub-micron-scale resolution on the electrode surface, as shown in Fig. 5.2(a). For electrochemical on-chip recordings, the electrode was fully covered with Pt (Fig. 5.2(b)). The composition of the deposited amorphous layer was platinum : carbon : gallium : oxide in proportions of 45 : 24 : 28 : 3, with a resistivity in the range of 70-700 $\mu\Omega$cm [15]. Penetration of impurities in the focused-electron-beam deposited film depends on the interaction between the electron beam and the sample, the beam current, and grounding of the sample. The challenge in using the electron beam is locating the region of interest. The CMOS die is covered with a thick overglass layer, and this insulating layer gets charged under electron bombardment, which makes identification of regions of interest difficult. In order to alleviate these problems, the layout design must include alignment marks on top metal layer, metal3 with openings in the overglass layer. In this case, the exposed aluminum pads could be located with a low-current electron beam without excessive charging, by properly grounding the chip. When a 5.0-kV, 25-pA electron beam was used to deposit the platinum layer, no evidence of damage was observed and the functionality of the CMOS chip was not affected. A schematic

of the various layers of the circuit pre-FIB fabrication is shown in Fig. 5.2(d), and a cross-sectional FIB image of the CMOS potentiostat circuit post fabrication is shown in Fig. 5.2(c).

5.2.2 Photolithography

Focused-electron-beam deposition has the advantage of high resolution and ease of handling, but for larger areas and arrays with many electrodes, this method is too slow and involves chip exposure to the ion beam for extended periods to locate the electrodes, and may eventually alter the functioning of the circuit. As an alternative procedure, the use of physical vapor deposition of Ti/Au could be utilized for post-CMOS fabrication of the chip was investigated. A process flow diagram of the post-CMOS fabrication is shown in Fig. 5.3(a). To allow proper handling, the small 2.5-mm × 2.5-mm CMOS die was attached to a 4" photoresist-coated wafer and baked. Subsequently, a 1.3-μm thick photoresist (Shipley 1813) layer was spun on the chip surface. The photoresist was patterned using a tone-reversed photomask, exposing all areas except the aluminum electrodes. The chip was then developed (MF 321 for 60 sec) following image reversal. Photoresist spins off of the edges of the small CMOS die due to its rectangular shape, thus, the edges of the chip were initially not covered with photoresist. In some cases, the photoresist on the edges was stripped during the photomask contact. This was corrected by manual application of additional photoresist to the edges of the CMOS die (Fig. 5.3, step 4) before it was baked. The chip was then descummed (stripped of organic materials and residual photoresist) using GLEN 1000p plasma cleaning system in the electron-free mode. Electron-free mode prevents electrostatic damage. In the electron-free mode, the samples to be cleaned are placed on a floating shelf be-

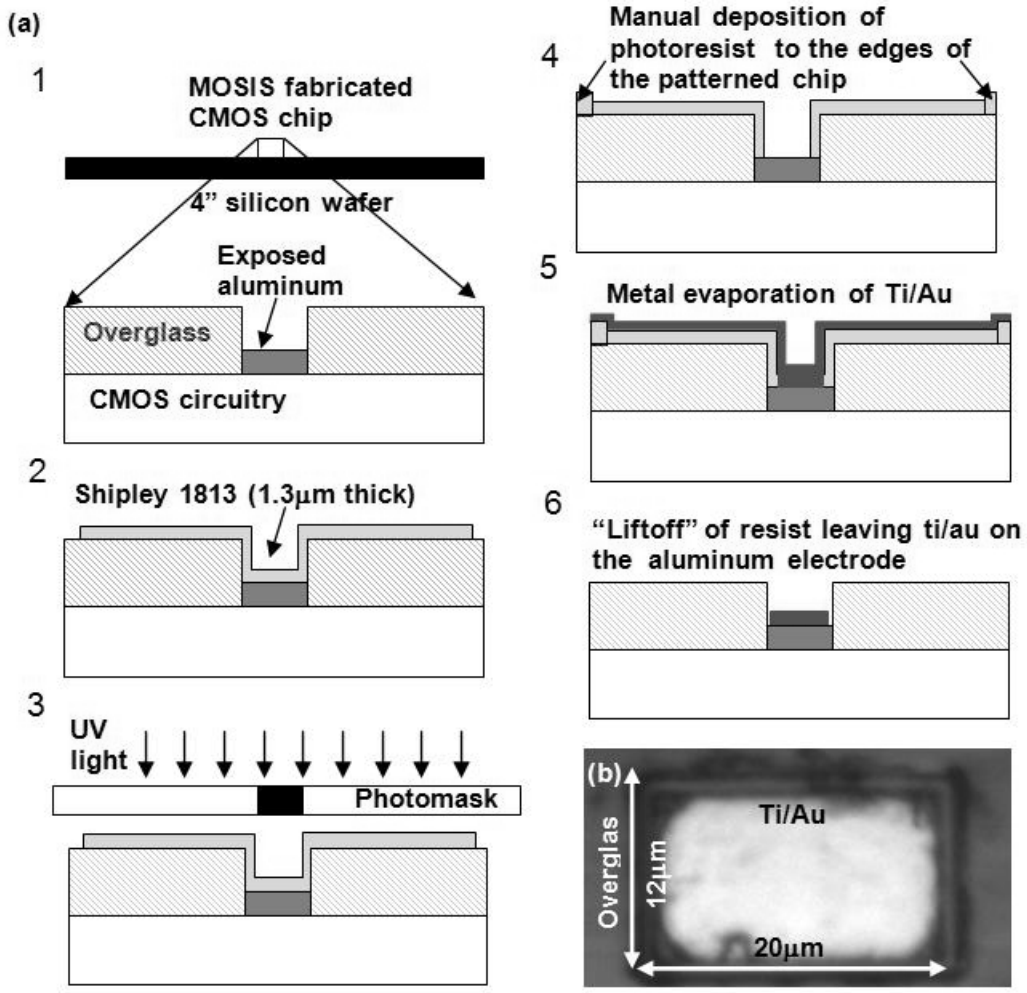

Figure 5.3: (a) Schematic of the process flow for deposition of polarizable material on aluminum electrodes. There are six steps associated with the post-CMOS fabrication using photolithography. In the first step, the CMOS die is placed on a 4" carrier wafer coated with photoresist and baked. The following steps illustrated in the figure do not show the carrier wafer. (b) Microscopic image of a single aluminum electrode coated with 10-nm Ti layer for adhesion and 200-nm Au layer.

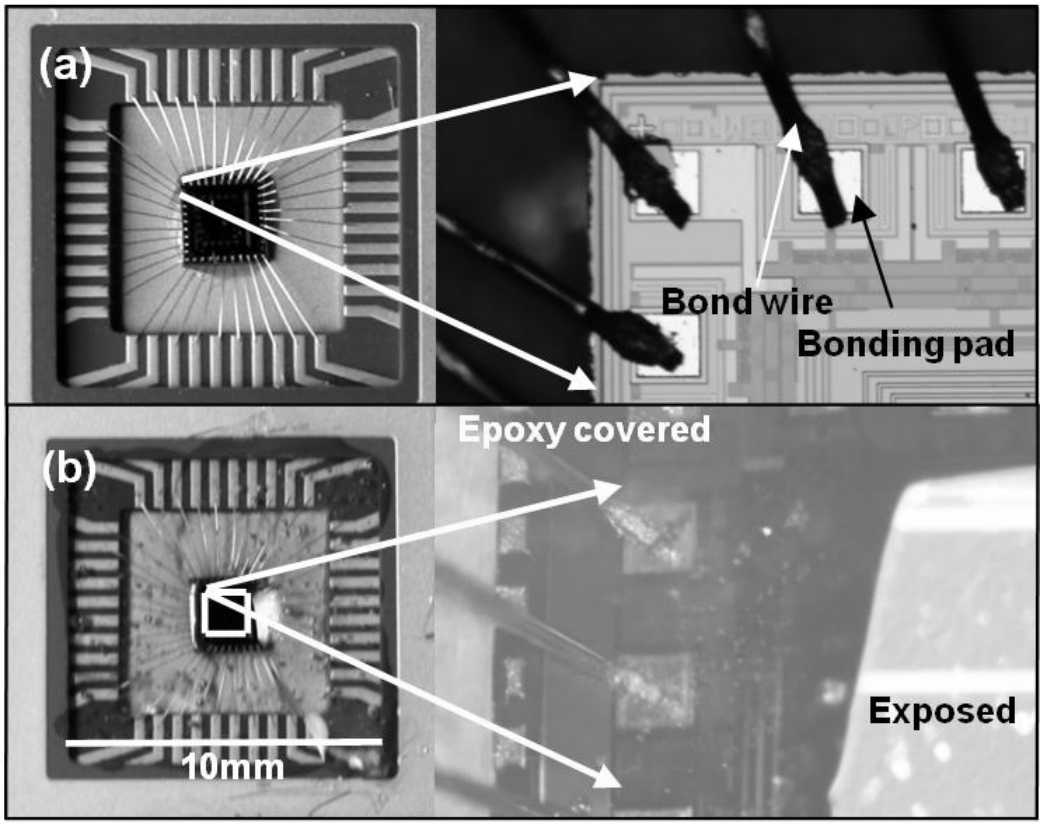

Figure 5.4: (a) A photograph of a CMOS chip in the package and a microscopic image of the bonding pads and wire bonds. (b) Photograph of the CMOS chip covered with epoxy excluding the boxed area. Microscopic image showing the epoxy covered and exposed areas.

neath the RF powered and ground shelf. Plasma is generated between the RF powered and ground shelf. Heavy plasma gas ions pass through the perforated ground shelf onto the samples, balancing the lighter electrons on the ground shelf and preventing surface charge buildup on the sample. The metal (Pt or Au) was vapor deposited over the entire surface. The next step was to lift-off photoresist along with the metal leaving behind only the metal in direct contact with the Al pads. The deposited metal forms the new electrode surface.

5.2.3 Packaging

The CMOS die was epoxy glued to a dual-inline package (DIP), as shown in Fig. 5.4(a). The package cavity along with the die was subsequently covered with epoxy (Devcon 5 minutes) to protect the sensitive bonding pads, wire bonds and connecting wires from contact with the electrolyte solution. Only the central part of the chip (inside the square in Fig. 5.4(b)) is left open, exposing only the surface of the CMOS die with electrodes (Fig. 5.4(b)). The layout of the chip was designed such that the electrodes are positioned in the center of the chip, spatially well separated from the I/O pads to avoid the epoxy encapsulating the active electrode area.

5.3 Experimental Results

The first measurements of catecholamine release from chromaffin cells were performed with a CFE externally connected to the CMOS chip. A CFE extending from a pipette is positioned on the cell, as shown in Fig. 5.5. The pipette was filled with 3-M KCL. A Ag/AgCl wire placed in the same pipette translates ionic current to electronic current. The Ag/AgCl wire was connected to the input of the potentiostat circuit, which maintained the CFE at 0.7 V. A second pipette filled with a bath solution containing 20-μM calcium ionophore ionomycin is positioned close to the cell. The cell was stimulated by ejecting ionomycin and the amperometric current that was recorded is shown in Fig. 5.5. Two events are shown on expanded scales with the fits from spike parameter analysis. The spike parameters are within the range previously reported [17–19]. The amperometric current indicates the time course of the catecholamine release from the cell.

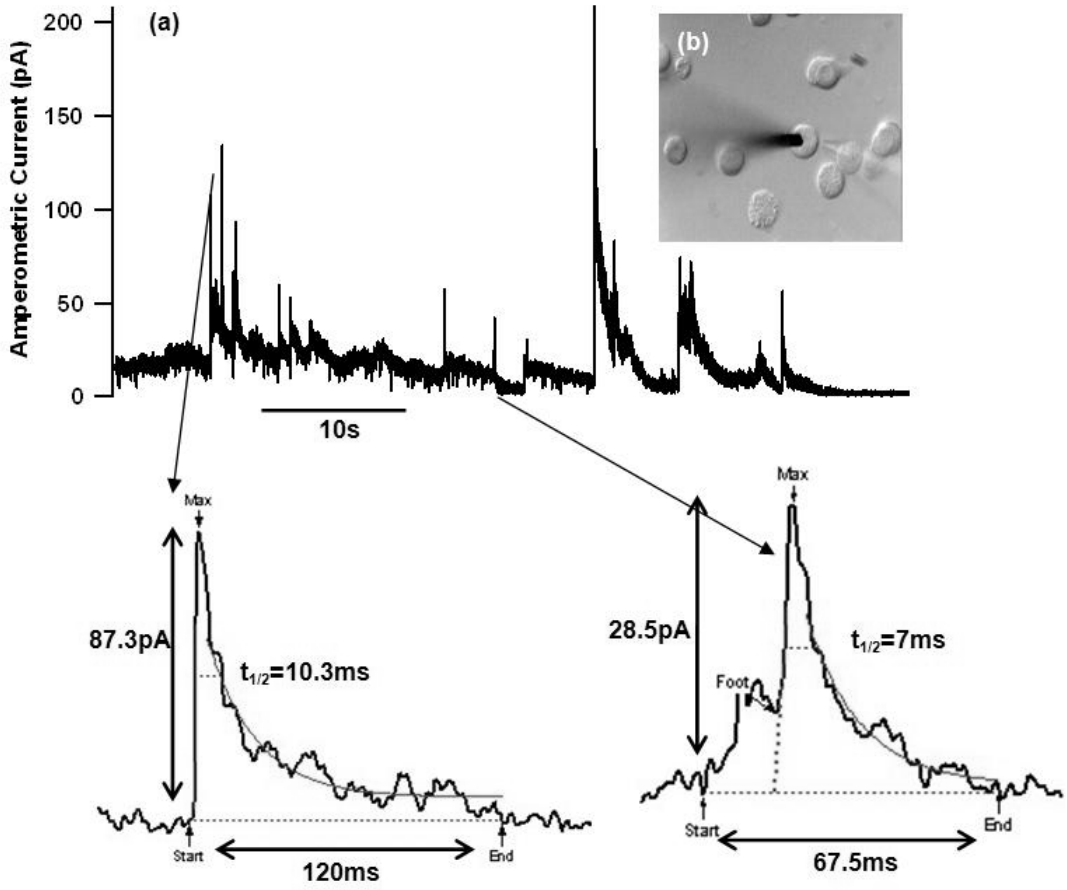

Figure 5.5: (a) Amperometric current trace of catecholamine release. Two events (smoothed) of varying amplitudes and half-widths on expanded scales with fit lines from the spike parameter analysis. (b) Microscopic image of the carbon-fiber-electrode touching the cell and another pipette with 20-μM ionomycin positioned close to the cell.

The current exhibits spikes as well as considerable fluctuations. Near the end of the recording, the current approaches zero and the fluctuations cease. The rms noise at the end was $\approx$0.3 pA, somewhat higher than the electronic noise previously reported (section 4.2) [11], which is presumably due to the antenna effect of the CFE and the connecting wire. During the release phase, the current fluctuations had increased to $\approx$1.65 pA rms at 2.5 kHz. The additional fluctuations thus appear to reflect actual fluctuations in local dopamine concentration at the CFE. The measured current was analyzed using the software program IGOR PRO

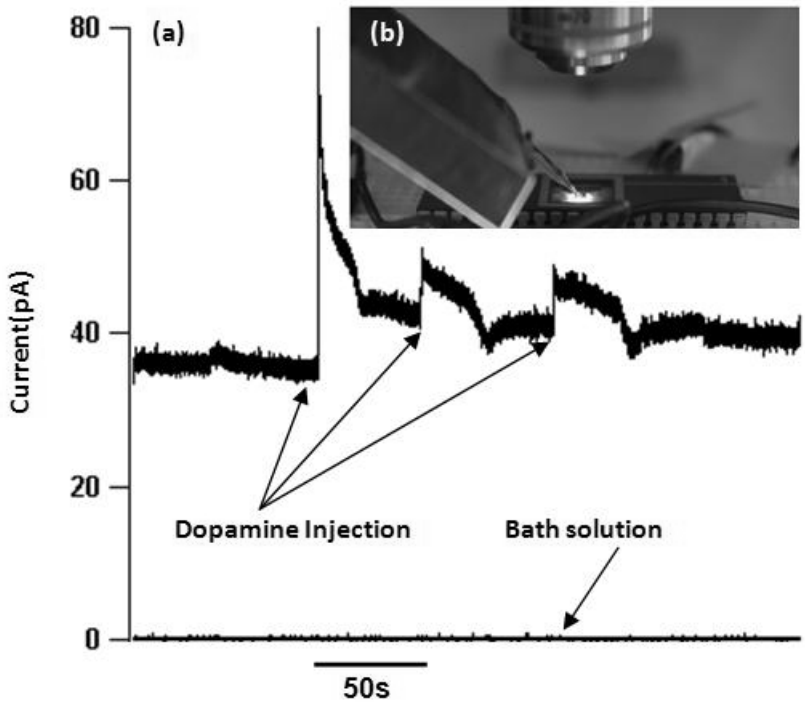

Figure 5.6: (a) Two current traces recorded by ejecting 50-μM concentration dopamine and bath solution. (b) Experimental setup showing the solution filled pipette with the ground electrode ejecting solution on the electrode.

(Wave Metrics, Lake Oswego, OR). Event detection and analysis was performed automatically using the IGOR procedure Quanta_Analysis_ver.ipf (downloadable at `www.sulzerlab.org/download.html`) [16].

5.3.1 On-Chip Dopamine Experiments

The exposed cavity of the chip (white box shown in Fig. 5.4(b)) was filled with $\approx 20\,\mu$L of bath solution. Glucose was not added to the bath solution for dopamine

experiments. A micropipette containing bath solution supplemented with 50-μM dopamine was immersed and positioned over the electrodes (Fig. 5.6(b)). Using a picospritzer, small amounts of solution were ejected from the pipette onto the Pt electrode. The Ag/AgCl reference electrode was located inside the ejection pipette. Application of bath solution did not produce detectable current (Fig. 5.6(a), lower trace). The rms noise level of the current trace was $\approx 0.1\,\mathrm{pA}$ at $2.5\,\mathrm{kHz}$. In contrast, ejection of dopamine solution produced clear amperometric responses to the dopamine ejections. The background current is presumably due to dopamine leaking from the ejection pipette before pressure pulses were applied. The rms noise level was $\approx 0.56\,\mathrm{pA}$ at $2.5\,\mathrm{kHz}$. The shot noise associated with a current I is given by

$$I_{\mathrm{rms}} = \sqrt{2qI\triangle f}$$

where q is usually the charge of an electron e_0. However, for dopamine oxidation, the unit is twice that carge, because two electrons are transferred for every detected dopamine molecule. The bandwidth $\triangle f$ for an averaging time interval τ is $\triangle f = 1/(2\tau)$. In this recording, with $\tau = 400\,\mu s$, the rms noise current is given by

$$I_{\mathrm{rms}} = \sqrt{\frac{2e_0 I}{400^{-6}}} = 2.8 \times 10^{-8}(\sqrt{A})\sqrt{I}$$

For a current of $40\,\mathrm{pA}$ (Fig. 5.6), the rms shot noise is $0.18\,\mathrm{pA}$, which only partially accounts for the observed $0.56\,\mathrm{pA}$ noise in the recording.

5.3.2 On-Chip Cell Experiments

To demonstrate on-chip recording of single-release events, a wide-tipped pipette, approximately 100-200 μm, was filled with physiological saline containing suspended adrenal chromaffin cells and was positioned close to the electrodes, similar

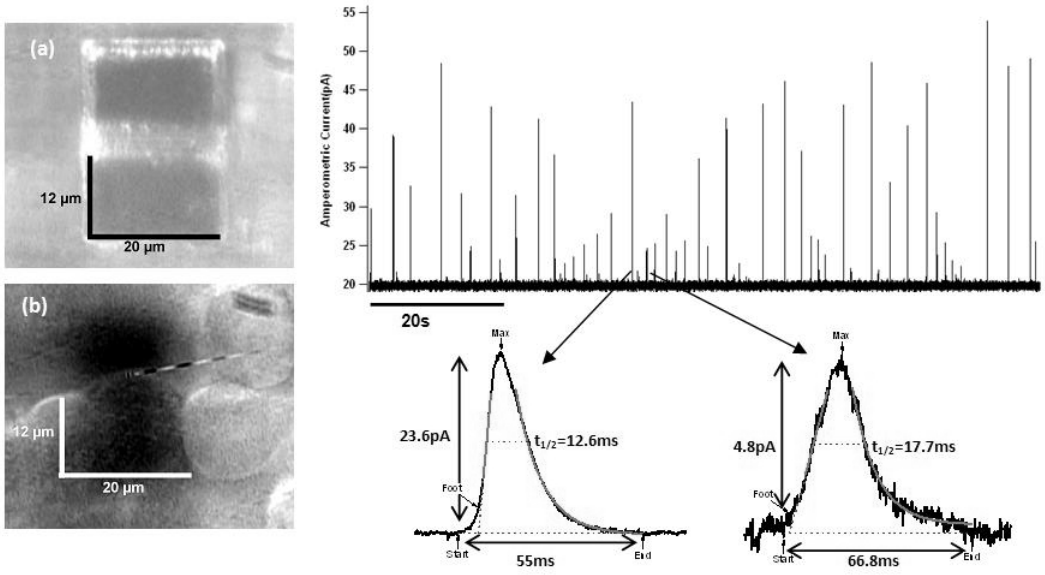

Figure 5.7: (a) Microscope image of on-chip Pt electrode dimensions. (b) Bovine chromaffin cells dropped onto the chip surface. The image was taken for demonstration purposes only and not during actual experimentation. Cells were released onto the electrodes and a water immersion objective focused on the cells. In the background electrodes can be seen as dark shadow. (c) Amperometric current trace showing spikes of variable amplitude up to ≈ 55 pA. Two events on expanded scales with fit lines from the spike parameter analysis.

to the dopamine experiments described earlier. Gentle pressure was applied allowing the cells to move out of the pipette tip and settle randomly on the surface (Fig. 5.7(a)). To stimulate the cells, a small volume of a solution containing the calcium ionophore ionomycin at 20-μM concentration was added from a 10-μL pipette and amperometric currents were recorded. Most experiments showed no amperometric spikes, presumably because no cell had settled onto the recording electrode. However, amperometric spikes were recorded in a few successful experiments, as shown in Fig. 5.7(b). The trace shows amperometric spikes as expected for a series of release events. Two events of different amplitudes are shown on expanded scale with peak currents of 23.6 pA and 4.8 pA, respectively. The noise is considerably less ($\approx$0.17 pA rms) than for the electrochemical measurements of dopamine and

for the off-chip carbon-fiber measurements. This could be attributed to the proximity of the cell to the electrode. Event detection and analysis was performed automatically and the detection threshold for the events was set to 1.4 pA, four standard deviations of the average baseline current. For the two expanded events the theoretical fits for spike parameter determination are also shown Fig. 5.7(b). Statistical analysis of the 46 detected events revealed a median full width at half maximum of 12.8 ms and median peak current amplitude of 10.28 pA. These values are consistent with typical parameters of amperometric measurements of individual catecholamine release events from bovine chromaffin cells [17–19]. During the experiment, direct observation of cells through the microscope was difficult due to the curvature of the solution meniscus and the ionomycin application. However, these results suggest that a cell was presumably attached on or positioned very close to the electrode and that these events reflect single exocytotic events. However, in contrast to conventional carbon-fiber recordings, we observed few events which exhibited an extended pre-spike foot signals, which would normally be expected to occur among these events. An alternative possibility would be that the recorded events reflect release from vesicles that were liberated intact from damaged cells and which burst upon contact with the electrode. At this stage, the feasibility of on-chip recording of single vesicle release events with high resolution was demonstrated by proof of principle.

REFERENCES

[1] Jenkner, M., Tartagni, M., Hierlemann, A., Thewes, R., "Cell-based CMOS sensor and actuator arrays," *IEEE Journal of Solid-State Circuits,* vol. 39, no. 12, pp. 2431-2437, 2004.

[2] Eversmann, B., Jenkner, M., Hofmann, F., Paulus, C., Brederlow, R., Holzapfl, B., Fromherz, P., Merz, M., Brenner, M., Schreiter, M., Gabl, R., Plehnert, K., Steinhauser, M., Eckstein, G., Schmitt-Landsiedel, D., Thewes, R., "A 128x128 CMOS biosensor array for extracellular recording of neural activity" *IEEE Journal of Solid-State Circuits,* vol. 38, no. 12, pp. 2306-2317, 2003.

[3] Schienle, M., Paulus, C., Frey, A., Hofmann, F., Holzapfl, B., Schindler-Bauer, P., and Thewes, R., "A fully electronic DNA sensor with 128 positions and in-pixel A/D conversion" *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2438-2445, 2004.

[4] Milgrew, M. J., Riehle, M. O., Cumming, D. R. S., "A 16x16 CMOS Proton Camera Array for Direct Extracellular Imaging of Hydrogen-Ion Activity," *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International,* pp. 590-638, Feb. 2008.

[5] M. Stanacevic, K. Murari, N. V. Thakor, and G. Cauwenberghs, "VLSI Potentiostat Array With Oversampling Gain Modulation for Wide-Range Neurotransmitter Sensing," *IEEE Transactions on Biomedical Circuits and Systems,* vol. 1, no. 1, pp. 63-72, March 2007.

[6] H. S. Narula and J. G. Harris, "A Time-Based VLSI Potentiostat for Ion Current Measurements," *IEEE Sensors Journal*, vol. 2, pp. 239-247, April 2006.

[7] H. S. Narula, J. G. Harris, "Integrated VLSI Potentiostat for Cyclic Voltammetry in Electrolytic Reactions," *Proceedings of the IEEE Computer Society Annual Symposium on VLSI Emerging Trends in VLSI Systems Design (ISVLSI'04),* pp. 268-270, 2004.

[8] Genov, R., Stanacevic, M., Naware, M., Cauwenberghs, G., Thakor, N. V., "16-Channel Integrated Potentiostat for Distributed Neurochemical Sensing," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 53, no. 11, pp. 2371-2376, 2006.

[9] K. Murari, M. Stanacevic, N. V. Thakor, and G. Cauwenberghs, "Wide-range,Picoampere-Sensitivity Multichannel VLSI Potentiostat for Neurotransmitter Sensing," *Proceeding of the 26th Annual International Conference of the IEEE EMBS,* pp. 4063-4066, San Francisco, CA, 2004.

[10] Laiwalla, F., Klemic, K. G., Sigworth, F. J., Culurciello, E., "An Integrated Patch-Clamp Amplifier in Silicon-on-Sapphire CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 53, no. 11, pp. 2364-2370, 2006.

[11] Ayers, S., Gillis, K. D., Lindau, M., Minch, B. A., "Design of a CMOS potentiostat circuit for electrochemical detector arrays," *IEEE Transactions on Circuits and Systems I-Regular Papers,* vol. 54, no. 4, pp. 736-744, 2007.

[12] Parsons, T. D., Coorssen, J. R., Horstmann, H., Almers, W., "Docked granules, the exocytic burst, and the need for ATP hyd rolysis in endocrine cells," *Neuron,* vol. 15, 1085-1096, 1995.

[13] D. R. Crow, *Principles and applications of electrochemistry,* New York : Blackie Academic & Professional, 1994.

[14] C. H. Chow, Rüden in (B. Sakmann and E. Neher, eds.), *Single Channel Recording,* New York:Plenum Press, 1995.

[15] Giannuzzi, Lucille A., Stevie, F. A., *Introduction to focused ion beams : instrumentation, theory, techniques, and practice,* New York:Springer, 2005.

[16] Mosharov, E. V., and D. Sulzer, "Analysis of exocytotic events recorded by amperometry," *Nat Methods,* vol. 2, pp. 651-658, 2005.

[17] Gong, L. W., G. Alvarez De Toledo, and M. Lindau, "Secretory vesicles membrane area is regulated in tandem with quantal size in chromaffin cells," *Journal of Neuroscience,* vol. 23, no. 21, pp. 7917-7921, 2003.

[18] A. Albillos, G. Dernick, H. Horstmann, W. Almers, G. Alvarez de Toledo, and M. Lindau, "The Exocytotic Event in Chromaffin cells Revealed by Patch Amperometry," *Nature,* vol. 389, pp. 509-512, 1997.

[19] Chow, R. H., L. v.'Rden, and E. Neher, "Delay in vesicle fusion revealed by electrochemical monitoring of single secretory events in adrenal chromaffin cells," *Nature,* vol. 356, pp. 60-63, 1992.

CHAPTER 6

CMOS BIONSENSOR ARRAY DESIGN

In the previous chapter, I described post-CMOS fabrication methods, and demonstrated by proof of principle, measurements of chatecholamine release. The next stage of the project was to demonstrate array operation by performing simultaneous measurements. In this chapter, I will describe the architecture and operation of the timing circuitry that will be used to operate an $n \times n$ array. I will present evidence of array operation by showing simultaneous electrochemical measurements from a 4×4 electrode array. In Section 6.3, I will describe the architecture of a hybrid chip that comprises of an 8-electrode linear array a 100-electrode 2-D array. In Section 6.3.1, I will describe a biasing scheme that is capable of tuning the gain and bandwidth of the feedback amplifiers in order to use the potentiostat for a wider range of applications. This system-level architecture was successfully simulated and the simulation results will be presented.

6.1 Timing

The architecture of an $n \times n$ array is shown in Fig. 6.1(a). There are three sets of switches in the array: a set of reset switches S_{1x}, per column, per row; a set of column select switches S_{2x}, per column, per row; a set of clamping switches S_{3x} per row. All the rows are identical, and the output of each row is buffered onto an input channel of an n-channel A/D converter. It is possible to multiplex the output of all the rows on a single output line. However, this scheme was employed because of availability of multi-channel A/D converters and to avoid using a high frequency clock on chip.

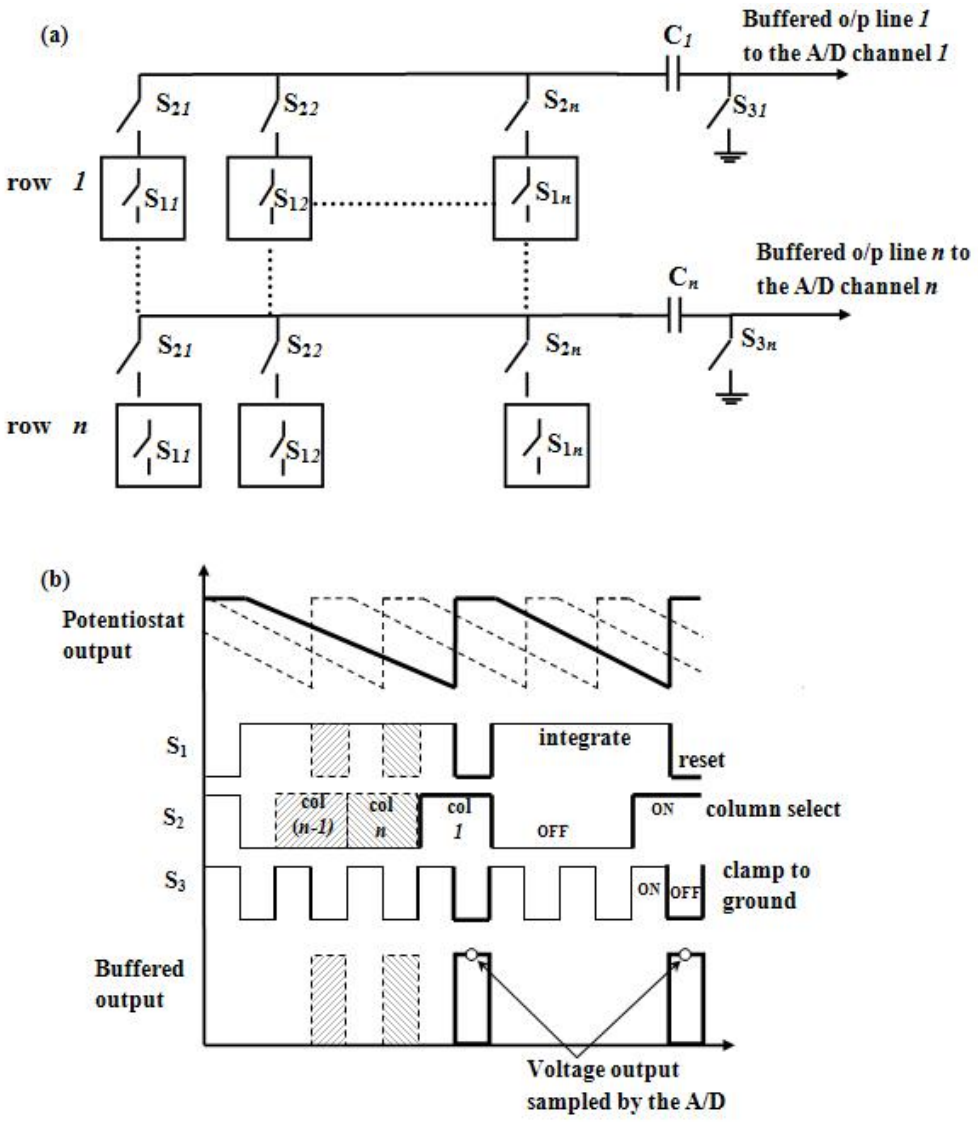

Figure 6.1: (a) The box represents a potentiostat circuit, with a reset switches S_{1x}, where $x = (1, 2...n)$. The set of switches S_{2x}, represent the column select switches, where $x = (1, 2...n)$. The switch S_{3x} clamps the capacitor C_x to ground to enable CDS operation, where $x = (1, 2...n)$. All rows in the array are identical. The output from each row is buffered onto the several lines of multi-channel A/D converter. (b) The first trace is the output of the potentiostat circuit, which is in "integrate" state when the switch S_1 is high and "reset" state when low. The column switches S_{2x} and S_3 operate as described in Chapter 4. The bottom trace shows the output buffered onto a single channel of the A/D converter. The circles indicate the data points sampled by the A/D converter.

The switching signals of a single row are illustrated in Fig. 6.1(b). I will now describe the operation of the switching sequences in the context of a single row operation. The top trace in Fig. 6.1(b) is the buffered output of the potentiostat circuit. The reset switch S_{11} is used to reset the voltage across the capacitor to zero after the integration period. Before it is reset, S_{21} is switched ON selecting column x and charging the capacitor C_1 to the output voltage of array unit 11. The switch S_3, is turned OFF, at the instant when the integrating capacitor is reset. The voltage across the capacitor subsequently represents the charge integrated (see Section 4.3).

The frequency of the clamping signal is n times the frequency of the reset pulse, and the pulse width of the column select signal is twice that of the reset pulse (Fig. 6.1). These pulses were generated by the architecture shown in Fig. 6.2, by using a shift register and combinational logic gates. The reset pulse and the master clock are generated using off-chip components. A CMOS shift cell [1, 2] operating on a single-phase clock signal alternating between high and low is used as the building block of the shift register, instead of a two-phase nonoverlapping-clock-operated shift cells. The main reset pulse is shifted through two shift cells to generate the reset pulses for various rows, from which the column select and clamp signals are derived, as shown in Fig. 6.2.

6.2 4×4-Electrode Array

A 4×4-electrode array was fabricated in $0.5 - \mu m$ AMIS C5F technology through MOSIS. The layout of the design is shown in the inset of Fig. 6.3(a) and Fig. 6.3(c). This array was operated using the timing scheme described in the earlier section.

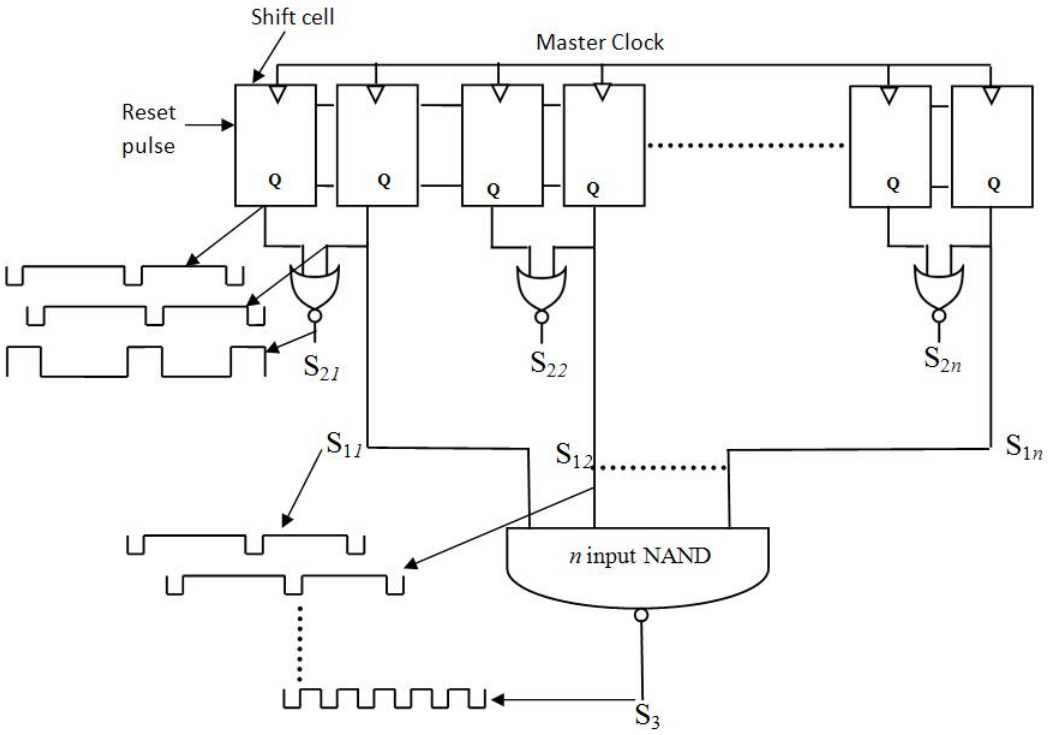

Figure 6.2: The timing system contains $2n$ shift registers, n 2-input NOR gates and one n-input NAND gate.

The bias currents, in this case, were provided by Keithley 236 source measurement units. The sensing electrodes in this test chip were located inside the periphery of the pad frame. To test the array operation, gold electrodes were fabricated using lithography as described in Chapter 5. Amperometric current fluctuations in response to dopamine released from a wide-mouthed pipette were observed, as shown in Fig. 6.3(a). Peak current fluctuations and time course of fluctuations are shown on an expanded scale in detail in Fig. 6.3(c). The ejection profile of dopamine is shown in Fig. 6.3(b) by scaling the grey-scale bar using the normalized peak current. Fig. 6.3(b) clearly shows a directional flow of dopamine to the left corner of the chip.

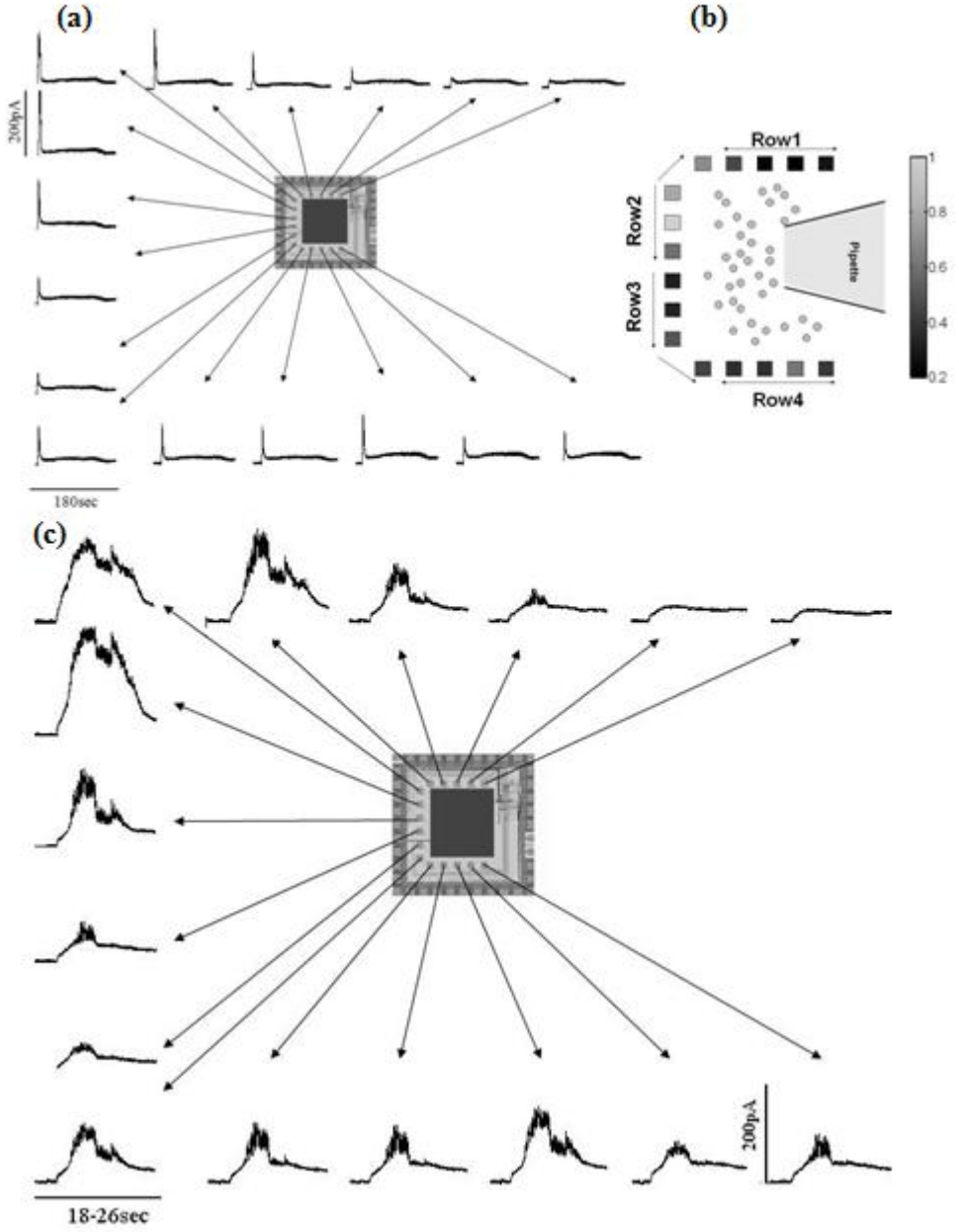

Figure 6.3: (a) Amperometric current fluctuations due to dopamine release. (b) Normalized peak currents are shown on a grey-scale bar. (c) Peak current fluctuations on an expanded time scale.

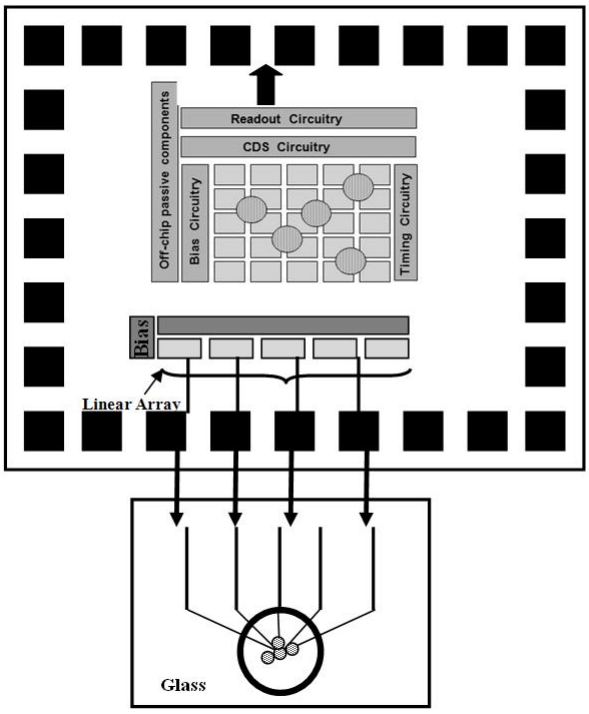

Figure 6.4: System architecture of a hybrid chip comprising of a one-dimensional linear array and a two-dimensional array. A linear array with external inputs may be used to perform experiments (e.g. TIRF) that requires substrates other than silicon, a glass substrate is shown here.

6.3 Hybrid Chip Architecture

In the next stage of the project, a hybrid chip comprising a linear array with external inputs for off-chip experimentation, and a 2-D array for on-chip experimentation, was designed, which I will describe here. This chip represents an improvisation over the previous two designs (Chapter 4, Section 6.2) in that it requires no external instrumentation, and only requires off-chip components, and can be used with a battery for a considerable time, due to its low power consumption.

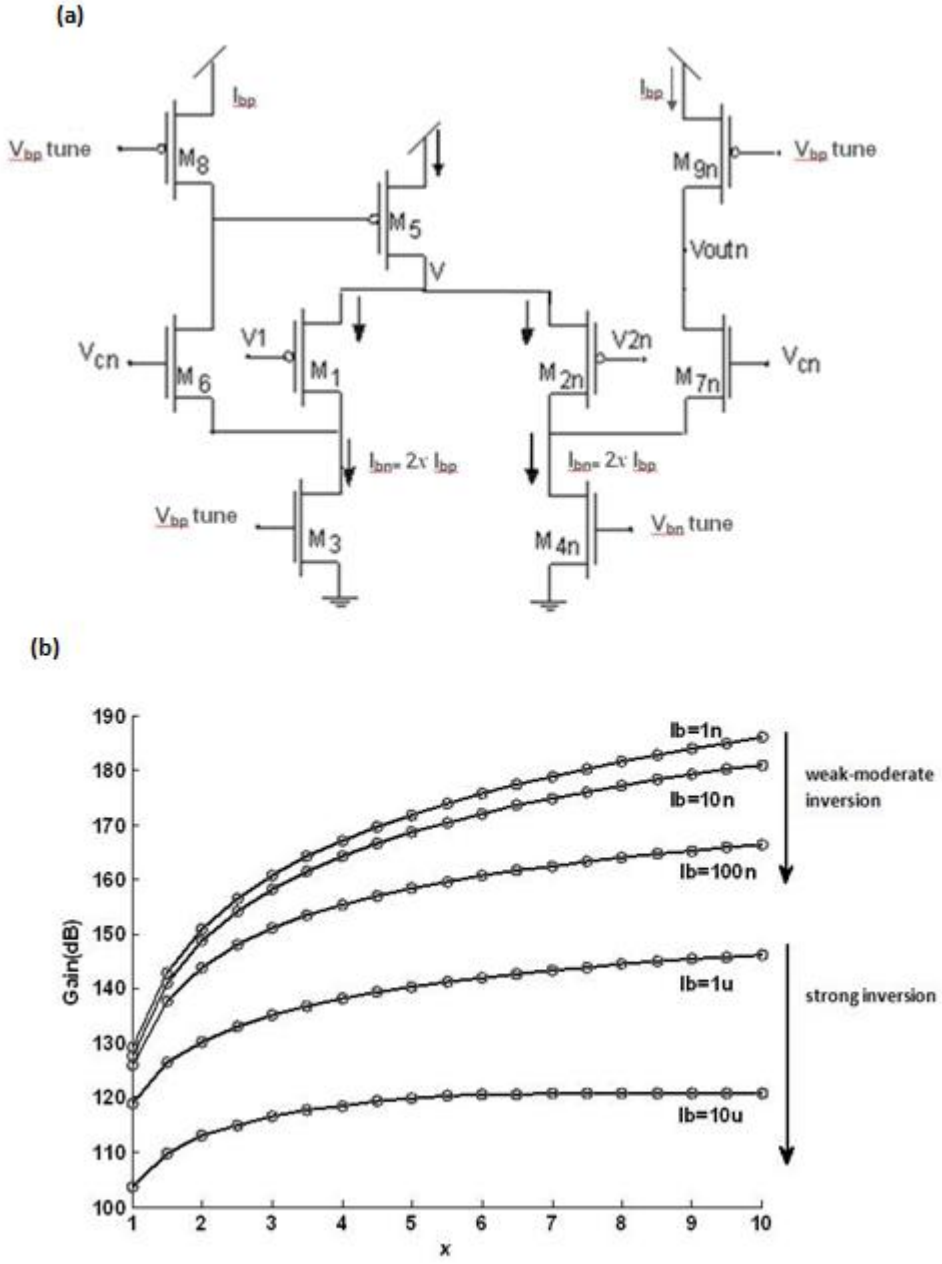

Figure 6.5: (a) The regulated-cascode feedback amplifier with a tunable p-bias V_{bp} and a tunable n bias V_{bn}. By tuning the bias voltages, parameters such as gain, bandwidth, power consumption, and noise performance can be optimized (b) As the ratio of $I_{rm2n} : I_{rm9n}$, x, is increased, g_{m2n} increases, increasing the gain. As I_{9nsat} is increased, r_{o9n} decreases leading to a reduction of gain.

6.3.1 Bias Current Generator

For the biosensor to operate independent of external instruments and sources, a bias current generator is necessary. The potentiostat array can used for various purposes including sensing fast changes in neurotransmitter release (mouse chromaffin cells), cyclic voltammetry, and CMOS imagers. It is therefore, desirable to tune the gain and bandwidth of the feedback amplifier. The regulated-cascode amplifier described in Chapter 4 can be biased to operate from subthreshold to above threshold. By tuning the bias voltages $V_{\rm bp}$ and, $V_{\rm bn}$ of the folded-cascode feedback amplifier shown in Fig. 6.5(a), the gain of the amplifier can be varied. The gain of the regulated-cascode amplifier is $g_{\rm m2}{}_n r_{\rm o9}{}_n$. In weak-inversion mode, $g_{\rm m2n} \propto I_{\rm sat}$, and in strong-inversion mode, $g_{\rm m2n} \propto \sqrt{I_{\rm sat}}$. The Early effect resistor $r_{\rm o9n} \propto \frac{1}{I_{\rm sat}}$. Hence, by biasing the current such that $I_{\rm 2n} \gg I_{\rm 9n}$, the gain can be varied by as much as 80 dB as shown in Fig. 6.5(b).

A bias current generator with a wide dynamic range, independent of supply voltage and process technology has been developed [3, 4] for various applications. This bias current generator spans six decades of current. The basic building block of this bias current generator is a *bootstrapped current reference* [5–10], shown in Fig. 6.6. The master current I_m is forced to be mirrored in $M_{\rm n1}$-$M_{\rm n2}$ by the current mirror pair $M_{\rm p1}$-$M_{\rm p2}$. However, the strength ratio of $M_{\rm n1}$-$M_{\rm n2}$ is M:1. In order for both the transistors to sink the same current, there has to be a voltage drop across resistor R. In weak inversion region,

$$\begin{aligned} I_{\rm n1} &= I_{\rm n2} \\ M I_{\rm s} e^{\kappa(V_{\rm n} - I_{\rm m} R)/U_{\rm T}} &= I_{\rm s} e^{\kappa V_{\rm n}/U_{\rm T}} \\ I_{\rm m} &= \ln(M)\frac{U_{\rm T}}{R}. \end{aligned} \tag{6.1}$$

In the strong inversion region, the current can be approximated (neglecting the

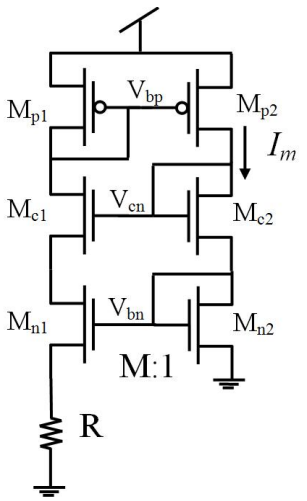

Figure 6.6: Schematic of the bootstrapped bias generator. The voltage across the off-chip resistor R sets up the current I_m in the bias generator. The bias current does not depend on the power supply or other process parameters.

Early effect resistor) by the saturation current $I_{\rm sat}$

$$\begin{aligned} I_{\rm n1} &= I_{\rm n2} \\ M\frac{\beta_{\rm n1}}{2\kappa}\left(\kappa\left(V_{\rm bn}-V_{\rm T0}\right)-I_{\rm m}R\right)^2 &= \frac{\beta_{\rm n2}}{2\kappa}\left(\kappa\left(V_{\rm bn}-V_{\rm T0}\right)\right)^2 \\ I_{\rm m} &= \frac{2}{\beta_{\rm n2}R^2}\left(1-\frac{1}{\sqrt{M}}\right)^2 \end{aligned} \tag{6.2}$$

where $\beta_{\rm n} = \mu_n C_{\rm ox}\frac{W_{\rm n}}{L_{\rm n}}$. From Eq. 6.1 and Eq. 6.2, it is evident that the bias current is independent of power supply voltage. Individual biases $V_{\rm bp}$ and $V_{\rm bn}$ can be generated, as shown in Fig. 6.7(a) and Fig. 6.7(b). Fig. 6.7(c) shows that bias current spans over six decades by varying the resistor R.

For proper operation, a bypass capacitor terminated by the appropriate power rail is usually connected to the generated bias voltage $V_{\rm bn}$ and $V_{\rm bp}$ to prevent noise on the line due to power supply ripples and noise coupling from other signal lines. Therefore, these nodes must be brought out to bonding pads to connect off-chip bypass capacitors.

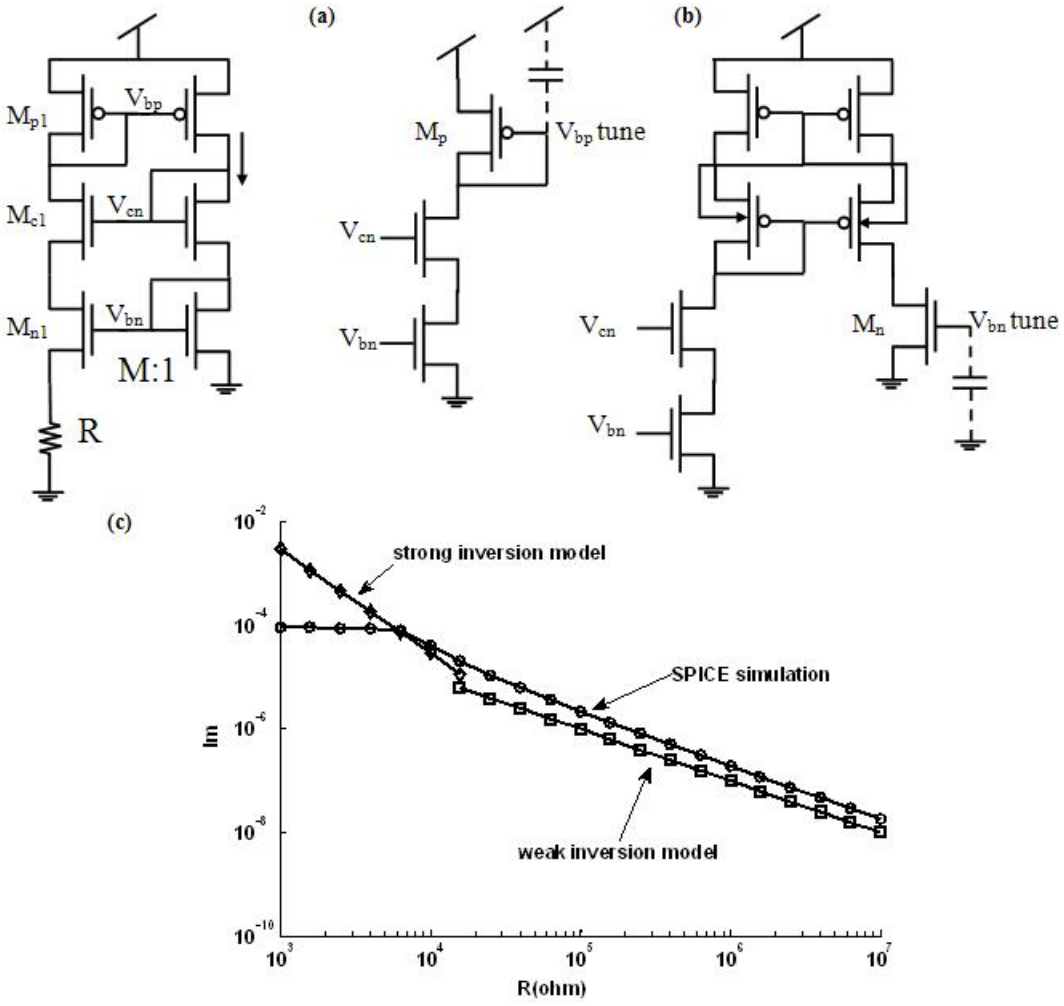

Figure 6.7: (a) Schematic circuit of an individual p-type bias. (b) Schematic circuit for an individual n-type bias. A bypass capacitor terminated by the appropriate power rail is usually connected to the bias voltage to prevent noise on the line due to power supply ripples and other signal lines coupling noise. (c) Spice simulation results and the traces according to Eq. 6.1 and Eq. 6.2

The boot strapped bias circuit (Fig. 6.6) is, in theory, a self-starting circuit. However, it could settle to a stable state of zero current. In order to prevent this state of operation, a start-up circuit was used [4]. Design kits and extensive literature on the subject, provided by Dr. Delbrück, are available at `http://jaer.wiki.sourceforge.net/biasgen`.

6.3.2 Linear Array

The schematic of the linear array is shown in Fig. 6.8. The linear array contains 8 units, each unit comprising the potentiostat and CDS circuits represented by P_x, where x is (1,2...8) (Fig. 6.8(a)). The linear array is designed to be used along with off-chip microfabricated devices, therefore, there is no limitation on layout area. Individual CDS circuits were included in every array unit. Dummy units were laid out on either side of the the end array units, to enable better matching [15]. A calibration unit was also included to measure a current-voltage characteristic, using which the output voltage is converted to current. To get an accurate calibration curve, a *active current mirror* M_{n1}-M_{n2}, shown in Fig. 6.8(a) was used. As described in Chapter 3, the quiescent current of the MOS transistor is a function of the drain-source voltage due to the Early effect. A simple current mirror was replaced by the active current mirror [11–13]. The advantage of using the active current mirror is that the input voltage can be fixed independent of the mirroring device gate voltage. By keeping the mirror output and input terminals at the same potential, systematic mismatch due to the Early effect was eliminated.

The cell-solution interface was modeled as a 50-100 pF capacitor in parallel with a current source carrying an amperometric spike of magnitude 25 pA and half-width of ≈10 ms, shown by the solid line curves in Fig. 6.9. The same current

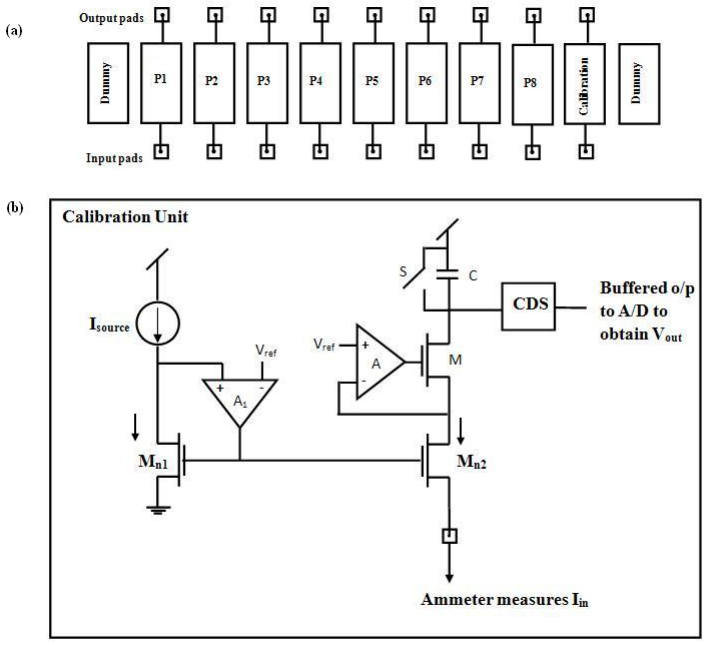

Figure 6.8: (a) Schematic of the linear array. Dummy units were laid out to produce better matching of current-voltage characteristics of all the elements in the array. (b) Schematic of the calibration unit. The calibration unit was used to characterize the $I_{\rm in}$ vs $V_{\rm out}$ characteristic.

Table 6.1: Performance Specifications of the Linear Array

$I_{\rm bn}$	$log(M)U_{\rm T}/R$	500 nA
$I_{\rm bp}$	$log(M)U_{\rm T}/R$	100 nA
$g_{\rm m2}$	$\kappa I_{\rm sat}/U_{\rm T}$	1.3×10^{-5}
$r_{\rm o9}$	$V_{\rm A}/I_{\rm sat}$	$\approx 6 \times 10^{8}$
Gain	$g_{\rm m2}r_{\rm o9}$	$\approx$ 180dB
Power consumption	$2I_{\rm bn}V_{\rm DD}$	$5\mu W$/unit
SNR	$I_{\rm signal}/I_{\rm noise}$	$\approx$ 90dB

source was connected to the inputs of all 8 units of the array with a successive delay of 10 ms for each unit and simulated for 150 ms. The results of this simulation are shown in Fig. 6.9. The output voltage measured was subsequently converted to current, which was in excellent agreement with input current. The simulations were performed by setting bias currents given in Table 6.1. Table 6.1 also lists the important performance specifications of the linear array. The power consumption

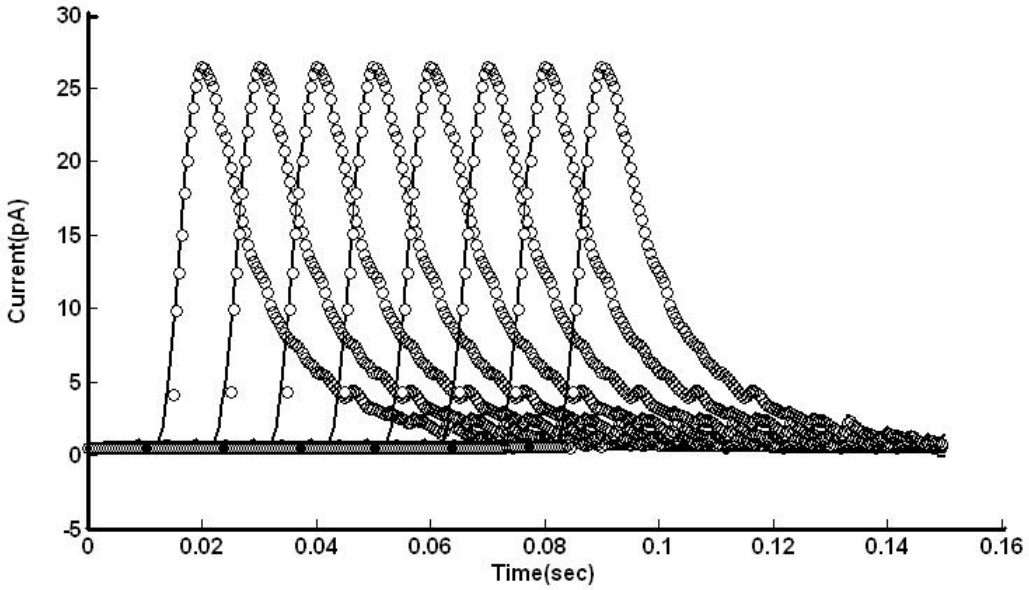

Figure 6.9: Simulation results of the 8-electrode linear array. The circles represent the simulated output, and the solid lines represent the input current.

per unit of the array is 5 μW. For the entire linear array, the power consumption would be half of the power consumed by a single unit times the number of units. Therefore, in an 8 unit array, the power consumption would be 22.5 μW.

6.3.3 2-D Array

The 2-D array has a different architecture from that of the linear array, as shown in Fig. 6.10. The 2-D array is a high-density array, and layout area restrictions apply. Hence, the CDS circuit is not included in the array units. Each row in the 2-D array shares half of the folded-cascode feedback amplifier, as described in Section 4.1. Each column in the 2-D array shares a CDS unit as described in Section 4.3. The calibration units in the 2-D array are similar to the units described in the previous section. A similar simulation experiment to the one

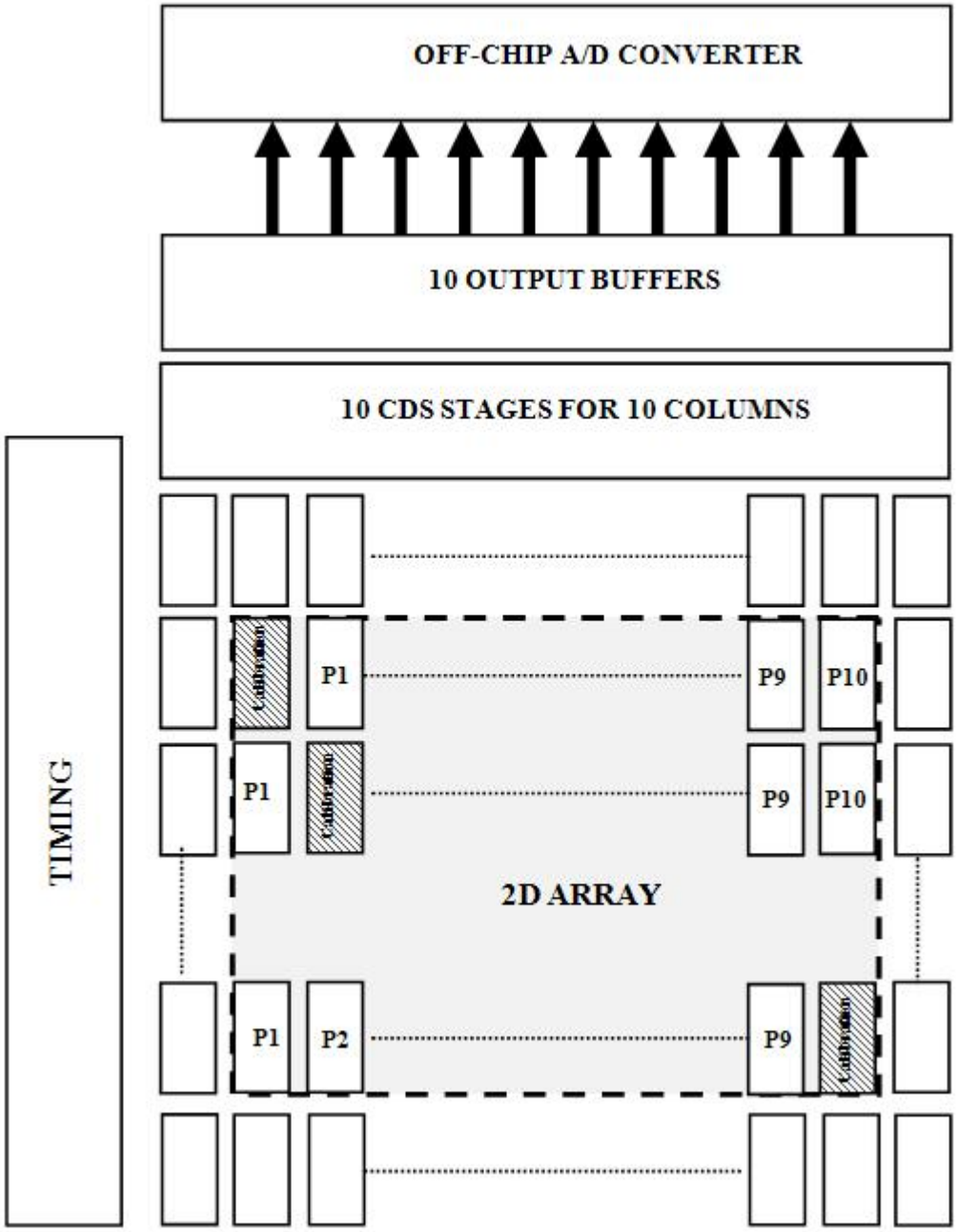

Figure 6.10: Schematic layout of the 2-D array. Dummy units were placed along the periphery of the array units. A calibration unit was placed in every row diagonally in the array to characterize the matching of all the units in the array.

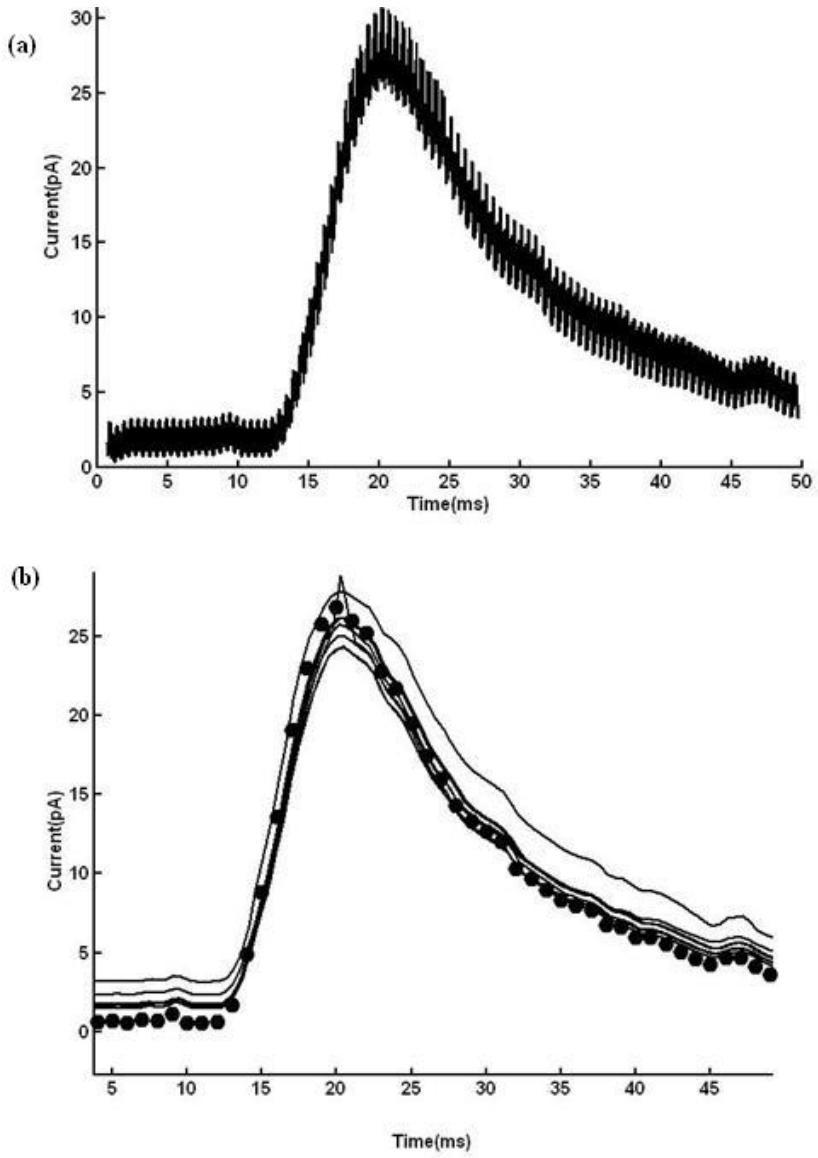

Figure 6.11: Simulation results of the 2-D array: (a) The output line comprising of samples from all the rows. (b) The output current sampled from the several rows are shown in the solid lines and the circles represent the input current.

described in the previous section was performed on the 2-D array. However, the same amperometric current source was applied to the entire column to conduct the simulation at a reasonable speed. The output of the ten rows are multiplexed onto the same line. The output voltage from a single output line and the data from individual units in a column are shown in Fig. 6.11. This result indicates good agreement between the output and the input current.

Performance specifications similar to the linear array are attainable by the 2-D array. However, the 2-D array will exhibit additional noise due to switching noises from the additional switches that were used to operate the array.

In this chapter, the operation of the shared CDS readout circuit was demonstrated by simultaneous measurement of dopamine from a 16-electrode array. The hybrid array architecture was designed and simulated for measuring catecholamine release on the CMOS chip as well as from external substrates.

REFERENCES

[1] M.A. Sivilloti, M.A. Mahowald, and C.A. Mead, "Real-time visual computations using analog CMOS processing arrays," *Proceedings of the Stanford Cotfference on Very Large Scale Integration,* MIT Press: Cambridge, MA, pp. 295-311, 1987.

[2] M. Sivilotti, "Wiring considerations in analog VLSI systems, with application to field-programmable networks," *Ph.D. thesis,* Dept. of Computer Science, California Institute of Technology, Pasadena, CA, June 1991.

[3] T. Delbrück, A. van Schaik "Bias current generators with wide dynamic range" *Proceedings of the 2004 International Symposium on Circuits and Systems,* vol. 1, pp. I-337- I-340, 2004.

[4] T. Delbrück and A. van Schaik, "Bias current generators with wide dynamic range," *Analog Integrated Circuits and Signal Processing,* vol. 43, pp. 247-268, 2005.

[5] R. J. Widlar, "Some circuit design techniques for linear integrated circuits," *IEEE Transactions on Circuit Theory,* vol. CT-12, pp. 586-590, 1965.

[6] R. J. Widlar, "Design techniques for monolithic operational amplifiers," *IEEE Journal of Solid State Circuits,* vol. SC-4, pp. 184191, 1969.

[7] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits basedon weak inversion operation," *IEEE Journal of Solid-State Circuits,* vol. 12, pp. 224-231, 1977.

[8] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits,* Cambridge Univesity Press, 1998.

[9] B. Razavi, *Design of Analog CMOS Integrated Circuits,* McGraw-Hill Higher Education, 2000.

[10] R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation,* IEEE Press, 1998.

[11] A. S. Sedra and K. C. Smith, "A second generation current conveyor and its applications," *IEEE Trans. Circuit Theory,* vol. CT-17, pp. 132-134, Feb. 1970.

[12] B. Wilson, "Recent developments in current conveyors and current mode circuits," *IEE Proc., Pt. G,* vol. 137, pp. 63-77, Apr. 1990.

[13] C. Toumazou, F. J. Lidgey and D. G. Haigh, *Analogue IC Design: The Current-Mode Approach,* Peter Peregrinus Ltd. (IEE): London, 1990.

CHAPTER 7

CONCLUSIONS & OUTLOOK

In this work, a novel CMOS potentiostat array was designed, fabricated, post-processed and successfully tested. The performance of the RCA potentiostat circuit was comparable to the commercially available amplifiers that are used for amperomtery. A prototype chip was fabricated using the AMIS C5F 0.5 μm process through MOSIS. The rms noise of the single potentiostat measurements is $\approx$ 110 fA or 274 electrons at 2 kHz. The lowest noise is achieved by Axopatch 200B (Molecular Devices), which was 0.06 pA at 5 kHz. The RCA potentiostat circuit has an added advantage in that, it uses fewer components and is expandable into a scalable array enabling simultaneous experiments from many cells at the same time.

Off-chip and on-chip electrochemical measurements were successfully conducted. Off-chip amperometric measurements of catecholamine release from bovine chromaffin cells were performed by connecting a CFE to the input of the potentiostat. The rms noise measured was 0.3 pA at 2.5 kHz. The CMOS processing technologies use aluminum as the interconnect material. Aluminum is not suitable for electrochemistry. Therefore, two post-CMOS fabrication methods were employed to include transducers on the chip. The focused-electron beam method and the optical lithography method were successfully used to deposit platinum and gold electrodes on the aluminum electrodes. Subsequently, the chip was tested for on-chip electrochemical sensitivity. Successful on-chip measurements of dopamine release and catecholamine release were presented. The rms noise of the catecholamine measurements were shown to be 0.17 pA.

A prototype hybrid chip comprising of a large-scale 2-D array of 100 electrodes, and a 1-D array of 8-electrodes, was designed and simulated. The bias currents were generated using a wide-dynamic-range bias current generator, which operates independent of power supply and other processing parameters. A timing scheme was implemented to scan the each column sequentially. Accurate calibration units were included in each of the arrays. The simulation results show excellent agreement between the input current and output current.

In the end, this work forms a good foundation for developing high-density CMOS biosensor arrays for measuring catecholamine release. Looking forward, the fabrication methods employed successfully in this work could be applied to the hybrid chip. With better packaging methods, and built-in microfluidic channels, the CMOS arrays have a potential to position the cells, and measure the release events at a faster rate than CFE amperomtery. This biosensor array has the potential to allow testing at a rate hundred times faster than existing technology and at one-tenth the cost. It could lead to breakthroughs in drug discovery and subsequently the treatment of neurological disorders.

APPENDIX A

EKV MODEL PARAMETERS

EKV model parameters of MOS devices fabricated using AMIS C5F 0.5 μm process technology are listed in Table A.1 and Table A.2.

Table A.1: EKV model parameters for the nMOS transistor.

DL=-0.0636e-6	DW=-0.95e-6	VTO=0.6256
GAMMA=0.5027	PHI=0.4303	LETA=0.9871
WETA=0.0260	COX=0.0024	XJ=1.5E-7
KP=1.2809e-004	THETA=0.0692	UCRIT=2.5e6
LAMBDA=0.1454	CGSO=1.99E-10	CGDO=1.99E-10
CGBO=0.0	CJ=4.233802E-4	CJSW=3.825632E-10
MJ=0.4495859	MJSW=0.1083618	PB=0.9899238
PBSW=0.1082556	FC=0.5	TNOM=27.0

Table A.2: EKV model parameters for the pMOS transistor.

DL=-0.0575e-6	DW=-0.809e-6	VTO=-0.81
GAMMA=0.5117	PHI=0.5201	LETA=0.74
WETA=0.7104	COX=0.0024	XJ=1.5E-7
KP=3.0e-5	THETA=0.012	UCRIT=6.9e6
LAMBDA=1.0959	CGSO=2.4E-10	CGDO=2.4E-10
CGBO=0.0	CJ=4.233802E-4	CJSW=3.114708E-10
MJ=0.4959837	MJSW=0.2653654	PB=0.9665597
PBSW=0.99	FC=0.5	TNOM=27.0