Multifunction-timing card lTTEV2 for CoDaC Systems of Wendelstein 7-X

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Abstract– **The timing system is a crucial element for the CoDaC (Control, Data Acquisition, and Communication) system of the steady state fusion experiment Wendelstein 7-X (W7-X). Its main task is the synchronization of all clocks with sufficient accuracy. Furthermore, it is able to send, receive, and process event messages. It offers a wide range of time related functions, e.g., time capturing, pulse generation, realization of time delays, and sending and receiving of trigger signals. The overall timing system consists of a central timing system and a considerable number of local timing systems. A revision of the existing lTTEV1 and TDC cards was necessary as many components used for their fabrication were no longer available. The need for a bus interface for the lTTE card with long term availability has led to the decision to use a GBit Ethernet interface. By choosing a more powerful FPGA device, it was possible to increase the time resolution by a factor of two. This contribution starts with a short introduction of the W7-X timing system. The key properties, all extended as well as new features of the lTTEV2 card to face new requirements regarding data acquisition are described. The actual state of the development is given.**

I. Introduction

Wendelstein 7-X is a fusion experiment based on the stellarator concept [1]. The main goal of this project is to demonstrate the steady state capability of the stellarator fusion device.

The magnetic field for the plasma confinement will be produced by 50 non planar and 20 planar superconducting coils. A pulse duration of up to 30 minutes at 10 MW electron cyclotron resonance heating (ECRH) power or even more is planned with lower power.

The requirement for steady state operation strongly influences the design of the technical components, the actively cooled in-vessel components, the plasma diagnostics, heating and fuelling systems, data acquisition and device control.

Due to planned data rates of up to 30 GByte/s and a total amount of data in a range of 50 TByte per long pulse experiment enhanced concepts for real time plasma control, continuous data acquisition and data archiving had to be developed.

Manuscript received June 14, 2012.

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An important requirement for steady state control and data acquisition is to combine all measured data with a precise time stamp.

II. Structure of the Trigger- Time- Event System

The timing system is a crucial element for the Control, Data Acquisition, and Communication (CoDaC) system of the steady state fusion experiment Wendelstein 7-X (W7-X). Its main task is the synchronization of all clocks with sufficient accuracy [2]. Furthermore, it is able to send, receive, and process event messages. It offers a wide range of time related functions, e.g., time capturing, pulse generation, realization of time delays, and sending and receiving of trigger signals. The overall timing system consists of a central timing system and a considerable number of local timing systems. Most of the technical systems like heating system, power supplies, gas inlet, and all diagnostic systems include a local timing system in a so called control station.

The requirements for the response time and precision of time stamps of the local systems are very different. Short response times with data processing in real-time and a time resolution in a range of 10 ns are essential for data acquisition systems, segment processing, and fast feedback control. Most control systems for the technical components and diagnostic systems, based on Programmable Logic Controllers (PLCs), are less demanding. Because the cycle time of a PLC often exceeds 10-50 ms, time resolution and time accuracy can be much lower than for real-time computer systems. A local Trigger-Time-Event (TTE) system consists of a computer board and software components for trigger, time, and event message tasks. It is integrated in the control systems of the technical components and diagnostic systems. The time, trigger, and event-related messages are broadcast from the central TTE system to the local units through a unidirectional fiber network. Units not equipped with a local TTE board, such as PLCs or computers with low requirements for the precision of time stamps, can receive the same information through a dedicated Ethernet. Trigger signals with high requirements for the response time or reliability will be distributed with hardware trigger lines. The number of TTE connected units is flexible and not limited. However, this allows the TTE system to be built and sized depending on the requirement resulting in the architecture and corresponding data, which are generated in an experiment cycle.

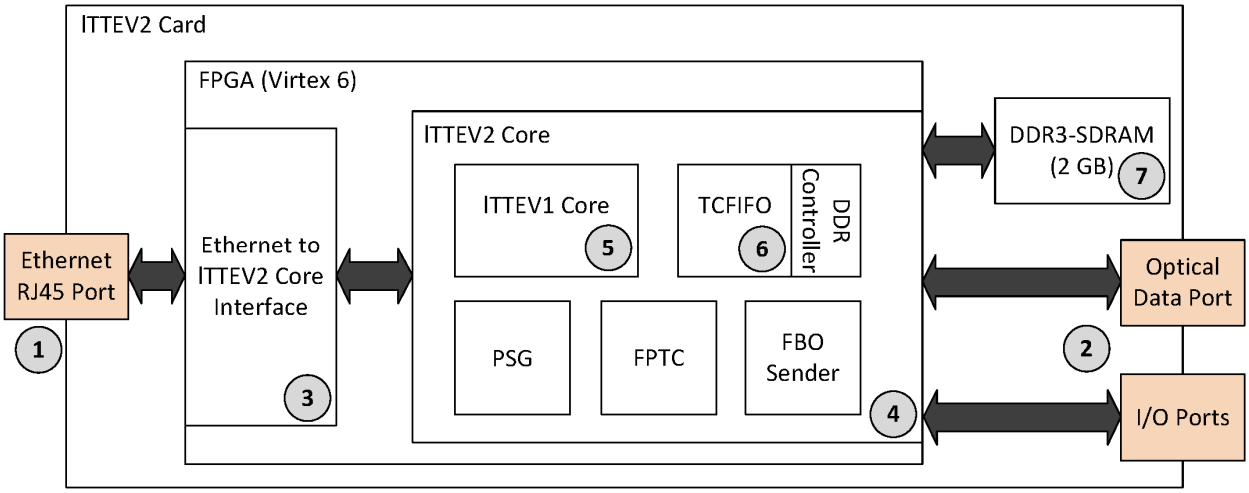

Fig. 1: System architecture of the lTTEV2 card

III. Description of the LTTEV2 Card

Until now, there exist two different types of local timing systems for control stations: the local Trigger Time Event card (lTTEV1) for control stations with real time requirements [3,4] and the local Time to Digital Converter card (TDC) for control stations used for data acquisition [5]. Both card types have a standard parallel PCI or cPCI bus interface.

A revision of the lTTEV1 and TDC cards is necessary as many components used for their fabrication are no longer available. Furthermore, the state-of-the-art bus interface is the serial PCIe bus. The need for a new bus interface with long term availability has led to the decision to use a GBit Ethernet interface. It will connect the new TTE card (lTTEV2), the successor of the lTTEV1 and TDC, with a host PC.

Additionally, DDR3 memory is integrated to allow the storage of high amount of data needed for high-resolution time capture processes. By choosing a more powerful FPGA device (Xilinx Virtex 6), it was furthermore possible to increase the time resolution by a factor of two.

The system architecture of the lTTEV2 card is depicted in **Error! Reference source not found.**. The main components are the inputs and outputs, the TTE-devices integrated in the FPGA, and external components on the lTTEV2 Card. The PCI connection of the lTTEV1 card is replaced by the new Ethernet port (1). Raw Ethernet packets are sent to the host bases to reduce communication overhead to a minimum. The connection is a full duplex Point-to-point connection which ensures a fair connection without any loss of packages due to collisions using Ethernet as the transmission protocol. The addressing is accomplished by using MAC addresses. The MAC address is not chosen statically. The Virtex 6 FPGA owns a so called Device-DNA [6]. This is an integrated eFUSE register which stores a unique 57 bit value. The eFUSE is a one-time programmable register and is nonvolatile. This DNA value will be used to generate the unique MAC address for the lTTEV2 Card. The lTTEV2 Card sends a “hello” message to the network with its own generated MAC address. If there is a collision due to compression of the 57 Bit to a corresponding 48 Bit MAC address the host will be able the change the MAC address dynamically during the operating of the lTTEV2 Card. A direct connection to a central TTE (cTTE) card, which is responsible to forward the actual time values, is realized by using an optic fibre connection (2). I/O ports (2) allow for receiving incoming serial data or signals and for outputing new values. The Ethernet to lTTEV2 Core Interface (3) handles all incoming raw Ethernet packets and converts the included data into corresponding commands, which will be accepted by the lTTEV2 Core (4). The lTTEV2 Core comprises the main TTE functionality in form of TTE-devices. The TTE-devices of the lTTV1 design are wrapped in the lTTEV1 Core (5) and can be accessed directly via the new Ethernet interface (3). The newly added TTE-device types: the Pulse Sequence Generator (PSG), the Fast Periodic Time Capture (FPTC), FBO sender and the Time Capture FIFO (TCFIFO) (6) will be described in the following section.

IV. TTE Device Overview

For the realization of the required trigger, time, and event functionality, specific device types have been defined.

The logic of all TTE devices is defined by the FPGA program. Several devices have input and output signals with a direct connection to signal ports (e.g., I/O trigger signal ports, data receiver) of the TTE card. Via these ports, W7-X field signals can be coupled with TTE device input/output signals.

Table 1 summarizes all TTE device types and their main functions. Some important devices such as the I/O device are available more than once.

An important design goal of the development of the new lTTEV2 card was the implementation of all main TTE functions into a FPGA (field programmable gate array). The integration of all TTE devices on a chip minimizes the effort for external assembly parts and minimized signal delays by signal transmissions between devices. Another advantage is the possibility to update TTE devices to new versions only by adapting the FPGA program. A hardware change is not needed.

TABLE 1: DEVICE TYPES OF THE LTTEV2 CARD

TTE device type	Number of device instances	Function
Ident Device	1	Saving of: card type, release number of FPGA program, number of devices of a all implemented device types, start addresses of TTE devices,
Time Counter Device	1	Local 64 bit time counter, synchronization with a central time counter,
FBO Data Transceiver	1	Receiving synchronization, time, and event data packets from cTTE sender, Sending of event and status data packets to the cTTE receiver,
I/O Device	16	Output and input of trigger signals
Time Capture Device	8	Time value capture by occurrence of events,
Time Capture FIFO Device	1	Time value capture by occurrence of different event sources with high event rate,
Fast Periodic Time Capture Device	2	Time value capture by occurrence of periodically events with high event rate,
Alarm Timer Device	4	Generation of alarm events by using absolute or relative alarm time values,
Delay Timer Counter Device	8	Generation of programmable delays,
Pulse Generator Device	4	Generation of programmable periodically impulses
Pulse Sequence Generator Device	1	Generation of sequences of user defined impulse patterns
Interrupt Generator Device	4	Generation of programmable periodical interrupt requests
Event Processing Device and Event Map Matrix Device	1	Processing of event data packets
Logic Device	4	Realization of free programmable logical signal functions
FSM Device and FSM RAM Device	1	Definition of a small Finite State Machine
Interrupt Device	1	Processing of interrupt requests of all TTE devices
Device Map Matrix Device lTTV2	1	Flexible signal processing by user defined coupling of the input and output signals of the TTE devices.

V. GENERIC MODEL OF A TTE DEVICE

TTE devices are functional units to carry out special time, trigger, or event processing tasks. A TTE devices type defines all device properties, signal processing functions, and the behavior. The number of implemented TTE devices of a special TTE device type is configurable during the FPGA program definition phase. All TTE devices are based on the generic device model, shown in Fig. 2. The type of a device is determined by the device transfer function, which defines the signal processing (e.g., the processing of the input signals and the generation of the output signals and values) and the device behavior. A device is equipped with a set of control and status registers and, depending on the device type, with different kinds of input and output signals.

Input signals are used for device enabling and for the starting of device functions. Output signals commit the result of the input signal processing and signalize the activity status of a device.

Input and output signals of a TTE device can be deactivated using the device control functions In_enable and Out_enable. Thus, a TTE device can be operated in different configurations regarding its hardware input and output signals.

A device is controlled either by software commands from the host-PC via network interface or by using of input control signals. The configuration of the device functions is set up using dedicated register entries.

Using a suitable setup, a device is able to generate interrupts, which can trigger software functions on host side.

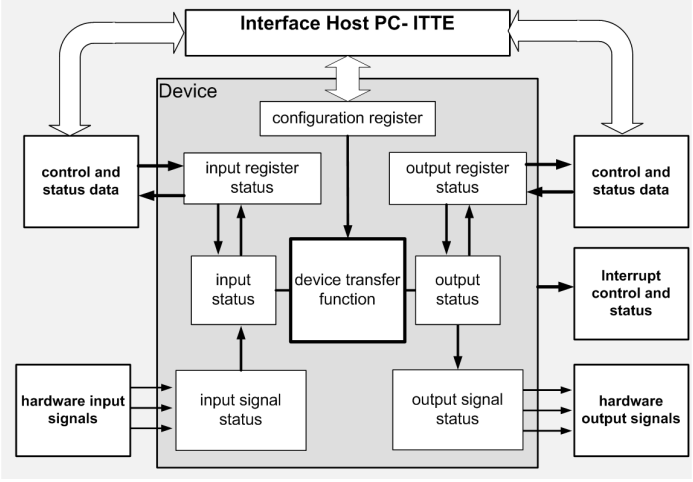

Fig. 2: System Generic model of a TTE device

The flexible combination of the signals of TTE devices allows a setup of complex signal processing in real time. Responsible for this kind of signal combination is a special TTE device called “Device Map Matrix”. By means of a control register configuration of the Device Map Matrix the required signal combination between device signals will be set. In Fig. 1 the principle of the device signal combination is shown.

Time Counter device:
The time counter device is the most important TTE device of the lTTEV2 card. The time function is based on the functions of this device. The time counter consists of a 64-bit counter and is clocked with a 100 MHz clock signal. Bit 0 of the time counter represents a time value of 1ns. The time counter works with three different time modes.

Time Mode 0:
The time counter works with a free-running local oscillator without clock and time value synchronization from the central TTE unit.

Time Mode 1:
The local oscillator is synchronized with signals from the master oscillator of the central TTE unit.

Time Mode 2:
The local oscillator and the time value are synchronized with signals from the master oscillator and time counter of the central TTE unit. If a time value error occurs, the right value will be set automatically. The error range for the time value is user-defined.

Because of the different path lengths of the optical transmission the time counter values arrive at different times in the local TTE units. In order to compensate this, the reference time for comparison with the local counter is delayed after the time of arrival by means of a variable-delay compensation unit. The resulting total delay (transmission delay and individual wait time) is the same for all TTE units and all local clocks run exactly synchronously.

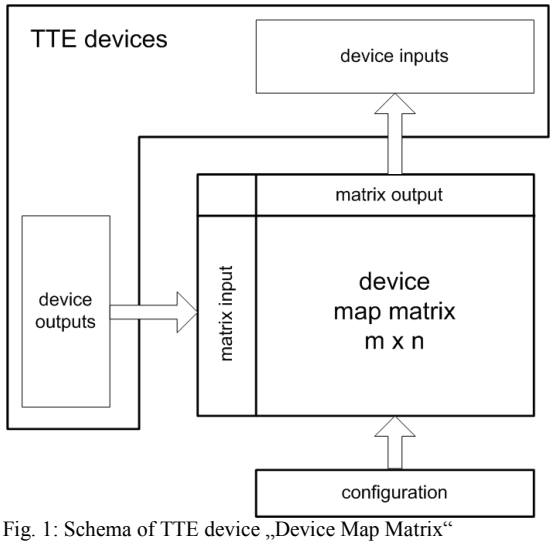

Fig. 1: Schema of TTE device „Device Map Matrix“

Time Capture FIFO (TCF) device:
The TCF device is used for time stamping of dedicated time capture events. A time capture event will be produced by an active hardware signal of one of the eight time capture start inputs or by setting of a control flag TCFStartTC 7-0 within TCF control register.

The TCF device can be used in two different operational modes: the FIFO mode or the buffer mode.

The TCF device consists of three memory blocks, whereat two blocks are located within the FPGA circuit and the third block is external.

The first internal memory block works as cache for the time capture values after a capture event has occurred. The cached time values will be transferred into the external memory in a burst mode.

The external memory is a standard DDR3 RAM with 2 GB memory capacity and allows to store about 219 million time capture values with 73 bit word length (64 bit time capture value, 8 bit trigger source, 1 bit event source).

The read out of the time capture values from the DDR3-RAM to the host via the Ethernet interface is an automatically process using the second internal FPGA memory block. The transfer processes will be controlled by the fill level of the FIFOs.

FIFO mode of the TCF device:
The DDR3-RAM is used as a FIFO memory, which will be linearly filled with time capture values. During a time capture action the 64 bit time value and an identifier for the trigger source will be stored.

The lowest fill level of the external FIFO to start the transfer process of the time capture values can be determined via a configuration register.

A flow control for this transfer process exists. An application running on the host PC can force a wait cycle, which stops the transfer for a given time. This time is also configurable.

After a stop of all time capture actions the external FIFO can be fully read out, if the command Flush_DDR_RAM is activated.

Ring Buffer mode of the TCF device:
All time capture values will be stored in a memory, which is organized as ring buffer. This ring buffer is located in the external DDR3-RAM. A trigger event or software command can stop the time capture process if the configured number of post trigger events are detected and processed. Subsequently, the readout process starts automatically. The complex device structure of the TCF device is shown in Fig. 2.

FBO sender:
The lTTEV1 card was able to receive messages via fibre. Furthermore, the lTTEV2 FBO sender enables the lTTEV2 card to send data directly to the cTTE card. A message to the cTTE card contains a static and dynamic part. The static part contains information about the status of the lTTEV2 card.
The dynamic part can be used to transmit either raw data from the host or an event number with the corresponding data.
However, the host is now able to send raw data or events to the cTTE card using the lTTEV2 card as a connection unit. The packet is encoded with differential Manchester code and a CRC16 checksum enables error detection occurring during the transmission of the packet.

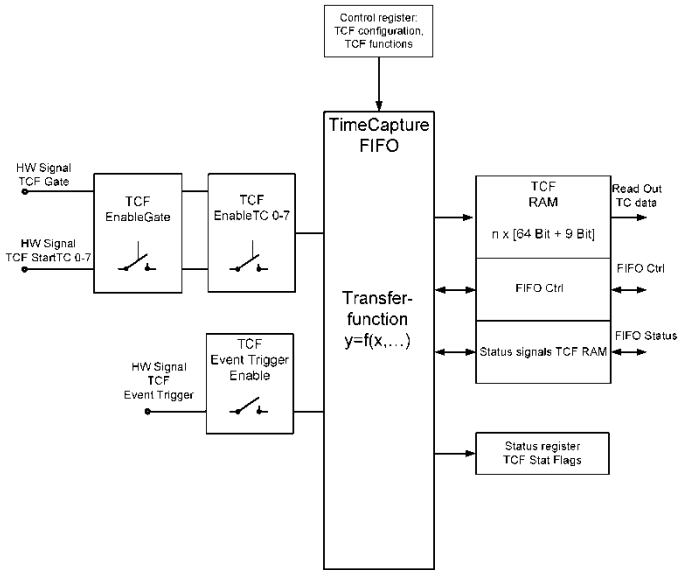

Fig. 2: Structure of the TCF device

Pulse Sequence Generator device:

A further new device of the lTTEV2 design is the Pulse Sequence Generator (PSG) device.

The PSG will be applied to generate pre-defined pulse sequences. The operational behavior of a PSG device can be finally adjusted using the PSG control register.

User defined pulse sequences are based on pulse patterns and pulse programs. It is possible to define 16 different pulse patterns. A pattern consists of a binary bit stream with a length of minimally 1 and up to 32 bit.

A pattern is described by setting a corresponding bit of the pattern definition register PSGSetPattern # n. If a bit is set to 0 then a low signal will be generated, and a high signal, if a bit is set to 1. The signal length for a low and for a high phase is defined by PSGSetImpuls #n register settings. The output length of a logical 0 and 1 can be individually set in a range of 10 ns up to 21 s.

A PSG device can handle up to 16 different impulse sequence programs. An impulse sequence program describes the sequential arrangement of the pulse generation and can consist of up to 16 sequence program sections. Every sequence program section has three configuration values for its setup. The first and the second value (program step type and identifier) define a pulse pattern or alternatively a sequence program, which has to be executed if this sequence program section is active. The third set value (repetition) configures the number of repetitions of a dedicated sequence program step.

Due to these chaining possibilities, it is possible to define infinite program loops or program calls inside a running pulse sequence program.

The start condition for a pulse sequence program can be generated by a hardware trigger signal (8 special start triggers exist for this function) or by a software command. Additionally, it is possible to switch between programs to react on incoming events.

A simple pulse program definition based on a 9 bit large pulse pattern and k repetitions is shown in Fig. 3.

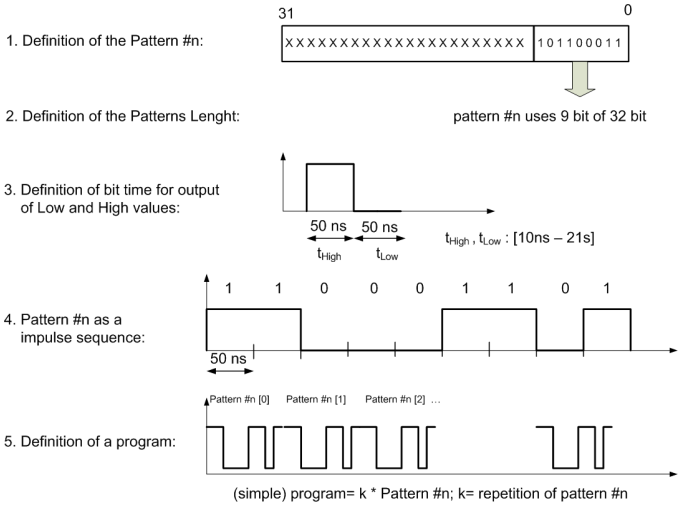

Fig. 3: Definition of a simple impulse program consisting of one pattern

Three different examples for pulse sequence program processing are shown in Fig. 4. The pulse program of the first example consists of a sequence of 16 program steps. Every program step is defined by a pulse pattern. The usage of an infinite loop depicts program example 2. The third example shows the possibility to change the pulse sequence program flow by using an event program trigger.

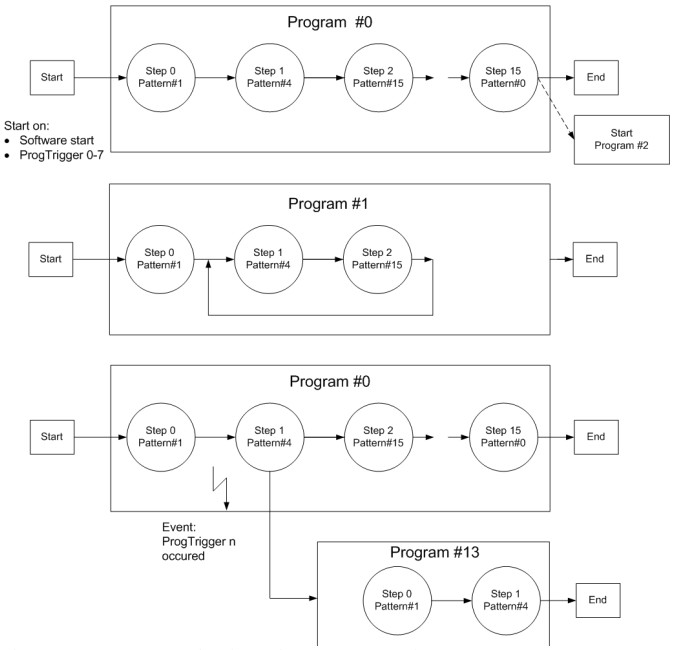

Fig. 4: Program examples for pulse sequences of a PSG

Fast Periodic Time Capture device:

The Fast Periodic Time Capture (FPTC) device allows fast capturing of incoming periodical events with a high frequency. A FPTC device produces time stamps after a predefined number of events. This allows a data reduction, e.g., for data acquisition with high sample rates.

There is a limit due to the system frequency. The FPTC can trigger signals with a maximum frequency of 50 MHz.

A monitor process watches the correct signal behavior and provides status information.

The old design without any further instances or new devices has been taken and mapped to the new Virtex 6 FPGA device to make a comparison between the old and new design. The reference FPGA is the Virtex 6 VLX240t-1FF1156 from the ML605 evaluation Xilinx board. The difference is depicted in Table 2: Resource Utilization.

TABLE 2: RESOURCE UTILIZATION

	lTTE V1	lTTE V2	Difference %
# Slice Registers	9,397	37,131	295
% Slice Registers	3	12	
# Slice LUTs	8,559	41,047	380
% Slice LUTs	5	27	
# Used IOBs	158	191	21
% Used IOBs	26	31	

The number registers are raised by the factor of nearly 4 and the number of used lookup tables (LUTs) for the logic is raised by the factor of 4.8. However, the higher utilization of the resources and the higher amount of used input/output blocks (IOBs) are due to the raised instance number of the devices and the added new devices. Furthermore, the integrated DDR3-RAM controller needs IOBs to connect with the physical memory on the board. The new functionalities have a share of about 43% of the registers and 47% of the LUTs of the final design compared to the design without the new devices. However, the new functionalities use nearly 50 % of the new required hardware resources.

VI. THE TTE TEST LOGIC GUI

During the project a GUI (graphical user interface) has been developed, which enables the user to interact directly with the lTTEV2 card. The GUI has been developed with Qt [7] and uses the pcap library [8] to ensure a secure and high performance data exchange.

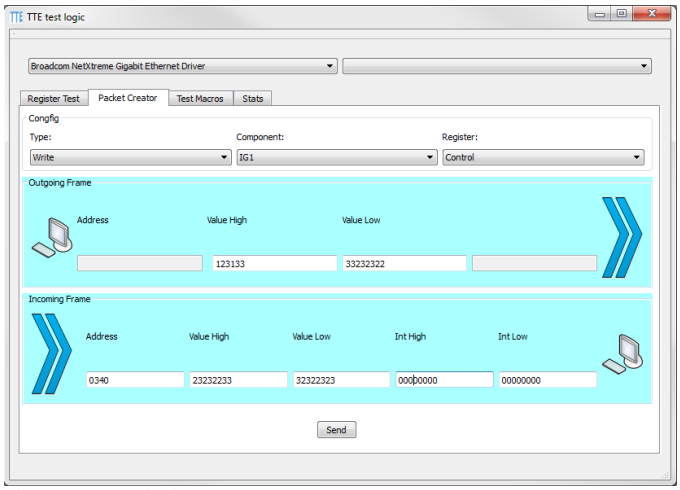

Fig. 5: TTE test logic GUI

The GUI is depicted in Fig. 5. There are four main tabs with different functionalities. The first "Register Test" tab enables a full test of all the registers storing the configurations and values of the devices. Prepared values will be send via Ethernet to the lTTE card. Each write command causes the card to send a write response packet. Furthermore, the write response packet contains the new stored value in the register. This value will be compared with a predefined desired value. The second tab enables the user to choose device registers directly. Additionally, the user can chose between read and write packets. The 64 bit values can be written directly into the corresponding fields. A read packet also induces a read response packet from the lTTEV2 card similar to the write response packet. These response packets will be directly captured by the pcap interface and the return values will be depicted in the GUI. The third tab allows the user to do different complex test scenarios. Complex test scenarios activate one or more devices which also interact with each other's. The fourth "statistics" tab holds information about the number of transmitted packets from and to the host connected to the lTTEV2 card.

VII. STATUS AND FUTURE WORK

The definition phase and the detail specification of the lTTV2 card have been finished. The working packages for programming the FPGA device should be finished by end of June 2012. The major part of the FPGA function has been tested using a Virtex evaluation board ML605 which contains all necessary interfaces and a Virtex 6 vlx240t-1FF1156 FPGA [9].

The next project steps are the development of the printed circuit board and of the 19" casing. The first prototype should be available for extensive tests by end of 2012.

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