Electrical Design Of The BUSSARD Inverter System For ASDEX Upgrade Saddle Coils

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A set of 16 in-vessel saddle coils is installed in the ASDEX Upgrade (AUG) nuclear fusion experiment for mitigation of edge localized modes (ELM) and feedback control of resistive wall modes (RWM). The coils were driven by DC current only during previous campaigns. Now, a new inverter system "BUSSARD" (German abbr. for "Bayerischer Umrichter, schnell schaltend für AUGs rasche Drehfelder", translated: "bavarian fast switching inverter for AUG's fast rotating fields") is built for the experiment. A four-phase system has been assembled to simultaneously operate up to 4 groups of coils consisting of up to 4 serial-connected coils each. The maximum current is 1.3 kA with a ripple in the range of 7 % and the frequency is variable between DC and approx. 100 Hz. The switching frequency is variable between approximately 3...10 kHz. As a first application, rotating fields are generated. The system can be enhanced in two stages to 16-phase operation with a bandwidth of 500 Hz and a 24 phase system with a bandwidth of up to 3 kHz.

Keywords: multilevel inverter, rotating fields, magnetic perturbation, pulse width modulation (PWM), Neutral Point Clamped Topology (NPC)

1 Introduction

Small non-axisymmetric perturbations of the magnetic confinement field are found to be beneficial in the ASDEX Upgrade nuclear fusion experiment in Garching/Germany, and to this end AUG is being equipped with two different sets of magnetic perturbation saddle coils – planned or already integrated into the vacuum vessel [1, 2, 3], the so called "A-coils" and "B-coils". Currently, only the B-coils are integrated.

The experimental aim is to mitigate different kind of plasma instabilities - "edge localized modes" (ELM) [4, 5] with stationary perturbation fields and "resistive wall modes" (RWM) [6] using an active feedback control mechanism [7]. At present, all coils are driven by direct current (DC), only, to generate small static deformations of the torus-shaped plasma. For full performance, it is necessary to operate each coil independently with arbitrary alternating current (AC) waveforms. Main applications are to generate rotating fields with different numbers of poles as well as fast magnetic responses to detect plasma disturbances. For full flexibility, 24 power inverters (one per coil) are needed. Alternatively, groups of coils can be connected in series by means of a "patch panel" to make use of a smaller number of inverters. The coils tolerate a current of 1 kA (full tokamak toroidal field and plasma current) or 1.3 kA (reduced toroidal field and plasma current), limited by JxB forces on the coil conductors. This current limit has to be monitored and enforced by the inverters. The bandwidth of the B-coils is 500 Hz and the bandwidth of the A-coils will be in the range of 3 kHz. Inductance and power consumption depend on frequency. They are in the range of 30...50 µH and up to 20 kW respectively for the B-coils. The main power loss is generated by eddy currents induced into the coils' housing (Inconel 600, up to 50% of total power) and by the cable's resistance. The power cable connecting each coil with its inverter differ in length from several 10 m up to 100 m. Their influence on the load impedance is not negligible. Additional passive output filter components are added.

2 Concept Overview

The Semikron power modules meet many of our demands to realize an adequate inverter system, as described in [8]. Except the switching frequency is too low for operation of the A-coils. Therefore, up to six power modules are connected to a "NPC-like" topology to power a single coil (see Fig. 1). This NPC-like topology offers the chance for phase shifted operation to increase the total switching frequency.

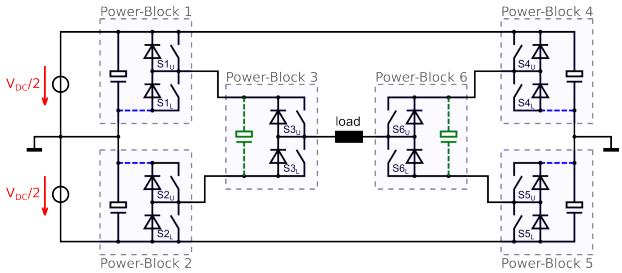

Fig. 1: NPC-like topology realized by "distributed" power blocks (see [8] for details).

The block diagram in Fig. 2 gives an overview of the final system. To operate the B-coils, a H-bridge topology would be good enough consisting of two power blocks. We chose an NPC-like half bridge consisting of three power blocks, instead. This offers the advantage to *(i)* gain experience in realizing the NPC-like topology needed for the more challenging A-coils operation and *(ii)* to realize fast grounding of the B-coils which is

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advantageous for protection of the weakly isolated electric feed through of the coils [8]. For the A-coils, the NPC-like full bridge is planned, consisting of 6 power blocks. Furthermore, as an intermediate step, it will be possible to *(iii)* connect an A-coil with two B-coil inverters for rapid realization of full bridge operation.

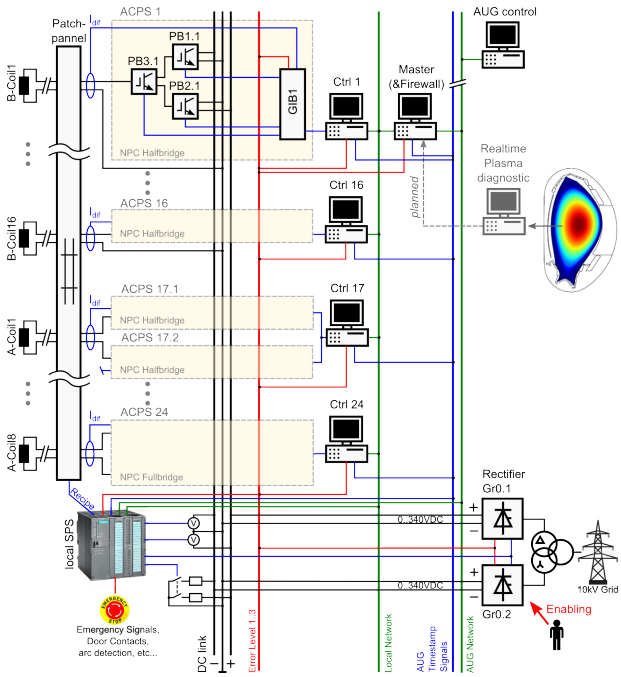


Fig. 2: Overview of BUSSARD

The fast current controllers and PWM engines are realized on flexible and robust realtime-patched LINUX-based industrial PC (iPC) systems. Since the iPC is not designed to be fail-safe by itself, special interface cards, the GIBs (gate driver interface board), were developed in-house. They make the power stage inherently safe from failed operations of the iPCs. Their main objectives are:

- PWM vector handling
- fast overcurrent detection (<10µs)
- fast differential current turn-off (I_{dif} >15A, t_{off} <10µs)
- watchdog (iPC-monitoring)
- error handling
- fade-out of switching events

The differential current probe is an in-house development, too. It detects fail-currents conducted to the vessel potential, e.g. due to a voltage breakdown of the gas-isolated electric feed-through of the coils (for details see [8]). The GIB is connected between controller and power blocks. Part of the controllers are Multi-I/O boards (MEILHAUS ME4680i) for analogue and digital signal exchange and another in-house developed interface card, the CBB (controller breakout board), for filtering and voltage separation / matching. For details about the fast current controlling see [9].

The GIBs and the controllers are bidirectionally connected with internal error lines. Error level 2 and 3 immediately lead to emergency shut-down actions of the whole system. Error level 1 signalizes warnings and suppresses the start of future operation. This is given e.g. in case of overheating the power blocks [10].

The inverters are commonly connected with two DC links (positive / negative voltage). This is advantageous for reactive power exchange, especially in the case of rotating field operation. Feeding of these DC links is realized by powerful thyristor rectifiers, primarily used for different test stands at the institute. It is connected to the 10 kV public grid and it can provide up to 2x 4 kA at 340 V. Fast current controlling and slow output voltage limitation are possible. The connection to BUSSARD has to be done via output inductors to smoothen the capacitive current. This results in a non-perfectly stiff link voltage. Voltage drops during strong load changes have to be compensated by the inverter controllers [10].

The thyristor rectifier is remote controlled by a local SPS (SIEMENS SIMATIC S7). The remote operation has to be enabled by local staff with special authorization. Additional tasks of the SPS are the monitoring and discharging of DC link voltage, the observation of different safety-relevant signals like emergency buttons, door contacts and the arc detection system, the verification of the current connections (the “recipe”) wired on the patch panel and the communication with general AUG safety signals e.g. grounding requests during opening the torus hall. The patch panel offers the option for wiring different coils or group of coils with different inverters [11].

The controllers are connected to an internal network with very limited data traffic. A master PC acts as gateway/firewall and offers the possibility for selected external access from the global AUG net into the internal controller net. The SPS is directly connected with both networks. Moreover, the master PC is a good interface for future planned higher-level controllers e.g. plasma diagnostics to respond on plasma events. In this case, the master PC receives reference values from the external controller to calculate the best inverter actions.

However, the first operations of BUSSARD are much more simple. E.g. the generation of rotating fields is realized in a different way. In this case, reference curves for each controller and values for the DC link voltage are calculated in a remote desktop PC offline. They are transferred via global network to the master PC, to the single inverters before the shot starts. After this, the local controllers and SPS receive the order to switch into “armed” mode. SPS and controllers are connected to global timing signals. They are now listening and waiting for different time stamp signals and starting their program immediately when the specific signal occurs. The whole procedure is prepared before the shot starts and no global realtime conditions have to be fulfilled. Each controller stores all the signals of its power stage (currents, voltages, gate and error states). At the end of the shot, all the inverter data are collected by a remote PC to generate the “shotfile”. The AUG shotfile is a big file including any data taken during a plasma shot.

3 The Power Stage

The main development effort was invested into the power stage although commercially available components were used as extensively as possible. Right from the beginning it was obvious that a "price" has to be paid for realizing the NPC power stage in a "distributed" way. But we were not sure, how much the "price" in terms of over voltage and additional losses can be reduced by a clever arrangement. Thus, the first step was building an adequate test bench to optimize the mechanical setup [11]. In the focus of optimization was the minimization of stray inductances between the power blocks. The areas responsible for $L_{\sigma 1}$ and $L_{\sigma 2}$ are marked in Fig. 3a. It was found out that they can not be reduced below approx. 1 µH each. This results in significant overvoltage events for the floating power blocks PB3/6. A simple calculation illustrates this: If a 1,000 A load current has to be commutated from PB1 output to PB2 output by switching PB3, the commutation time is in the range of 2.5 µs (as measured) and the total stray inductance $L_{\sigma 1} + L_{\sigma 2}$ is 2 µH. Thus, the stray voltage is calculated as

$$V_\sigma = L_\sigma \cdot \frac{di}{dt} = 2\mu H \cdot \frac{1000A}{2.5\mu s} = 800V$$

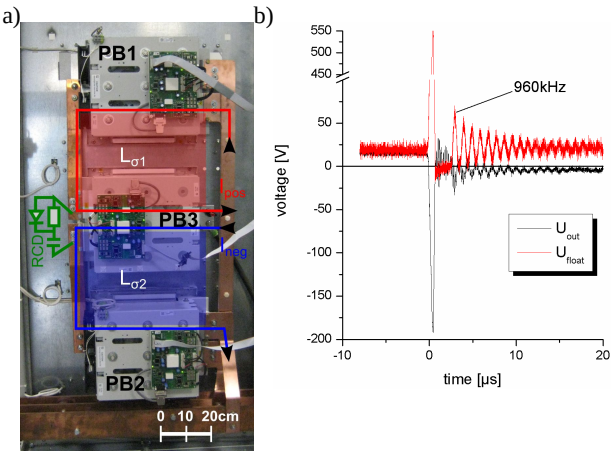


Fig. 3: (a) Photograph of the power stage mounted in a cabinet. Most critical stray inductances are marked. (b) Overvoltage event at PB3 due to stray inductances during current commutation process. U_{out} is the output voltage of PB3 which is the load voltage in half bridge operation and U_{float} is the input voltage of PB3.

The voltage strength of the power blocks is 1,200 V. With 200 V operation voltage, only, this results in 1,000 V electrical stress for the floating power blocks. The situation is tightened in reality because there is a simplification in the calculation above: The switching behaviour of a real IGBT is not smooth and linear. The current gradient during real switching events can be much higher. This results in higher stray voltage drops, as shown in Fig. 3b. Here, the power stage was operated with 30 V / 200 A, only, but the PB3 voltage was about 500 V – this is more than a factor 16! The difficult measurement was done by use of two different methods (floating probe / two single probes with fixed reference) and verified with circuit simulation tools (PSpice).

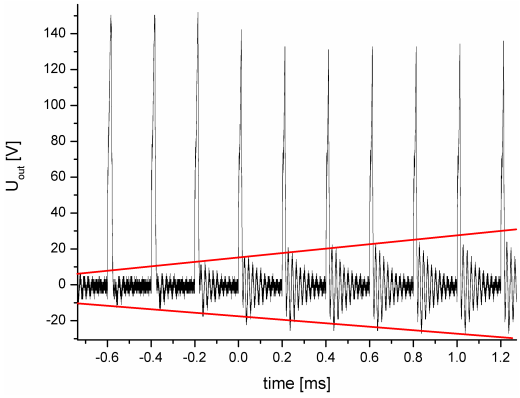


Fig. 4: Oscillating inverter output voltage due to influence of inter-powerblock stray inductances

There are two approaches to handle this challenge. *(i)* The "dirty" method is to convert the stray energy into inductive/capacitive voltage/current oscillations, oscillating between the power blocks until they are damped by conduction losses. This was done for the first tests. In Fig. 4 the NPC halfbridge output voltage for a floating PB3 capacity of 8 µF is shown. It can be seen, that the oscillating voltage amplitude is small at pulse start but it can be excited by following pulses. The risk for overvoltage of the floating power blocks PB3 and PB6 is minimized but the oscillations significantly increase losses and more importantly the electromagnetic interferences (EMI) to the environment and the driving electronics. The reliability of the overall system is significantly reduced by this behaviour. Of course, the effect doubles with increasing number of inverters operated in parallel.

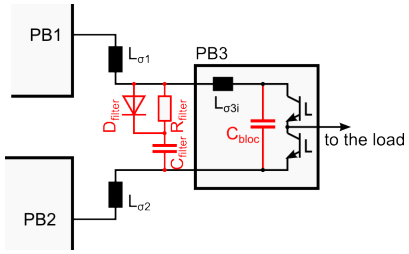


Fig. 5: 2-stage RCD filter schematic

A better approch is *(ii)* to filter the oscillations. This is challenging because the filter elements have to be low-inductive, otherwise the oscillations can be even amplified. Because it is technically impossible to realize perfect filter elements, a two-stage filter strategy was developed. The main stage is a RC or RCD circuit assembled as close as possible to the floating power block PB3/6 (see Fig. 5). The stray inductances of the filter elements have to be smaller than the stray inductances between the power blocks to have a good filter effect. The filter resistor has to be chosen in a way, that the oscillation is damped during the first period. The remaining (much smaller) inductance between filter and IGBTs of PB3/6 is compensated by very small block capacitors. Very high frequency oscillations of small amplitude are damped during few cycles because of additional loss mechanism like Skin effect and radiation.

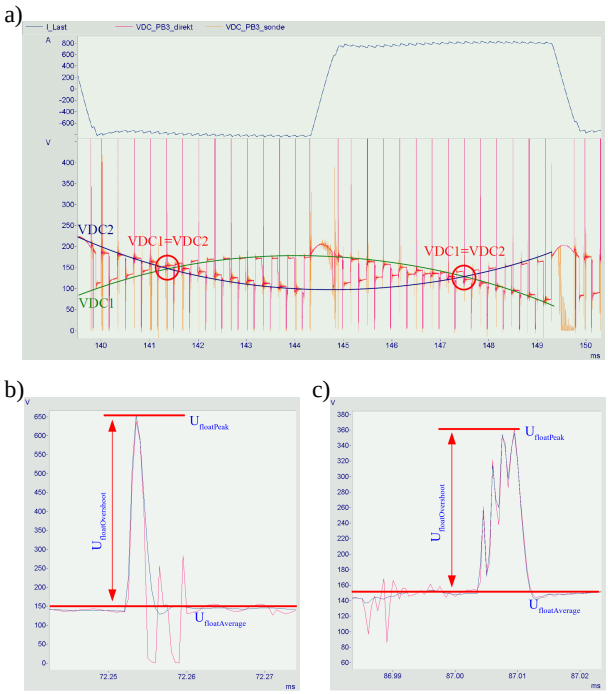


Fig. 6: Measurements of RCD filter at half bridge configuration. (a) Overview with (top) load current and (bottom) floating power block PB3 voltage. Detail of overshoot event at PB3 input voltage (b) without filter diode and (c) with filter diode. The difficult, floating measurements were done with different voltage probes (red and blue curves).

A filter resistor with a stray inductance smaller than 100 nH was found. This is 20 times better than the stray inductance between the power blocks and thus, good filter results were expected. The value of the resistor was optimized by parameter studies performed by PSPICE simulations. In Fig. 6 some measurements are shown. The filter diode improves the filter quality in terms of the first voltage overshoot after start of commutation. The "price" is a broader spectrum of overvoltage pulse, so the influence of a diode was investigated, too.

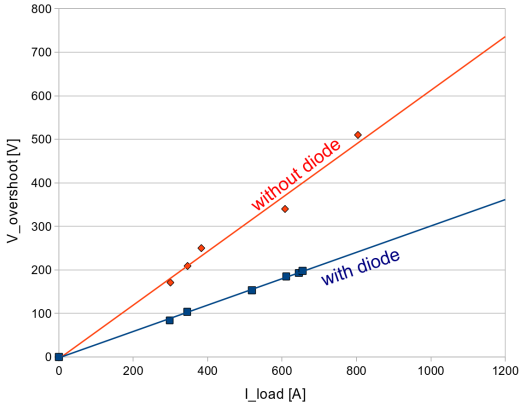


Fig. 7: Influence of RCD filter diode

In Fig. 7. The voltage overshoot is plotted against commutation load current. For 1 kA load current, the additional voltage stress for PB3 is approx. 600 V for the filter without diode and 300 V for the filter with diode. The filter losses were estimated by PSpice simulations for typical operation values. It is in the range between 1 and 2 kW for a switching frequency of 5 kHz, a load current of 1.2 kA and an operating voltage of 400 V (see Fig. 8). This conforms with temperature measurements of diode and resistor (C_{filter} = 5 µF was chosen). The "price" for realization of the NPC-like topology with distributed power blocks is now known and acceptable for the given application.

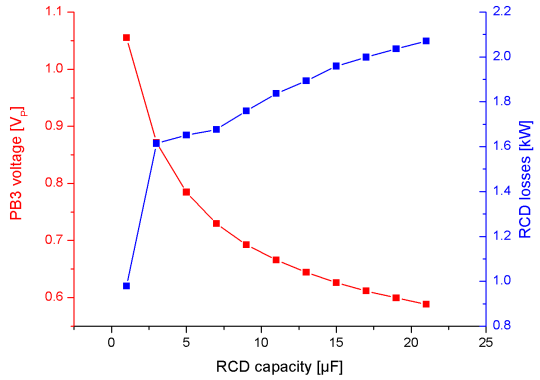


Fig. 8: RCD filter losses and peak value of overvoltage spike plotted against filter capacity

4 Cable Input Filter

The BUSSARD inverter system is situated far apart from the AUG tokamak. The cable length between inverter and coil differs between several 10 and 100 m. In addition, the cables have relative high capacity per length. The cable/coil resonance is 200 and 300 kHz. The cut-off frequency of the cable is calculated as 47 kHz for 100 m of cable. It is defined as the frequency where the cable-end voltage rises to a value of more than 20 % of the cable-input value due to reflection effects [12]. The bandwidth of the inverter output voltage is in the range of 0.5 … 1 MHz. Thus, filtering is required. This is important in particular for our case because of the weak high voltage feed-through of the coils. They are specified with about 2 kV but it was found out that the influx of high toroidal fields (up to 3 T) reduces the insulation voltage strength below 400 V [8].

The preferred filter-method is cable-input filtering (in contrast to cable-end filters) because of space restrictions. The filters require some space because there are some kW losses to cool down. It would be very difficult to place up to 24 units close to the torus. The schematic of a suitable LCR-filter ("sine filter") is shown in Fig. 9a. It can be slightly modified as shown in Fig. 9b to reject common mode contents in the voltage signal. In this case, the stray inductance of L_{filter} filters the load voltage and the main inductance the common mode content. The common mode content induces capacitive currents to the vessel, causing electromagnetic interferences with AUGs many diagnostics.

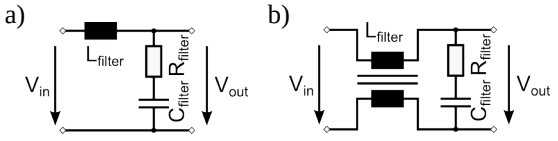


Fig. 9: Cable input filters

Unfortunately, the standard rating method is disadvantageous in our case. Typically, the filter resistor

is chosen equal to the characteristic wave impedance of the cable. It is 47 Ω in our case. To set the 3 dB filter frequency at the needed 47 kHz, a 150 µH inductance has to be installed. Due to the fact that B-coil and cable have an inductance of 40...60 µH, only, this results in a filter voltage drop of 71...79 %. Of course, this is unacceptable.

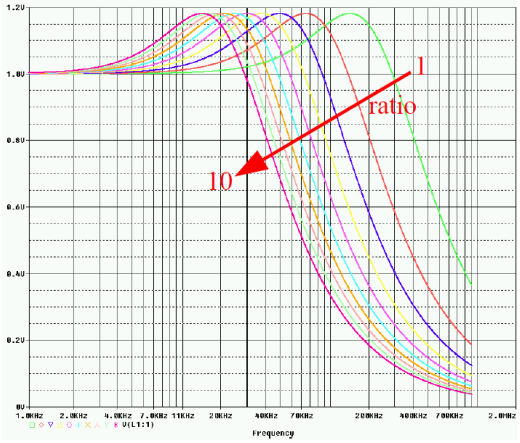


Fig. 10: Filter curves for sinus filters with L_{filter} = 20µH and reduced R_{filter} (see text)

Now the question is, why to chose the filter resistor in that way? This makes sense only for the case, the load impedance at cable end is matching the characteristic cable impedance, too. This is not the case, here. It is in the range of several 10 mΩ, instead. There are reflections at cable end and it is not possible to avoid them. So, additional reflections at cable input do not play a dominating role and the filter resistant can be modified to better fitting values. This is shown in Fig. 10. The filter resistor was reduced by a factor ratio = 1...10 and the filter capacitor increased by ratio squared. The filter inductance was fixed at 20 µH. That gave an acceptable filter voltage drop of 25...33 %.

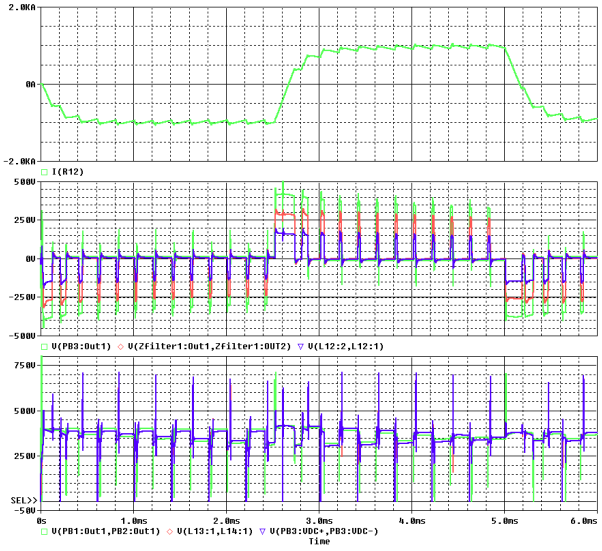


Fig. 11: Simulation results for RCD- and cable input filtering: (top) inverter output current, (middle) inverter output, cable input and cable end (=load) voltages, (bottom) floating PB3/6 voltage

The whole system was calculated in detail by the help of PSpice circuit simulation tool, including long cables (approximated by RCLG-cascades), the exact frequency behaviour of load impedance, RCD and cable input filters, stray inductances and approximated switching behaviour of the power blocks. The filter losses are in the range of 1...1.5 kW at switching frequency of 5 kHz and DC link voltage of ±200 V. RCD filter and cable input filter are complementary. In case of removing the RCD filter, the cable input filter losses increase. An example simulation result is given in Fig. 11.

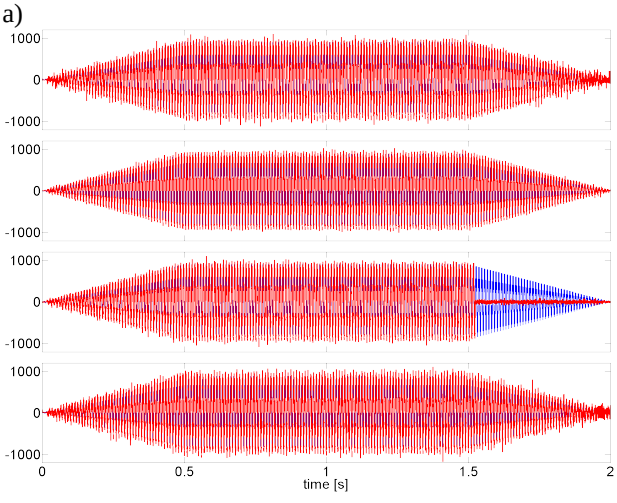
5 First Operation results

A four-phase system was tested at the end of the AUG campaign 2014. The whole infrastructure to operate the full (up to) 24-phase system had been setup. This includes the preparation of cabinet stage, the master PC, the safety systems, the connections to AUG signals, the power connections to the thyristor rectifier, the local SPS and the different power grids like e.g. battery buffered 230 V (uninterrupted power supply). The thyristor converter control had to be modified and optimized to feed capacitive loads. E.g. a soft ramp up/down had to be realized [10].

The first shots were mainly done for investigations of the electromagnetic influence on AUG's diagnostics. Groups of four coils were operated by different inverters, only one per shot (#31,394...31,399). The maximum current was 700 A and the link voltage 200 V. Switching frequency was 3.3 kHz and the coil current frequency 100 Hz. Until now, no serious interferences with the diagnostics have been found. Remote control and safety systems operated successfully.

Meanwhile, the system was improved to a level that synchronous operation of the four inverters succeeded, too. The maximum current induced into all 16 coils was 900 A at link voltage of up to ±300V. An n=2 rotating field with a frequency of 100 Hz was generated. All inverter currents and voltages as well as the cable-end voltage were monitored. Cable input filters were installed. The maximum shot length was 2 sec. Examples for the coil/inverter measurements are given in Fig. 12. Inverter No. 3 tripped after 1.5 sec due to EMI into the temperature signals. This is one of the many details remaining for improvement. Examples for the DC-link values are presented and discussed in [10].

a)



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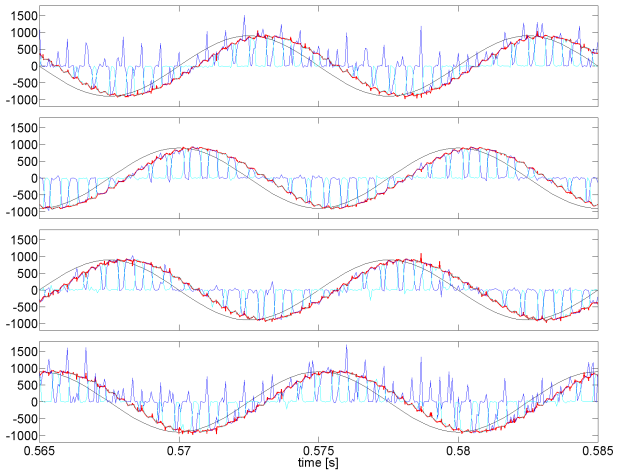
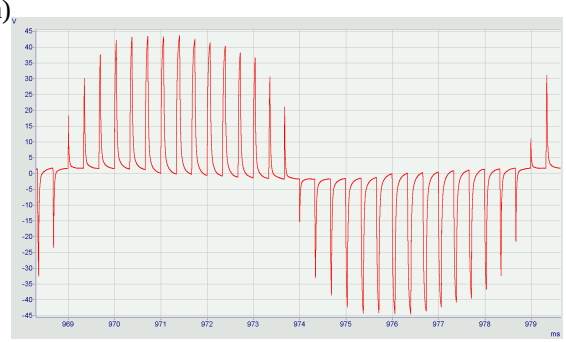


Fig. 12: 4-phase operation of BUSSARD to generate n=2 rotating fields at 900A_p coil current. (a) overview, (b) detail. red = output current, black = reference, blue/cyan = partial currents (PB1,2)

Single full-bandwidth (500 Hz) inverter operation was tested, too. The cable-end voltages were monitored and analyzed. Some results are given in Fig. 13.

a)



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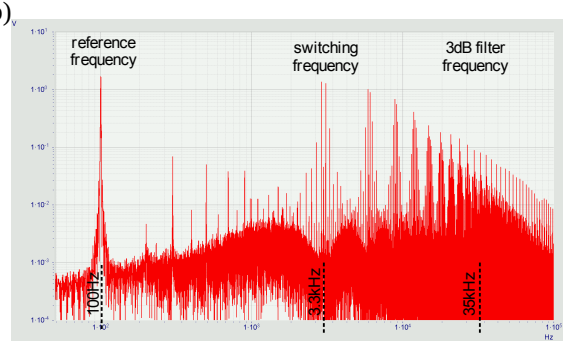

Fig. 13: Measured cable-end voltage during full-bandwidth single B-coil operation. The DC-link voltage was 100 V. (a) Time trace, (b) FFT spectrum

6 Summary and Outlook

First 4-phase operation of BUSSARD was successfully realized after 2.5 years of in-house development effort. The basic functionality of interface cards, safety systems, controller and network architecture, DC link feeding, shot setup automatization and synchronization was demonstrated and the over-all concept verified. The upgrade to 16 phases can continue. However, there is still a lot of detail work to do. The quality of controlling and signal monitoring can only be optimized if synchronous switching of all inverters is realized. This is prepared in principle but has to be assembled. There are still some EMI challenges for the interface cards left, only partially caused by asynchronous switching. The GIB firmware has to be optimized due to run-time problems. The inductive coupling of the DC link to the thyristor rectifiers has to be matched for the correct number of activated inverters, otherwise oscillations are the result [10]. For future, high-dynamic operation including external higher-level controllers, the DC link capacity could be increased. This mainly depends on intended signal quality. For very high quality, an additional fast DC-link voltage controller may be advantageous. Further experiments will be carried out to specify the requirements.

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