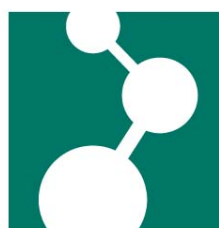

Molecular Self-Assembly in Mono- to Multilayer Organic Field-Effect Transistors

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Chapter 1

Introduction

1.1 Organic Electronics

The invention of field-effect transistors has dramatically changed our modern life by leading human society into the information era.^[1] Economic, health and national security rely on and are positively influenced by electronic technology. In the electronics industry, metal-insulator-semiconductor field-effect transistors (MISFETs) are fundamental building blocks of microprocessors, flash memories and other electronic devices,^[2-3] where silicon is the state of the art inorganic semiconductor. However, the resources and methodologies used for inorganic electronics raise urgent questions including the negative environmental impacts of manufacture, use, and the disposal of electronic devices. In comparison, a more environmentally friendly approach to manufacture in electronic industry may be to use organic materials to fabricate electronic devices. The discovery of conducting conjugated polymers in the late 1970s opened a new concept of organic electronics.^[4-5] Since then, extensive efforts have been made on this field including organic field-effect transistors (OFETs), organic photovoltaics (OPV) and organic light emitting diode (OLED).^[6] In comparison to their inorganic counterpart, organic electronics is more attractive due to its processing from solution at low temperatures significantly lowering the cost of device fabrication. Moreover, the mass density of organic materials is generally lower

than inorganic ones facilitating the production of light-weight devices. In addition, organic semiconductors offer mechanical flexibility and compatibility with plastic substrates leading to the possibility of flexible devices. Among these electronic devices based on organic materials, more attention has been paid on OFETs that can be considered as a key component of organic integrated circuits for use in flexible smart cards, low-cost radio frequency identification (RFID) tags, and organic active matrix displays.^[7]

In inorganic semiconductors, the valence and conduction bands play a dominant role in charge carrier transport, while in organic semiconductors that are mainly composed of hydrogen, carbon and oxygen, similar concepts, highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO), are also proposed. In a conjugated molecule, two types of bonds exist that are the σ -bond formed by the overlap of hybridized sp^2 orbitals and the π -bond formed by the overlap of the remaining unhybridized p_z orbitals. Electrons participating in the π -bond are called π -electrons. Bonding and antibonding states of overlapping p_z orbitals generate HOMO and LUMO energy levels in molecules with a π -conjugated system, where electrons can be transferred similarly to the transport of free electrons and holes in the conduction and valence bands in an inorganic semiconductor.^[8] Therefore, a good overlap between the π orbitals of the neighbouring molecules plays a dominant role in the electrical properties of organic semiconductors, which is closely related to the conjugation length or the presence of electron donating/withdrawing groups.^[9]

Based on different basic units, organic semiconductors can be categorized into two groups: low molecular weight materials (small molecules) including monomers and oligomers, and conjugated polymers. For conjugated small molecules, single-crystal OFETs usually exhibit excellent charge carrier transport due to the absence of grain boundaries, and hole mobilities of more than $10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ were reported.^[10-12] High-performance single-crystal OFETs with electron transport could also be fabricated by a modified drop-casting approach leading to a mobility up to $11 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[13] In comparison, OFETs with polycrystalline thin films as active layers are more practical for flexible devices. The film crystallinity of

2,7-dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C8-BTBT) was significantly enhanced during spin-coating by combination of centrifugal force and phase separation, and the hole mobility of resultant transistor reached as high as $43 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ with an average value of $25 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[14] In the case of conjugated polymers, a general strategy was proposed to mediate self-assembly of polymer chains and unidirectional alignment of thin films with the assistance of the capillary action. Processed by this method, an ultrahigh hole mobility of $36.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ was measured for poly(4-(4,4-dihexadecyl-4H-cyclopenta[1,2-b:5,4-b']dithiophen-2-yl)-alt-[1,2,5]thiadiazolo[3,4-c]pyridine) (PCDTPT) transistors.^[15] Unlike p-type polymers, n-type polymers usually show relatively low transistor performance. So far, only few n-type polymers have been reported with an electron mobility over $1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[16-18] Apart from unipolar charge carrier transport, organic semiconductors with ambipolar transport properties are also achievable by rational design and synthesis, especially donor-acceptor (D-A) copolymers. For instance, a diketopyrrolopyrrole-selenophene D-A copolymer carrying hybrid siloxane-solubilizing groups yielded ambipolar charge carrier transport with mobilities of $8.84 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for holes and $4.34 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for electrons.^[19]

Before discussing the research motivation of this thesis, it is necessary to have a basic introduction of OFETs. In section 1.2, the basic knowledge of OFETs is introduced in order to clarify the function and measurement of transistors. In section 1.3, factors that influence transistor performance are discussed from the viewpoint of molecular organization and interface engineering. At the end (section 1.4), various processing techniques for OFET fabrication, especially solution processing, are described in detail.

1.2 Physics of OFETs

1.2.1 Device Architectures

OFET devices typically require an organic semiconductor layer, an insulating dielectric layer and three electrodes (gate, source and drain). Inorganic insulators such as SiO_2 , Al_2O_3 and Si_3N_4 , and polymeric insulators such as poly(methylmethacrylate) (PMMA) and poly(4-vinylphenol) (PVP)^[20-21] are commonly used as dielectric materials. Three electrodes are usually high work function metals such as gold. Typical transistor architectures that are employed for OFETs are shown in Figure 1.1. According to the order of fabrication steps, OFET configurations are divided into bottom contact and top contact. If the source and drain electrodes are deposited before the deposition of semiconducting layer, a bottom contact device is created (Figure 1.1a). Bottom-gate bottom-contact might be the simplest device architecture for OFETs. For instance, source and drain electrodes can be prepatterned on a commercial silicon wafer with heavily doped silicon as gate electrode and SiO_2 as dielectric layer. With such configuration, the transistor fabrication can be finished by simply depositing organic semiconductor layer onto this prepared wafer. However, it has to be noted that this device architecture is sometimes not suitable for conjugated molecules that tend to form single crystals or highly crystalline films. The difference in surface properties between source/drain and dielectric can lead to different molecular organization of the organic semiconductor. It was reported that pentacene molecules preferred to “stand up” on SiO_2 surface with the molecular long axis perpendicular to the substrate plane.^[22] On the contrary, tiny grains were observed on the surface of source/drain electrodes due to strong interactions between pentacene and the metal surface.^[23] Such surface-dependent morphology, in most cases, causes significant contact problems degrading the device performance. One solution is to employ self-assembled monolayers (SAMs) to functionalize contacts, which will be discussed in more detail in section 1.3.2.

Figure 1.1b exhibits a bottom-gate top-contact (BGTC) device configuration. Compared with BGBC, in the BGTC configuration the source and drain electrodes are deposited on the top of the organic semiconductor layer. In this device architecture, the metal-semiconductor contact area is sufficiently increased resulting in lower contact resistance than BGBC. It is worth noting that access resistance exists in a BGTC device, because the charge carriers must travel from the source contact on top of the film down to the conducting channel at the semiconductor/dielectric interface, and then back to the drain electrode through the whole film.^[24] Therefore, the organic semiconductor layer should not be too thick in order to minimize the access resistance.

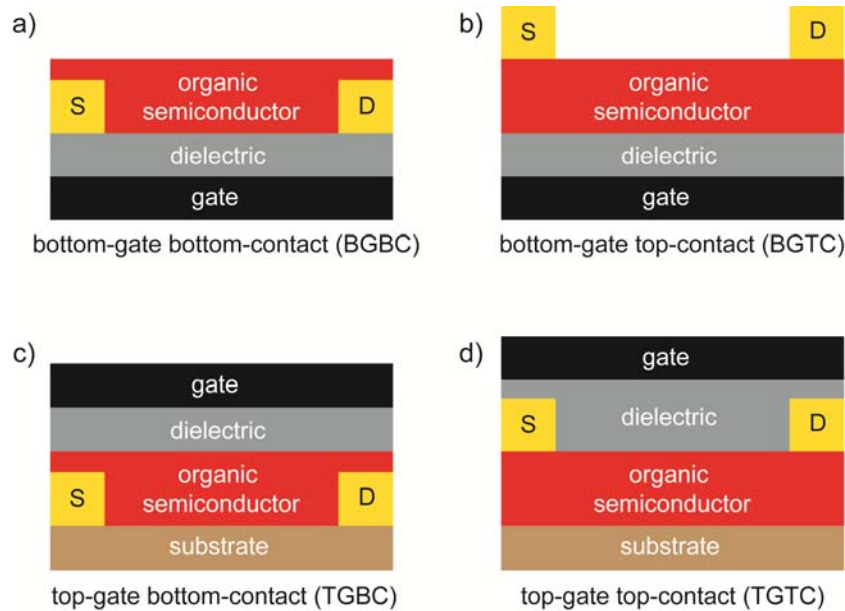


Figure 1.1 Four typical transistor architectures: a) bottom-gate bottom-contact (BGBC), b) bottom-gate top-contact (BGTC), c) top-gate bottom-contact (TGBC), d) top-gate top-contact (TGTC). “S” and “D” represent source and drain electrodes, respectively.

The deposition of the gate electrode and dielectric layer on top of the organic semiconductor layer generates top gate transistors, as shown in Figure 1.1c,d. Compared with top-gate top-contact (TGTC) architecture, top-gate bottom-contact (TGBC) devices also suffer from access resistance. One obvious advantage of

top-gate OFET device is its capability of investigating charge carrier transport at the top surface of semiconducting thin films. Poly(N,N-bis-2-octyldodecyl-naphthalene-1,4,5,8-bis-dicarboximide-2,6-diyl-alt-5,5'-2,2'-bithiophene) (P(NDI2OD-T2)) is a high performance semiconducting conjugated polymer, but high mobility could be only achieved in top-gate configuration where the conducting channel was created at the surface of the semiconducting layer.^[25] It was found that a more edge-on molecular orientation was observed at the surface of P(NDI2OD-T2) thin films facilitating charge carrier transport while a more face-on orientation was observed in the bulk of the film.^[26]

1.2.2 Working Principle of OFETs

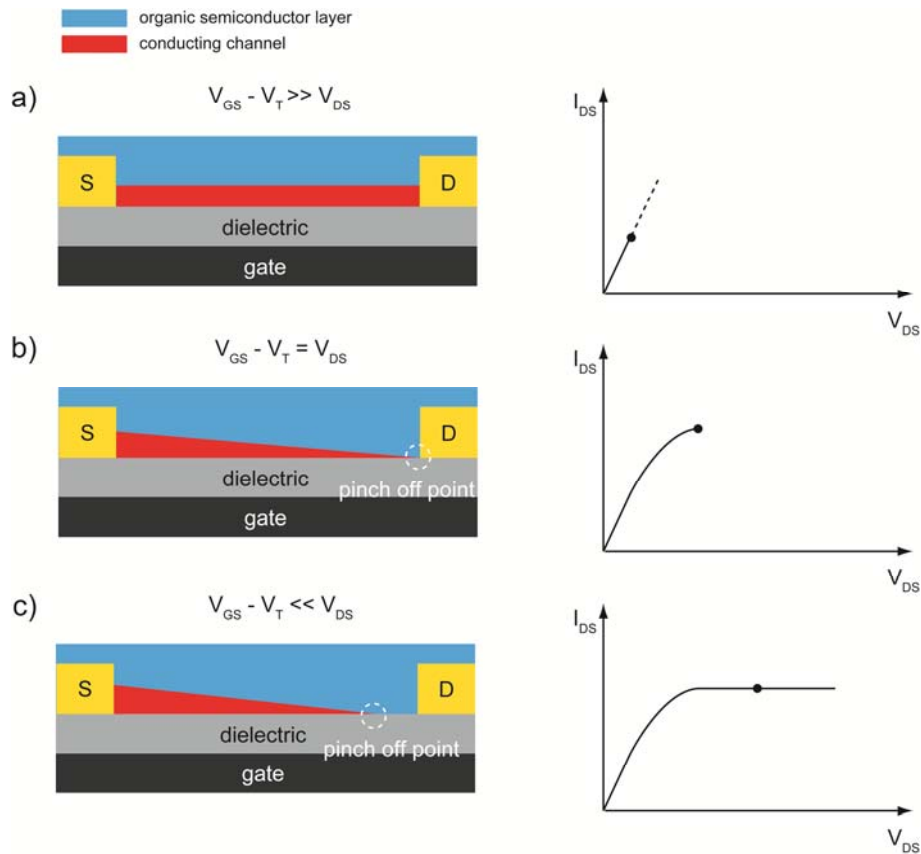


Figure 1.2 Schematic illustration of operating regimes of BGBC OFETs: a) linear regime, b) start of saturation regime at pinch off and c) saturation regime. In c), the pinch off point moves towards source electrode with increasing V_{DS} . The right figures are the corresponding current-voltage characteristics.

The working principle of OFETs is qualitatively described in this section, with BGBC configuration as an example. As described above, there are three electrodes in OFETs. To operate a transistor, voltage is usually applied to the gate electrode and the drain electrode, and the source electrode is grounded. The potential difference between the source and the gate is termed as the gate voltage (V_{GS}), and the potential difference between the source and the drain is referred as the drain voltage (V_{DS}). The effect of the gate voltage is to accumulate charge carriers at semiconductor/dielectric interface. Without the accumulation layer induced by the gate voltage, there will be theoretically no current between source and drain in spite of the drain voltage. If the gate voltage is negative, an accumulation layer filled with holes will be formed at semiconductor/dielectric interface. In contrast, a positive gate voltage will result in the formation of an accumulation layer with electrons. On the basis of this accumulation layer, a drain voltage forces accumulated charge carriers to move between source and drain creating a conducting channel.

Basically, there are two operating regimes (linear and saturation) for organic transistors, as shown in Figure 1.2.^[27] Not all accumulated charge carriers are mobile in the presence of the applied drain voltage due to the existence of trapping sites at the dielectric interface. In other words, the trapping sites at the interface have to be firstly filled by charge carriers induced by V_{GS} , and then the rest of accumulated carriers can contribute to the drain current (I_{DS}) in transistors. Therefore, the applied gate voltage, in general, has to be higher than a threshold voltage (V_T), which means that the effective gate voltage is $V_{GS} - V_T$. When $V_{DS} = 0$ V, the accumulated charge carriers uniformly distribute at the semiconductor/dielectric interface. A small drain voltage ($V_{GS} - V_T \gg V_{DS}$) results in a linear gradient of charge carrier density from source to drain electrodes, and the current flowing through the conducting channel (I_{DS}) is directly proportional to the drain voltage, as shown in Figure 1.2a. This is termed as the linear regime. When the drain voltage is increased, a pinch-off point appears close to the drain electrode at $V_{GS} - V_T = V_{DS}$, where a charge carrier depletion region is formed (Figure 1.2b). In this case, I_{DS} can still flow across this narrow depletion zone with the saturation in current value. A further increase in the drain voltage ($V_{GS} - V_T$

$\ll V_{DS}$) has no influence on the drain current anymore, but the pinch-off point moves towards the source electrode with the expansion of the depletion region.^[28] The OFET devices operated in this stage are said to be in the saturation regime (Figure 1.2c).

1.2.3 Electrical Characterizations

Most often the OFET devices are operated in the saturation regime. There are two basic types of electrical characteristics depending on V_{DS} and V_{GS} . The first measurement is called transfer characteristics in which V_{DS} is kept constant while V_{GS} is swept, as shown in Figure 1.3a. The increase in V_{GS} causes more charge carriers accumulated at the semiconductor/dielectric interface leading to a significant enhancement in I_{DS} . On the other hand, the output characteristics can be recorded by sweeping V_{DS} at various V_{GS} , where a typical linear/saturation behavior in I_{DS} is obvious (Figure 1.3b).

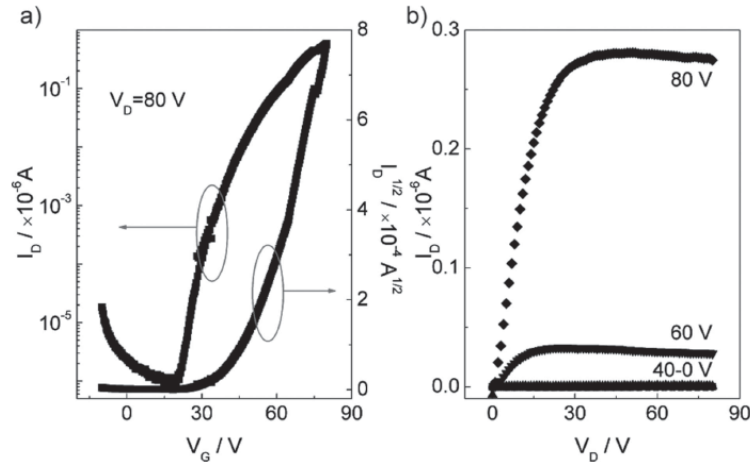


Figure 1.3 Classic transfer (a) and output (b) characteristics of OFET devices.^[29]

To quantitatively evaluate the performance of an OFET device, a few important parameters including charge carrier mobility (μ), on/off ratio (I_{on}/I_{off}) and threshold voltage (V_T) can be extracted from the electrical characteristics. The corresponding definition is described in the following sections.

1.2.3.1 Charge Carrier Mobility

As the most important parameter to characterize the OFET performance, the charge carrier mobility (μ) or simply the mobility, quantifies the drift velocity (cm/s) at which charge carriers move in the conducting channel of organic semiconductors in the presence of an applied electric field (V/cm). The unit of μ is normally $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. The charge carrier mobility can be extracted from the transfer characteristics, and the detailed procedure is discussed in chapter 9.6, where the mobility equations differ between linear and saturation regimes due to the various gate voltages.

In an ideal case, the square root of I_{DS} is supposed to increase linearly with V_{GS} in the saturation regime, however, two common issues can be encountered. The first observation is that in the saturated transfer characteristics the slope of the square root of I_{DS} versus V_{GS} increases with increasing V_{GS} . This behavior was reported for both small molecules^[29-33] and conjugated polymers^[16, 34-36]. It is assumed that the localized “low-mobility” states in the tails of the density of states have to be firstly filled, and then charge carriers are allowed to access parts of the density of states with more delocalized “high-mobility” states.^[37] Other unusual transfer characteristics are that the slope of the square root of I_{DS} is high at low V_{GS} but decreases when V_{GS} increases. Such behavior was observed in a few high-performance conjugated polymers.^[38-42] A high V_{GS} leads to an accumulation layer of charge carriers that are tightly confined at the interface.^[43-44] On the contrary, at a low V_{GS} , charge carriers have the possibility to extend further into the bulk. If the degree of disorder or the density of structural defects is lower in the bulk than at the interface, there will be charge carrier transport in three dimensions leading to a higher mobility at low V_{GS} .^[37, 45]

1.2.3.2 On/Off Ratio

As another important parameter to evaluate OFET performance, the drain current ratio between the on and off states ($I_{\text{on}}/I_{\text{off}}$) indicates the ability of a device to shut down, which plays a key role in applications of matrix active displays and logic

circuits.^[28] Typically, I_{on} is defined as the current at maximum V_{GS} , and I_{off} is defined as the current at $V_{\text{GS}} = 0$ V. It has to be noted that in the off state, no charges are accumulated at the semiconductor/dielectric interface. In other words, I_{off} represents basically the intrinsic conductivity of the semiconductor. For a high-performance OFET, the on/off ratio should be as large as possible. It is worth pointing out that some organic semiconductors can be doped by chemical impurity or oxygen and moisture. This doping behavior effectively enhances the conductivity of organic semiconductor leading to a relatively high off current. Consequently, an undesirably low on/off ratio is obtained.^[46-52] This is one possible reason why good transistor performance including high on/off ratio can be achieved by fabricating and measuring OFET devices in a glovebox under a dry nitrogen atmosphere. Additionally, a high purity of organic semiconductors can ensure a high on/off ratio to some extent.

1.2.3.3 Threshold Voltage

The threshold voltage (V_{T}) describes the minimum V_{GS} required to open the conducting channel in OFETs, that is, the transistors can be only switched on after V_{GS} beyond V_{T} .^[53-54] In an ideal case, the OFET device is operated in the accumulation regime, where no depletion layer exists to isolate the conducting channel from the dielectric. Therefore, the threshold voltage is supposed to be zero, which means the drain current should start to flow at $V_{\text{GS}} = 0$ V. However, it has to be emphasized that a threshold voltage is generally observed in most real organic transistors. This can be ascribed to the dependence of charge carrier mobility on V_{GS} .^[53] On the other hand, it is believed that both density of trapping sites at the semiconductor/dielectric interface and the quality of contacts between semiconductor and electrodes have significant influences on the value of V_{T} .^[54] In transfer characteristics with a plot of $|I_{\text{DS}}|^{1/2}$ versus V_{GS} , the threshold voltage can be estimated by determining the V_{GS} axis intercept of $|I_{\text{DS}}|^{1/2}$ in the saturation regime.^[53-54] Generally, a small value of V_{T} is desired, which represents a better device performance. A shift of the threshold voltage is commonly found when the operation of OFET device is prolonged in accumulation. To achieve

the same drain current, a higher $|V_{GS}|$ is required. This phenomenon, termed as gate bias stress,^[55-56] was reported for both n- and p-type organic semiconductors.^[57-60] A small or even negligible gate bias stress is desired for a high-performance transistor.

1.2.4 Hysteresis Effect

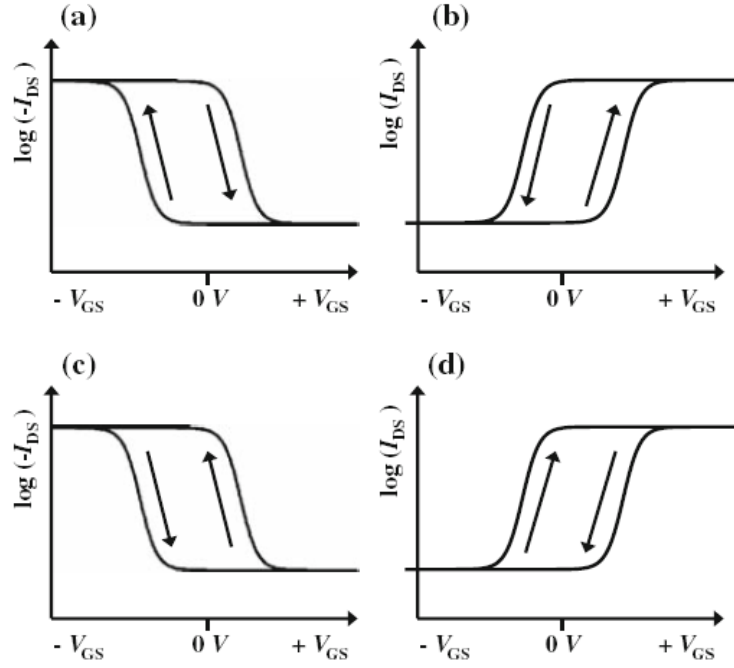


Figure 1.4 Schematic hysteresis effect of p- (a,c) and n-type (b,d) OFET devices.^[61] In a and b, the backward sweep current is higher than the forward sweep current; c and d show a lower backward sweep current hysteresis.

It is frequently observed that the transfer characteristics of organic transistors are dependent on the sweep direction of V_{GS} , as shown in Figure 1.4. This difference in I_{DS} values between forward and backward sweeps is called hysteresis effect.^[61] Figure 1.4a and b exhibit schematic transfer plots where the backward sweep current (BSC) is higher than the forward sweep current, which is defined as higher BSC hysteresis. It was reported that such hysteresis can be caused by applying ferroelectric materials such as poly(vinylidene fluoride/trifluoroethylene) (PVDF/TrFE)^[62-63] as dielectrics, because there is remanent polarization due to an externally applied electric field. Moreover, the mobile ions in the dielectric are another possible reason for higher BSC

hysteresis.^[64-65] In comparison, lower BSC hysteresis is more common, where the backward sweep current is lower than the forward sweep current (Figure 1.4c and d). There is clear evidence that charge trapping is responsible for this hysteresis. The hysteresis observed in a pentacene transistor could be sufficiently eliminated by simply annealing the device in vacuum before the deposition of semiconductor, and reappeared after exposure to moisture.^[66] In this case, moisture acted as the charge trappings. Furthermore, with SiO₂ as dielectric, it was widely proven that oxygen or moisture could trap charge carriers leading to noticeable hysteresis.^[67-69] In many conjugated systems the lower BSC hysteresis is closely related to the gate bias stress (section 1.2.3.3).^[70] Besides, a polaronic/bipolaronic mechanism was proposed as another explanation for lower BSC hysteresis in conjugated polymers.^[71-73] In the application of integrated circuits, hysteresis is an unwanted feature, but it is useful in nonvolatile memory devices.

1.3 Influencing Factors of OFET Performance

To realize high-performance OFETs, firstly, it is necessary to clarify the influencing factors that determine the transistor performance. This section mainly introduces the optimization of OFETs by the control of microstructure and molecular ordering (1.3.1) and interface engineering (1.3.2). In particular, it is emphasized in section 1.3.2 that the first few monolayers adjacent to the dielectric are responsible for the charge carrier transport in OFETs.

1.3.1 Microstructure and Molecular Ordering

Microstructure is used to describe the appearance or morphology of the material on the nm-cm length scale, while molecular ordering exhibits the periodicity of the material at a molecular level^[74]. If a semi-crystalline polymer is taken as an example, its microstructure contains ordered regions composed of large domains with

long-range periodicity, disordered regions comprised of small domains with short-range ordering of a few molecular units, and completely amorphous regions.^[74] Microstructure can be observed using a range of microscopy techniques, and molecular ordering can be determined by X-ray diffraction. Both of these two terms are closely related to the structural defects and grain boundaries having essential effects on the charge carrier transport in OFETs. There are significant differences in microstructure and molecular ordering between small molecules and conjugated polymers. Therefore, these two types of organic semiconductors are discussed separately in this section.

1.3.1.1 Small Molecules

The grain size of organic semiconductor thin films plays a dominant role in transistor performance. It is reasonable that a large grain size is far more preferable for charge carrier transport since there is a lower density of grain boundaries. This has been proven by systematic investigations on small molecules. A higher substrate temperature seems to be effective to enlarge the grain size during the film deposition of organic semiconductors. When the substrate temperature was varied from 10 to 65 °C, the grain size of pentacene thin films was significantly enlarged from 0.2 to 5 μm, resulting in an improvement of mobility from 0.05 to 0.5 cm² V⁻¹ s⁻¹.^[75] Octithiophene was reported to follow an identical trend, and a theory on the basis of Debye length was proposed for explanation.^[76] When the grain size was more than twice the Debye length, the barrier height was only dependent on the distribution of defect-related localized states in the grain boundary.^[76] On the other hand, when grain size was less than Debye length, the medium behaved as if the localized states were uniformly distributed all over the film.^[76] In brief, the energy barrier between grains was the main reason for the dependence of mobility as a function of grain size, which has been also confirmed by theoretical work.^[77]

However, it must be noted that a sparse nucleation was often induced by high substrate temperature, so that a discontinuous film was deposited because the resultant

large grains were separated far from each other. Sometimes such an effect cannot be ignored and an obvious reduction in mobility can be observed.^[78] Similar observations were also reported in tetracene transistors. If small grains are well interconnected with each other, the charge carrier transport will be more efficient than large grains in spite of more grain boundaries.^[79] In addition to charge carrier mobility, grain size was found to have a considerable influence on the threshold voltage. The threshold voltage shift, namely bias stress (section 1.2.3.3), of C₆₀ OFETs was strongly dependent on the grain size, which was mainly originated from the mechanism of charge trapping at grain boundaries.^[80]

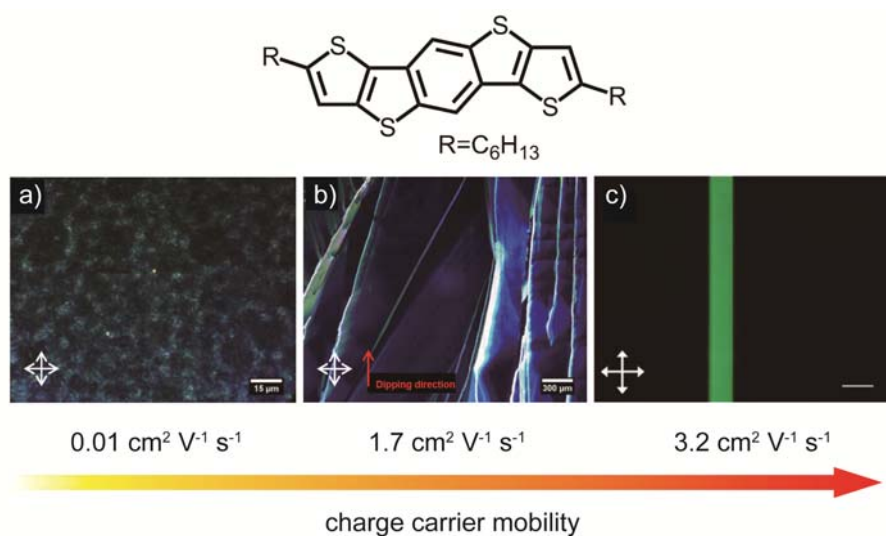


Figure 1.5 Cross-polarized optical images of DTBDT thin films with various microstructures: polycrystalline films with small (a) and large (b) domain sizes^[81], and single crystal (c)^[82]. The microstructure has a significant influence on the charge carrier transport in OFETs.

The influence of the microstructure of the semiconducting layer on charge carrier transport is more obvious for dithieno[2,3-d;2',3'-d']benzo[1,2-b;4,5-b']dithiophene (DTBDT), a five-ring-fused pentacene analog (Figure 1.5).^[81] DTBDT homogenous thin films with a high number of small crystal grains/domains were obtained by spin-coating (Figure 1.5a), but the presence of a high density of grain boundaries acting as structural defects remarkably hindered the charge carrier transport in OFETs

leading to the hole mobility of only on the order of $0.01 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[81] In comparison, dip-coating was able to significantly enlarge the crystalline domains up to the millimeter scale. According to Figure 1.5b the grain boundaries were preferentially parallel to the dip-coating direction. Since the resultant OFET device was fabricated with the working channel along the dip-coating direction, the detrimental influence of grain boundaries was minimized resulting in a much improved device performance with the mobility of $1.7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[81] Ideally, a single crystal of the organic semiconductor is favorable to charge carrier transport due to the absence of grain boundary. By optimizing the experiment parameters such as solution concentration and solvent, a DTBDT single crystal was grown (Figure 1.5c).^[82] In this case, the effect of grain boundaries was completely eliminated, and the OFET performance was further improved with the mobility of $3.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[82] It is thus demonstrated that the microstructure of the organic semiconductor films critically affects the charge carrier transport in OFETs.

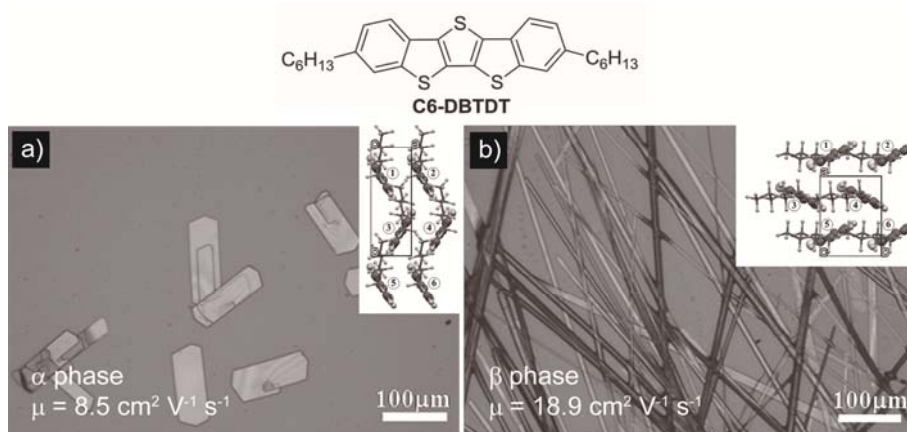


Figure 1.6 Optical images of platelet-shaped α -phase (a) and microribbon-shaped β -phase (b) C6-DBTDT crystals.^[83] The insets are the corresponding molecular packing structures. β phase depicts a much higher field-effect mobility than α phase.

Besides film microstructure, how the molecules are self-organized in the semiconducting layer (molecular orientation) is another influencing factor of OFET performance. In comparison to polycrystalline thin films, single-crystal OFETs

generally exhibit superior charge carrier transport due to the absence of grain boundaries, but they still depend on molecular orientation in single crystals. A well-known example is the mobility anisotropy of rubrene single crystals, in which the mobility measured along the a and b axes is 4.4 and 15.4 cm² V⁻¹ s⁻¹, respectively.^[12] This difference is caused by the fact that the charge carrier transport is facilitated along the direction of π - π stacking. Different types of crystal phases could be formed for a given organic semiconductor. Dihexyl-substituted dibenzo[d,d']thieno[3,2-b;4,5-b']dithiophene (C6-DBTDT, Figure 1.6)^[83] was self-assembled into single crystals with two different phases: platelet-shaped α phase and microribbon-shaped β phase. The electrical measurement for single-crystal OFETs indicated that the β phase showed more than twofold higher mobility than the α phase.^[83]

1.3.1.2 Conjugated Polymers

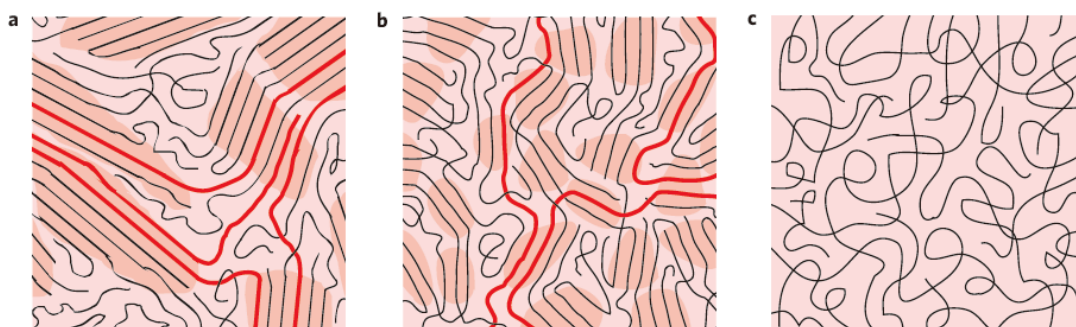


Figure 1.7 Conjugated polymer films with various molecular ordering: a) semicrystalline polymers, b) disordered aggregates and c) completely amorphous film.^[74] There is the coexistence of ordered (darker shadowed areas) and spaghetti-like amorphous regions. The red lines represent long polymer chains that can connect ordered regions.

Unlike small molecules, the chains of conjugated polymers limit their self-assembly into single crystals. Instead, thin films of conjugated polymers typically consist of both ordered and spaghetti-like amorphous regions, as shown in Figure 1.7.^[74] Semicrystalline conjugated polymers possess large domains with

three-dimensional long-range periodicity, and long polymer chains contribute to the connectivity of ordered regions (Figure 1.7a). Poly(3-hexylthiophene) (P3HT) is a well studied semicrystalline polymer. It was believed that the amorphous fraction of P3HT had a larger bandgap than the ordered region, so that there was no energetic overlap of electronic states between amorphous and ordered regions.^[74] In other words, the ordered regions played a predominant role in charge carrier transport, because charge carriers had to overcome the energy barrier between amorphous and ordered regions.^[74] It is evident from Figure 1.7b that the density of the energy barrier is significantly increased when the length of periodicity (crystallite) is shortened. In this case, a lower transistor performance was often observed. In contrast, amorphous polymers adopt a highly disordered microstructure, which means there are extremely weak or even no π - π stacking interactions. Their polymer chains were enough to create sufficient pathways for charge carriers, and reasonable field-effect mobilities ranging from 10^{-3} to 10^{-2} $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ were achieved.^[20, 84]

The importance of molecular weight for conjugated polymers has attracted extensive attentions, and polymers with higher molecular weight are revealed to have greater potential in high-mobility OFET devices.^[85-91] For instance, a 10-fold improvement in hole transport for a cyclopentadithiophene-benzothiadiazole copolymer (CDT-BTZ) was observed when increasing molecular weight from 11 to 35 kg mol^{-1} yielding a maximum mobility of $3.3 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$.^[34] One proposed explanation is related to the polymer ordering. It was found that the film microstructure was independent of the molecular weight, but the intermolecular π - π stacking interactions and molecular ordering were significantly improved by higher molecular weight as evident from XRD data.^[34] On the other hand, the interlayer distance between backbones decreases from 2.78 nm for 11 kg mol^{-1} to 2.56 nm for 35 kg mol^{-1} . A high order and tighter packing favor the charge carrier transport leading to a maximum value of $3.3 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ for 35 kg mol^{-1} polymer.

Depending on the compound's chemical structure and substrate surface property, conjugated polymers are usually self-organized in two fashions, as shown in Figure 1.8.^[92] The first type of molecular orientation is termed as in-plane, or edge-on

arrangement, where the polymer backbone is oriented normal to the substrate (Figure 1.8a). More importantly, this molecular orientation is favorable for charge carrier transport in OFETs, because the directions of π - π stacking and working channel are both in-plane. On the contrary, when polymers are self-assembled parallel to the substrate, a molecular orientation in an out-of-plane, or face-on way is formed (Figure 1.8b). It was reported that such orientation is only indirectly related to the charge carrier transport in OFETs.^[93] The interaction between polymer and substrate is the key issue to determine the molecular orientation in thin films. Furthermore, a rational design of side chains for conjugated polymers was effective to enable the transition of molecular orientation from face- to edge-on, so that the charge carrier mobility was dramatically increased by one or two orders of magnitude.^[94-95]

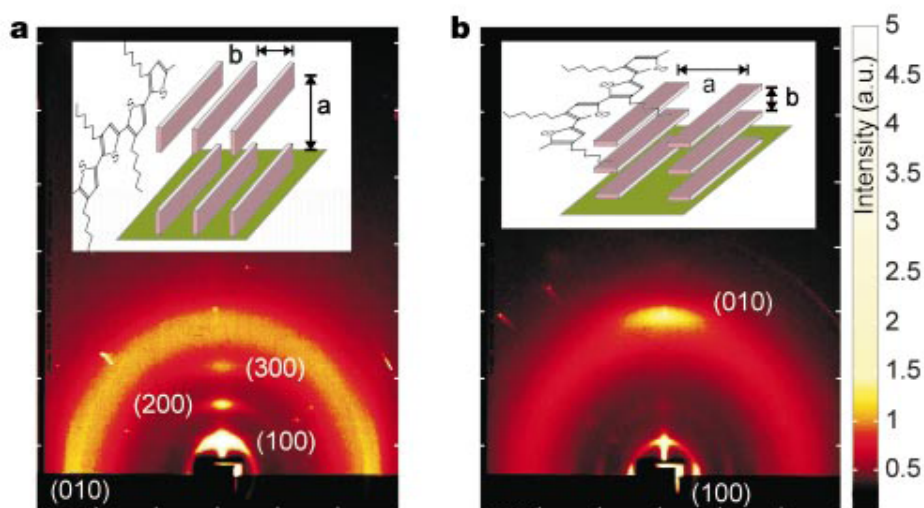


Figure 1.8 Grazing incidence wide angle x-ray scattering (GIWAXS) patterns of ordered P3HT lamellar domains with different molecular orientations.^[92] a) The polymer backbone is normal to the substrate, which is called in-plane, or edge-on arrangement. b) The polymer backbone is parallel to the substrate, which is called out-of-plane, or face-on arrangement.

In brief, the microstructure and molecular ordering of organic semiconductors including both small molecules and conjugated polymers have essential effects on the device performance of corresponding OFETs. It has to be noted that the control of self-assembly of organic semiconductors can be achieved through proper fabrication

approaches. In section 1.4, the state of the art of processing techniques for OFETs will be described.

1.3.2 Interfaces in OFETs

Interfacial engineering offers novel ways to improve the device performance of OFETs. The interface between semiconductor and dielectric plays a predominant role in charge carrier transport, while the interface between semiconductor and electrode has a key influence on the injection of charge carriers.^[96]

1.3.2.1 Interface between Semiconductor and Dielectric

As described in the section of working principle of OFETs (1.2.2), the charge carriers are accumulated at the interface between semiconducting layer and dielectric layer in the presence of gate voltage, where the conducting channel is created. Therefore, the property of dielectrics critically affects the charge carrier transport in OFETs. Insulating polymers are attractive materials for dielectric layer in transistors due to their solution processability.^[21] Homogeneous polymer thin films can be easily fabricated by spin-coating or printing at room temperature and under ambient condition. There are numerous polymeric dielectric options that possess different chemical and physical properties. Moreover, the availability of chemical modification is another advantage of polymers as dielectrics. Common polymeric insulators used in OFETs include PMMA, PVP, polystyrene (PS), polyvinylalcohol (PVA), polyvinylchloride (PVC), polyvinylidenefluoride (PVDF) and so on.^[97-101] Polymers with low permittivities were suggested as the dielectric layer in OFET devices, because high- k dielectrics could enhance carrier localization to the random dipole fields present at the interface.^[84] However, the opposite trend was also reported.^[100]

As another main type of dielectric materials, inorganic oxides, especially silicon dioxide (SiO_2), are usually treated with SAMs that are ordered molecular assemblies spontaneously adsorbed onto the surface. Such surface treatment appears to be

effective to reduce the density of trapping sites induced by the hydroxyl groups at the dielectric surface, and then efficiently improves the transistor performance.^[102] In the case of SiO₂ surfaces, in situ formation of siloxanes is the driving force for self-assembly, where the precursor silane is connected to the surface silanol (-Si-OH) groups via very strong Si-O-Si bonds.^[102-103] It is believed that the underlying siloxane network and interchain interaction, as well as reaction temperature, determine the packing and ordering of the chemisorbed organosilanes.^[104] Usually the precursor molecular species were dissolved in common solvents for dielectric modification. Also, a few silanes with short chain length such as hexamethyldisilazane (HMDS) can be deposited on the hydroxylated surfaces from the vapor phase.^[105-106] When poly(9,9'-dioctylfluorene-co-benzothiadiazole) (F8BT) was deposited on the surface of untreated SiO₂, a striking effect of interfacial trapping was observed, as shown in Figure 1.9a.^[60] By SAM modification on SiO₂ surface, the surface hydroxyl groups were remarkably passivated, and the charge carrier transport in F8BT transistors was significantly improved.^[60] Furthermore, the improvement of device performance was also dependent on the chain length of SAM molecules.^[60]

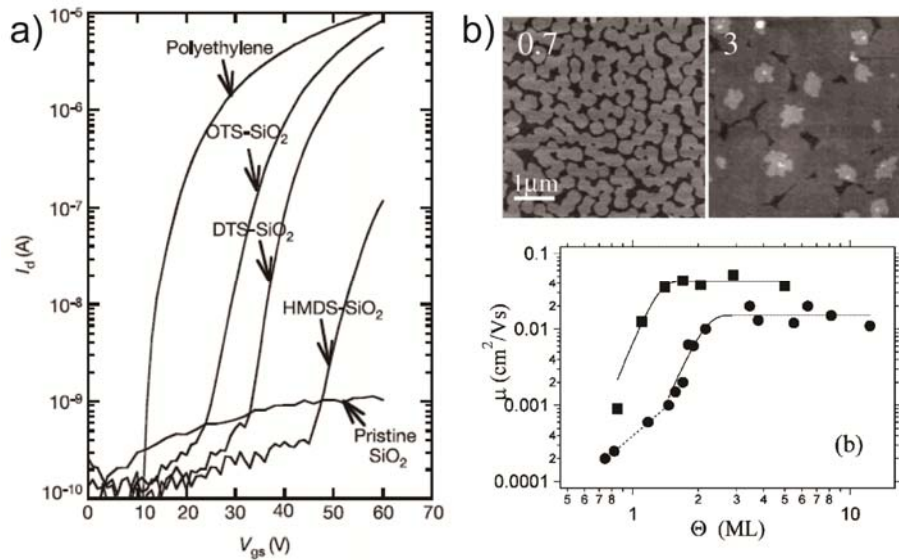


Figure 1.9 a) Transfer characteristics of F8BT OFETs with various siloxane SAMs on SiO₂ as dielectric, or with polyethylene as buffer dielectric.^[60] b) Top: AFM images of sexithienyl films with the thickness of 0.7 and 3 monolayers; Bottom: Dependence of charge carrier mobility on the monolayer thickness.^[107]

It must be emphasized that the first few monolayers close to the dielectric are of eminent importance because they are mainly responsible for the charge carrier transport in OFET devices.^[107] Hole mobility of sexithienyl OFETs was investigated as a function of the film coverage, as shown in Figure 1.9b. It was evident that the charge carrier mobility was rapidly enhanced with increasing the coverage of semiconducting layer, but was saturated when the coverage reached around two monolayers (bottom atomic force microscope (AFM) image in Figure 1.9b).^[107] A similar investigation was performed for α,ω -dihexylsexithiophene (α,ω -DH6T) by employing in situ OFET measurements during deposition.^[108] The first monolayer provided efficient percolation pathways for charge carriers, while the contribution of additional layers was negligible.^[108] A mobility saturation was observed in both cases of pentacene^[109] and DTBDT^[110-111] when 5-6 monolayers were deposited on the gate dielectric (SiO₂). On the other hand, much effort has been dedicated to organic transistors based on a single molecular layer that appears to be an ideal platform to explore the fundamental mechanism of charge carrier transport in OFETs. The monolayer transistors of oligothiophene and their derivatives exhibited moderate device performance with mobilities on the order of $10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[108, 112] In particular, a monolayer of 1,4-bis((5'-hexyl-2,2'-bithiophen-5-yl)ethynyl)benzene was grown as two-dimensional single crystal by drop-casting, and an excellent charge carrier transport was reported with a mobility of up to $1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[113] A self-assembled monolayer field-effect transistor (SAMFET) is an efficient bottom-up technology to downscale organic semiconductor into monolayer channels.^[114-115] Typically, the organic semiconductors used in SAMFETs are molecules consisting of a π -conjugated semiconducting core that is chemically modified with an anchoring group capable of covalently binding to the dielectric surface (usually oxides). Semiconductor molecules are densely packed perpendicular to the dielectric facilitating the charge carrier transport with the mobility of $0.01\text{-}0.04 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[116-119] Nevertheless, in comparison to their small molecule counterparts, it is still a great challenge to fabricate high-mobility monolayer transistors on the basis of conjugated polymers. In spite of considerable efforts on polymer monolayer

transistors, only a relatively low field-effect mobility could be obtained ($< 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$),^[120-125] even for a monolayer with well-defined microstructures ($1\text{-}6 \times 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$).^[126-127]

1.3.2.2 Interface between Semiconductor and Electrode

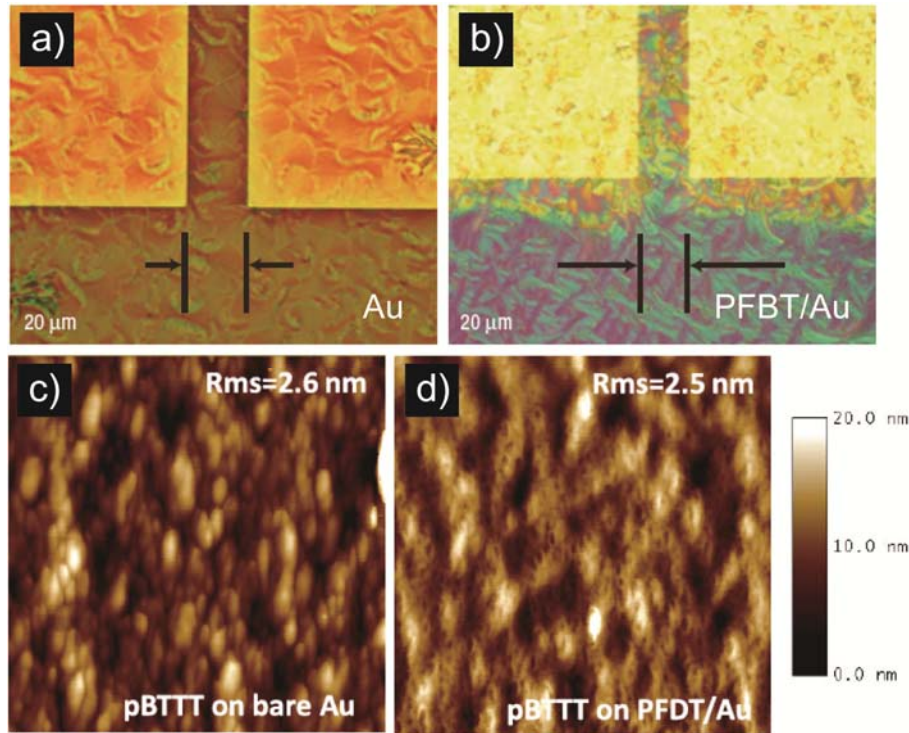


Figure 1.10 a-b) Optical images of diF-TESADT films without and with Au modification by PFBT SAMs.^[128] c-d) AFM images of PBTtT films on top of bare Au and PFDT/Au surfaces.^[129] The image size is $2 \times 2 \mu\text{m}^2$.

The interface between organic semiconductor and electrode also has a key influence on the film microstructure and the subsequent device performance, especially for bottom-contact OFETs.^[96, 130] In bottom-contact transistors, the source/drain electrodes and dielectric usually present different surface properties, so that inhomogeneities appear at the edge of electrodes leading to large contact resistance. The surface functionalization of metal electrodes by thiol-based SAMs is one of the most efficient ways to improve such semiconductor/electrode interface. Pentafluorobenzenethiol (PFBT) is often used to modify Au electrodes. PFBT/Au

electrodes induced the nucleation of fluorinated 5,11-bis(triethylsilylethynyl) anthradithiophene (diF-TESADT) in the plane of the film with the formation of plate-like crystals, as shown in Figure 1.10a,b.^[128] Such contact-induced crystallization could be originated from the interaction between the sulfur atoms in the thiophene rings of diF-TESADT and the PFBT-treated Au rather than the surface energy of the SAMs.^[128] A further study demonstrated that PFBT SAM modification on Au electrodes induced the growth of <001> textured domains that facilitate the charge carrier transport.^[131] This SAM modification of metal electrodes is also applicable to conjugated polymer based OFETs. The transistor performance of poly(2,5-bis(3-alkylthiophen-2-yl) thieno[3,2-b]thiophene) (PBTTT) was dramatically improved with the mobility from 0.08 to 0.44 cm² V⁻¹ s⁻¹ by using Au modification with 1H, 1H, 2H, 2H-perfluorodecanethiol (PFDT) SAMs (Figure 1.10c,d).^[129] The function of PFDT SAM modification can be described in two aspects. Firstly, the electrode modification caused a lower barrier for hole injection by dipole alignment.^[129] Secondly, it induced the growth of PBTTT film with higher crystallinity in the formation of lamellar morphology.^[129]

1.4 Processing Techniques

As indicated in section 1.3.1, the microstructure and molecular ordering of organic semiconductors have a significant influence on the charge carrier transport in OFETs. Although the microstructure of semiconducting layers largely depends on the intrinsic properties of the conjugated molecules, a proper processing approach allows the fine control of the self-assembly of organic semiconductors. In this section, the five most commonly used processing techniques, including vacuum sublimation and four typical solution processing methods, are introduced, and several other techniques such as printing technique are also mentioned in the end.

1.4.1 Vacuum Sublimation

Vacuum sublimation, or thermal deposition under vacuum is a wide-spread method for the fabrication of the active thin layer for OFET devices, especially for conjugated small molecules. During this process, the organic semiconductor is sublimed in a chamber under high or ultrahigh vacuum with the pressure ranging from 10^{-8} to 10^{-6} Torr.^[132] The application of high vacuum can 1) avoid the potential reaction between semiconductor and oxygen or other gases; 2) lower the pressure in the chamber so that the evaporation of semiconductors with very low vapor pressure is achievable. The semiconductors have to remain stable at the sublimation point.^[133]

Three growth modes can be observed during vacuum sublimation.^[134-137] The first mode is the so called Frank-van der Merwe or layer-by-layer growth, in which one monolayer is completely covered before the adsorption of the next layer. The second one is a three-dimensional growth, termed as island or Vollmer-Weber mode, where new molecular layers are formed before the completion of the underlying layers. The third growth mode, Stranski Krastanov growth, combines the layer-by-layer and island modes. Besides their intrinsic properties, the microstructure of organic semiconductors can also be tuned by the deposition parameters during sublimation. The deposition rate has a key impact on the microstructure of deposited thin films. A slow deposition rate provides more time for molecular self-assembly on the substrate allowing a growth of large grains.^[138] In contrast, a high deposition rate usually leads to smaller grain size due to high nucleation density, however, the film connectivity and coverage during the early stages of growth can be strongly improved.^[79] On the other hand, the substrate properties including surface energy and temperature also influence the microstructure of deposited semiconductor thin films by changing kinetics of nucleation.^[75, 139] Additionally, the growth of thin films is also dependent on the atmosphere in the chamber.^[140] There are few exceptions for vacuum sublimation. For example, single-crystal OFETs with electron mobility of $3.5\text{-}8.6\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ were obtained by sublimation in air.^[141]

1.4.2 Solution Processing

Vacuum sublimation possesses obvious drawbacks such as high manufacturing costs and low utilization rate of the semiconductors limiting its application in industry. In comparison, solution processing is attracting increasing attention because of its potential in low-cost mass production of flexible large-area organic electronic devices.^[142] Typical solution processing includes drop-casting, spin-coating, dip-coating and zone-casting.

1.4.2.1 Drop-Casting

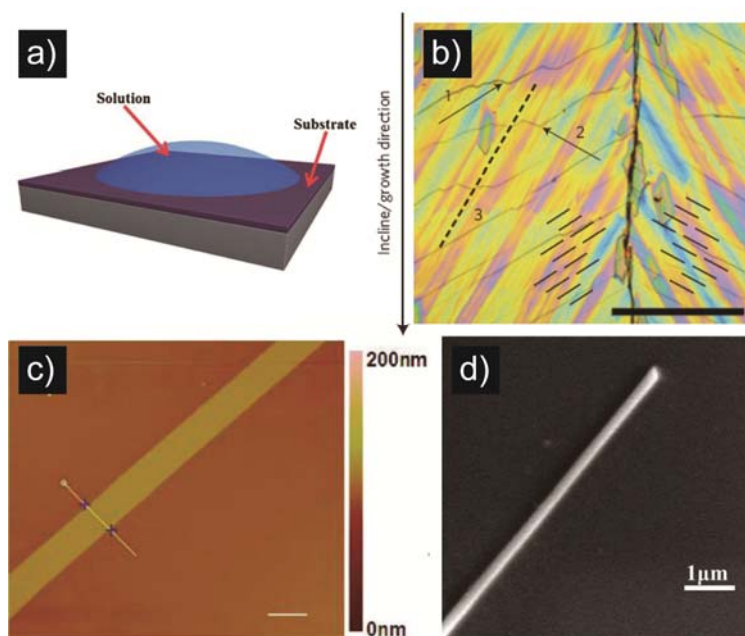


Figure 1.11 a) Schematic illustration of drop-casting,^[143] b) Optical image of N,N'-bis(n-ctyl)-x:y,dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI₈-CN₂) film aligned by drop-casting on a titled substrate;^[144] c) AFM image of DTBDT microribbons fabricated by SVD;^[82] d) Scanning electron microscope (SEM) image of CDT-BTZ polymer fiber deposited by SVD.^[145]

As the simplest method among solution processing, drop-casting only requires to drop the organic semiconductor solution onto the substrate surface (Figure 1.11a).^[143]

After the solvent evaporation, thin films are formed on the substrate. However, this method suffers from dewetting and coffee ring effects that are detrimental for the formation of long-range ordered thin films. During drop-casting, the film growth of elongated, oriented crystalline domains was observed by using a tilted substrate (Figure 1.11b), but the resultant thin film was still inhomogeneous in the tilted direction.^[144] One significant improvement of drop-casting is the application of a solvent atmosphere during processing, which is termed as solvent vapor diffusion (SVD).^[82, 145-146] By fine control of the evaporation rate of the solution, the SVD method can not only minimize the dewetting effects inducing the growth of homogenous thin film, but also adapt the intermolecular interactions leading to the formation of well-ordered microstructures. Figure 1.11 c and d show the defined crystal microribbons^[82] and polymer fibers^[145] deposited by the SVD method, and resultant transistors reached the field-effect mobilities over $3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.

1.4.2.2 Spin-Coating

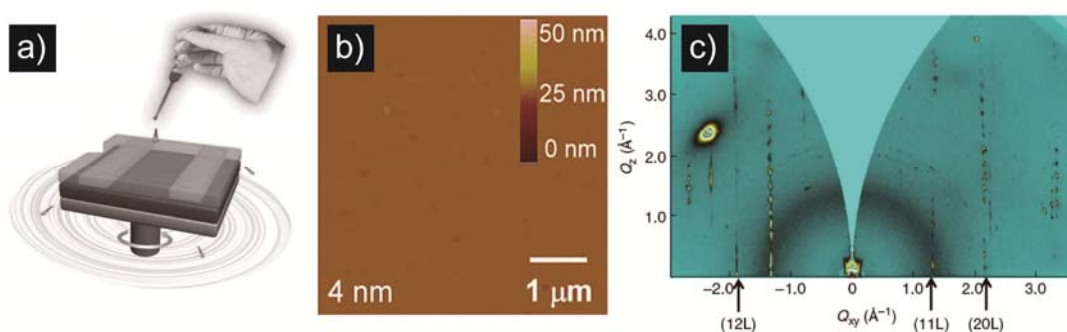


Figure 1.12 a) Schematic illustration of spin-coating,^[147] b) AFM image of spin-coated thin film of a naphthalene diimide,^[147] c) GIWAXS pattern of highly aligned C8-BTBT film deposited by a simple off-center spin-coating.^[14]

Spin-coating is another simple but versatile processing technique, as presented in Figure 1.12a. Similar to drop-casting, spin-coating also involves dropping the organic semiconductor solution onto a substrate. Subsequently, the substrate is rotated at a high speed, and the solution spreads over the whole surface. Accompanied with the

solvent evaporation, a homogeneous thin film is obtained. A solvent with a relatively lower boiling point is required for spin-coating to ensure the quick evaporation during the rapid spinning process (usually a few minutes). Typically, it is difficult to fabricate continuous ultrathin films with the thickness less than 10 nm, especially on hydrophobic surfaces. To solve this problem, the solution can be dispensed when the spin-coater motor is already operating at high speed, which is called on-the-fly-dispensing spin-coating.^[147] A homogeneous thin film with a thickness of only 4 nm can be prepared (Figure 1.12b). Because of the fast processing, the fine control of molecular self-assembly is not possible during spin-coating. An off-centre spin-coating method combined the centrifugal force with the vertical phase separation between organic semiconductor and polymer dielectric, so that highly aligned thin films with high crystallinity were fabricated (Figure 1.12c).^[14] Astonishingly, a mobility of up to $43 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ was reached.^[14]

1.4.2.3 Dip-Coating

In comparison to drop-casting and spin-coating, dip-coating is more powerful because of its capability to align the organic semiconductors from solutions (Figure 1.13a).^[148] The microstructure of dip-coated thin films can be optimized by utilizing proper solvents and dip-coating speeds. Organic conjugated molecules such as 6,13-bis(triisopropyl-silylethynyl) pentacene (TIPS-pentacene) and 5,11-bis(triethylsilylethynyl) anthradithiophene (FTES-ADT) were dip-coated into ultrathin microstripes with a high degree of alignment and few grain boundaries leading to superior FET performance.^[149] The film thickness of dip-coated thin films can be controlled in a monolayer precision (Figure 1.13b), and the morphology of dip-coated monolayer with well-defined microstructures is shown in Figure 1.13c.^[111, 150] Furthermore, this precise control over film thickness allows the inspection of the evolution of microstructure and device performance. In the case of dip-coated PBTTT thin films, the first monolayer was essentially important for the bulk microstructure evolution, where a critical multilayer network was grown creating necessary

percolation pathways for charge carriers in polymer OFETs (Figure 1.13d).^[150]

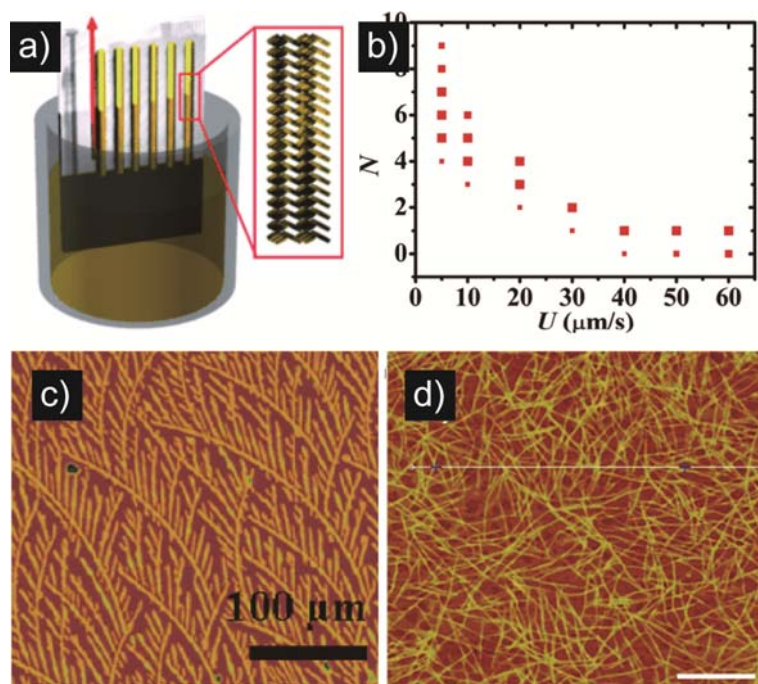


Figure 1.13 a) Schematic illustration of dip-coating,^[148] b) Dependence of layer number of DTBDT monolayer on the dip-coating speed, and c) AFM image of DTBDT monolayer.^[111] d) AFM image of PBTTT nanofibers deposited by dip-coating.^[150]

1.4.2.4 Zone-Casting

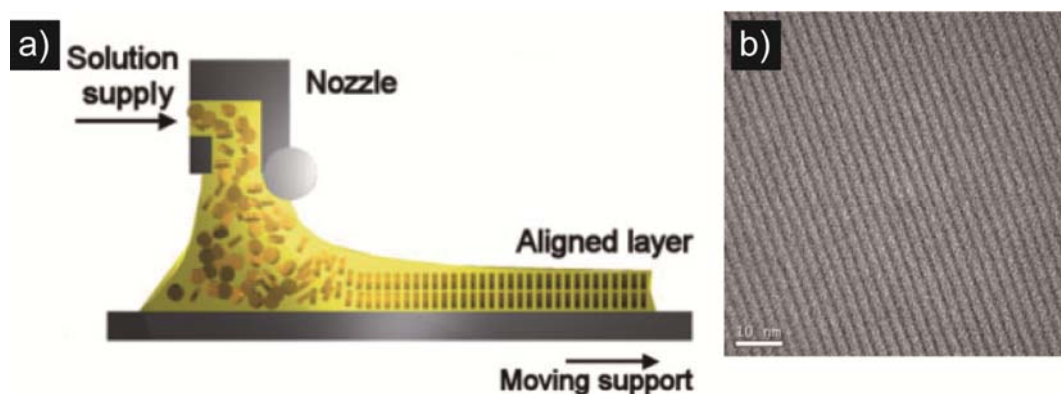


Figure 1.14 a) Schematic illustration of zone-casting; b) the high-resolution transmission electron microscope (HRTEM) image of a HBC derivative thin film by zone-casting.^[151]

In addition, the molecular orientation of organic semiconductors on the substrate can be efficiently improved by zone-casting.^[151-153] During zone-casting, the organic semiconductor solution was supplied through a flat nozzle and deposited onto a moving support (substrate), as shown in Figure 1.14a.^[151] The substrate motion was beneficial for the alignment of organic molecules. Furthermore, the temperatures of the solution and the substrate could be precisely controlled providing the possibility to optimize the kinetics of molecular self-assembly. Hexa-peri-hexabenzocoronene (HBC) derivatives are well known as discotic liquid-crystalline semiconductors, however, these molecules typically show a strong tendency towards aggregation already in solution making solution processing difficult.^[154] Interestingly, a HBC derivative was self-organized by zone-casting along the casting orientation with long-range order of the columnar structures (Figure 1.14b).^[151] Similar with zone-casting, blade-coating^[155] and its advanced version, solution shearing^[156], also have the capability to deposit thin films with good orientation. However, it must be emphasized that sometimes the solution temperature that is controllable only in zone-casting may become the key parameter to determine the microstructure of deposited thin films.

1.4.3 Other Techniques

In comparison to four solution processing approaches mentioned above, printing techniques such as inkjet printing^[98] and roll-to-roll printing^[157], have a great potential to revolutionize the existing electronics field due to their capability of the mass production of low-cost, flexible digital devices in a variety of substrates such as plastic, paper or even textiles. Therefore, organic electronics is also named “printed electronics”.^[133] One obvious advantage of printed electronics is cost saving, because the materials including semiconductor, dielectric and electrodes are deposited where they are required. Moreover, the overall complexity of the device manufacture process is greatly simplified. Typically, there are only two steps, printing and curing processes, allowing the fabrication of a working functional device from a bare substrate.

Although the performance and reliability of printed components are generally lower than their non-printed counterparts, printed electronics can also be seen as an entirely new market and industry.^[25, 158]

One has to admit the reality that almost each processing technique has its own shortcomings that cannot be completely avoided, but the post-treatments of as-cast semiconducting layers/devices including thermal annealing and solvent vapor annealing seem to be effective to further improve their microstructure and molecular ordering.^[159-160] It is demonstrated that thermal annealing leads to an obvious transition of molecular ordering from face-on to edge-on arrangement for diketopyrrolo-pyrrole (DPP) based polymers, and the organization of edge-on domains is also greatly improved.^[161] Consequently, a significant increase in the mobility of resultant transistors is observed. Similar effects of thermal annealing are also reported for small molecules such as perylene diimides and their derivatives.^[162] On the other hand, the annealing under solvent vapor atmosphere, defined as solvent-vapor annealing, allows the fine control of molecule-solvent, molecule-substrate, molecule-molecule and solvent-substrate interactions, in which the choice of the vapor solvent plays a key role in the microstructure of the deposited thin films.^[163] Both of post-treatments can be considered as the efficient compensatory methods of the existing solution processing techniques.

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Chapter 2

Motivation

Organic transistors with field-effect mobilities over $10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ have been realized for a variety of organic systems, and the mobility record is continuously increased. These reported OFET performances are comparable to or even higher than those of amorphous silicon transistors. However, OFETs are still far away from large-scale commercialization in industry. A good understanding of the relationship between molecular self-assembly of organic semiconductors and device performance in mono- to multilayer transistors is able to provide new insights into the fabrication of high-performance OFETs. In particular, the charge carrier transport at the interface between organic semiconductor and dielectric is of vital importance, which requires a further investigation (section 2.1). On the other hand, the evolution of microstructure and molecular ordering of semiconducting layer in OFETs is primarily determined by processing methods and processing parameters, which should receive much attention in order to enhance transistor performance (sections 2.2 and 2.3). Finally, traditional solution processing suffers from its limitation such as the prerequisite of good solubility of organic semiconductors, therefore, new techniques are in high demand to enlarge its applicability in organic electronics (section 2.4).

2.1 Impact of Interfacial Microstructure on Charge Carrier Transport

Although considerable achievements have been made on the influencing factors of OFET performance as introduced in chapter 1.3, the mechanism of charge carrier transport in organic transistors is still not fully understood yet. It is widely proven that the first few monolayers adjacent to the dielectric play a dominant role in charge carrier transport.^[1] However, in most reports^[1-3] the microstructure and molecular ordering almost remain unchanged. Therefore, one interesting question arises: what if the first few monolayers close to the dielectric are relatively disordered, but the upper ones are highly ordered? In other words, what is the intrinsic role of interfacial microstructure on charge carrier transport through a bulk film?

A common conjecture would be that the OFET performance should be remarkably reduced, or the field-effect behavior may even disappear, because the charge carrier transport is supposed to be significantly hindered by the disordered microstructure in the first few layers where charge carriers are accumulated. Indeed, it seems that many reports^[4-7] on the dependence of transistor performance on dielectric roughness support the above conjecture. However, so far there has been no direct evidence to confirm such intrinsic role of interfacial microstructure yet, because most studies employed the dielectrics with surface roughness on a nanometer scale that is comparable to the thickness of an organic semiconductor monolayer. As a result, the control of only interfacial microstructure may be achieved by using dielectrics with smaller surface roughness than the reports.

In chapter 3, I focus on developing a simple solution method to create dielectrics with a surface roughness within a narrow range on a sub-nanometer (sub-nm) scale. Organic semiconductors including a semicrystalline 5,6-difluorobenzothiadiazole based polymer, FBT-Th₄(1,4), an amorphous polymer poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine] (PTAA) and a crystalline cyano substituted perylenediimide (PDI₈-CN₂) are deposited by dip-coating from mono- to multilayers on the dielectrics

with sub-nm roughness. The choice of these three semiconducting compounds allows the clarification whether variations in chemical structure and crystallinity of organic compounds, and nature of charge carriers play a role on the relation between surface roughness and morphology. Careful inspection of the microstructure in different layers is carried out, and it is revealed that the microstructure of the interfacial monolayer is strongly dependent on the dielectric roughness but the microstructure of upper layers remains unchanged. This gives the opportunity to investigate the intrinsic role of interfacial microstructure on charge carrier transport. The electrical characterizations of all semiconductor systems in chapter 3 demonstrate that interfacial microstructure has basically no impact on charge carrier transport in multilayers.

Solution processing is employed to deposit semiconducting layers in chapter 3, but strong π -interactions between conjugated molecules are able to induce aggregation in solution before and during processing, which could, to some extent, affect the roughness dependence of molecular self-assembly and subsequently the final conclusion.^[8-10] Therefore, this suggests to also utilize vacuum sublimation that is effective to avoid aggregation in solution, by which the conclusion in chapter 3 can be further verified. In chapter 4, an α,ω -dihexylsexithiophene (α,ω -DH6T) is sublimed in high vacuum on dielectrics with sub-nm roughness. The film deposition in a layer-by-layer fashion confirms the strong and diminished dependence of microstructure on dielectric roughness for mono- and multilayers, respectively. More importantly, chapter 4 reveals an identical conclusion to chapter 3 providing a further understanding on the mechanism of charge carrier transport in OFETs.

2.2 High Performance Polymer Monolayer Transistor

Organic transistors based on a single molecular layer, termed as monolayer transistors, are an ideal platform for the investigation of charge carrier transport because of their two dimensional transport. Furthermore, monolayer transistors also own great potentials in applications such as chemical and biological sensors with fast

response and high sensitivity.^[11-13] Up to now, a few reports successfully realized the fabrication of working monolayer transistors on the basis of oligothiophenes and their derivatives, and moderate field-effect mobilities on the order of $10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ were obtained.^[2, 11, 14-15] Especially, a two-dimensional single crystal with monolayer thickness was processed in solution resulting in the mobility up to $1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[16]

In comparison to their small molecule counterparts, semiconducting polymers have higher flexibility and better compatibility with plastic substrates, both of which are essential for future flexible electronics. However, it is still a great challenge to fabricate high-mobility polymer monolayer transistors.^[17-22] This is the main motivation of chapter 5 where I focus on FBT-Th₄(1,4). The microstructure of the FBT-Th₄(1,4) monolayer can be well controlled by dip-coating, and the corresponding monolayer transistor leads to an excellent charge carrier transport with the field-effect mobility over $3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. This is a mobility record for organic monolayer transistors so far and opens the door towards ultraflexible monolayer-thick devices in organic electronics.

2.3 Control of Polymer Aggregation and Surface Organization

The control of the molecular organization on surfaces is a challenging, but significant topic which is important for the device performance of organic photovoltaics (OPVs)^[23] and OFETs^[24]. The molecular orientation of P3HT was reported to change from face- to edge-on fashion with increasing regioregularity from 81 % to 96 %.^[24] Moreover, the side chains of diketopyrrolopyrrole (DPP) based polymers critically affected the thin film organization on the surface.^[25] Strictly speaking, the chemical structures of polymers mentioned above vary to some extent. In other words, there is no effective method to tune the surface organization for a given compound yet. This is the motivation of chapter 6. I find that the kinetic control of FBT-Th₄(1,4) pre-aggregation in solution can be achieved by solvent tuning. When the polymer strongly aggregates in solution, the processed thin films show high crystallinity with edge-on molecular arrangement resulting in mobilities of $\sim 2 \text{ cm}^2$

$\text{V}^{-1} \text{s}^{-1}$. On the contrary, when the polymer pre-aggregation in solution is released, as-cast thin films are oriented in a face-on fashion causing a dramatic decline in mobility by two orders of magnitude.

2.4 New Solution Approach for Fabrication of Ultrathin OFETs

In spite of its versatility and practical significance, traditional solution processing possesses some specific requirements for organic semiconductors such as a good solubility in common solvents to obtain homogeneous thin films. As a result, conjugated compounds with high mobility but poor solubility, such as pentacene, can be hardly processed from solution. Moreover, a large amount of organic solvents is usually applied during solution processing, which is harmful to the environment. Therefore, efficient but environmentally friendly processing techniques are still in high demand. In chapter 7, I focus on a new solution processing method, termed as two-phase dip-coating, to deposit organic semiconductor ultrathin films with well-defined microstructures for OFET devices, with the assistance of a surfactant solution. It is proven that this two-phase dip-coating is a lower-cost but more environmentally friendly solution method because only few μg of the organic semiconductor and few μL of the organic solvent are required to fabricate aligned microstripes over a cm^2 large area. Additionally, the results based on four different semiconductor systems indicate that this method is a general method to align organic semiconductors, especially for conjugated molecules with poor solubility.

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Chapter 3

Impact of Interfacial Microstructure on Solution Processed Organic Field-Effect Transistors

3.1 Introduction

Dielectric surface properties, such as chemical composition, surface energy, surface viscoelasticity, and especially surface roughness critically affect the semiconductor film microstructure determining device performances of resultant transistors.^[1-3] A few previous studies reported the influence of dielectric surface roughness on the organic semiconductor layers, but only relatively thick films of between 50 nm and 150 nm were investigated with the dielectric surface roughness in the nanometer range.^[2, 4-7] These nanoscale-roughness dielectrics were comparable to or even larger than the molecular dimension of organic semiconductors so that the microstructure varies through the entire semiconducting film (Figure 3.1a), disallowing the investigation of the intrinsic role of interfacial semiconducting layer in charge carrier transport. A method that enables the microstructure control of organic semiconductors in a higher precision is required.

The deposition procedures of organic semiconductors could cause film inhomogeneity perpendicular to the substrate. For instance, during the deposition by organic molecular beam deposition (OMBD) thin films underwent an orientational and structural transition leading to lateral inhomogeneity.^[8] Such transition could be

kinetically controlled by using different temperatures or substrates to tune the molecule/substrate interactions.^[8] In the case of conjugated polymers including poly(N,N-bis-2-octyldodecyl-naphthalene-1,4,5,8-bis-dicarboximide-2,6-diyl-alt-5,5'-2,2'-bithiophene) (P(NDI2OD-T2))^[9] and poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3,2-b]thiophene) (PBTTT)^[10], a spatial inhomogeneity was also reported in solution-processed thin films significantly influencing the charge carrier transport in transistors. However, it is still a great challenge to precisely modify the microstructure of only the interfacial monolayer and to investigate its impact on the charge carrier transport in solution-processed transistors.

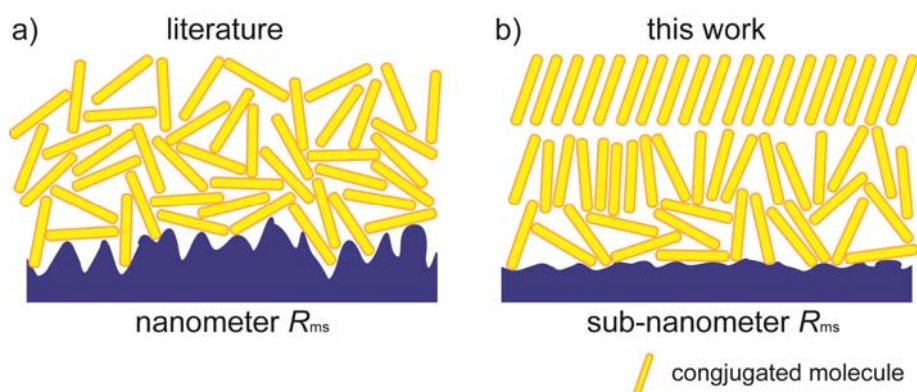


Figure 3.1 Conceptual comparison between the literature and this chapter.

In this chapter, a highly efficient solution approach is proposed to precisely tune surface roughness of the dielectric surface within a very narrow range on a sub-nanometer scale from 0.15 to 0.39 nm. The dielectric surface that shows sub-nanometer roughness allows the control of only the interfacial microstructure in the organic semiconductor film, without affecting the morphology in the upper layers, as shown in Figure 3.1b. The surface properties of the modified dielectrics are characterized in section 3.2. Subsequently, the influence of sub-nm dielectric roughness on the conjugated polymer monolayer is discussed in section 3.3. In order to investigate the impact of interfacial microstructure on the charge carrier transport, crystalline, semicrystalline and amorphous conjugated molecules are investigated allowing the clarification whether the chemical structure and film microstructure of

organic semiconductors, and nature of charge carriers play a key role for the relation between surface roughness and morphology (section 3.4). Finally, in section 3.5, a by-passing transport mechanism is proposed to interpret the role of interfacial microstructure on charge carrier transport.

3.2 Dielectrics with Sub-Nanometer Surface Roughness

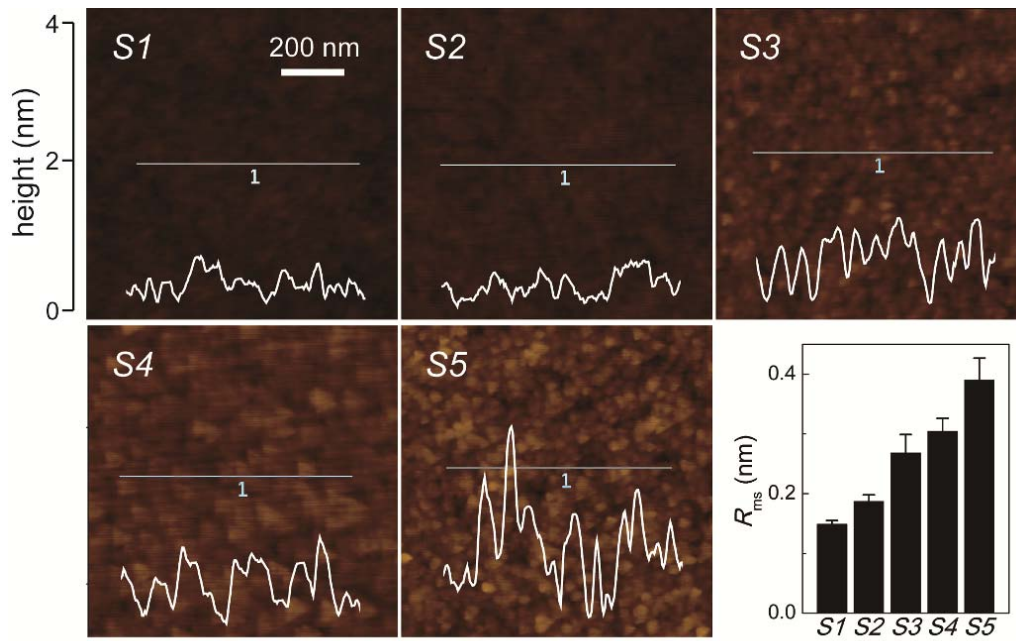


Figure 3.2 AFM images of the topography of **S1-S5**, in which the white lines indicate the integrations of the height plots with corresponding height tick label from 0 to 4 nm displayed at the left. All images have the same scale bar. The bottom right figure summarizes the R_{ms} value of **S1-S5**.

Up to now, several approaches have been developed to control the surface roughness of SiO_2 , including direct sputtering^[4], reactive ion etching^[7, 11], and plasma-enhanced chemical vapor deposition (PECVD)^[6, 12]. However, their potential in practical use is limited due to high cost and slow processing. On the other hand, their precision is relatively low, only on a nanometer scale. A single molecular layer (monolayer) of organic semiconductor possesses a thickness of only 1-3 nm, so the

nanoscale roughness is incapable of precisely tuning the self-assembly of organic semiconductor monolayer. Hence, a simple but efficient solution method is proposed in this chapter to modify the surface of dielectrics (SiO_2) resulting in the surface roughness ranging from 0.15 to 0.39 nm. The details of experiments and characterizations are described in chapter 9.1. The topography of these spin-coated SiO_2 layers is characterized by AFM in tapping-mode, as shown in Figure 3.2. An isotropic surface is observed in all cases. Corresponding height plots clearly depict a continuous increase in roughness from **S1** to **S5**. The surface roughness is quantified by the root-mean-square value (R_{ms} , the detailed definition is described in chapter 9.1.2). The average R_{ms} for each dielectric is calculated from 5-8 AFM images of $2 \times 2 \mu\text{m}^2$ in size, with values of 0.149 ± 0.006 , 0.187 ± 0.011 , 0.268 ± 0.031 , 0.304 ± 0.022 and 0.390 ± 0.037 nm for **S1-S5**, respectively (Figure 3.2).

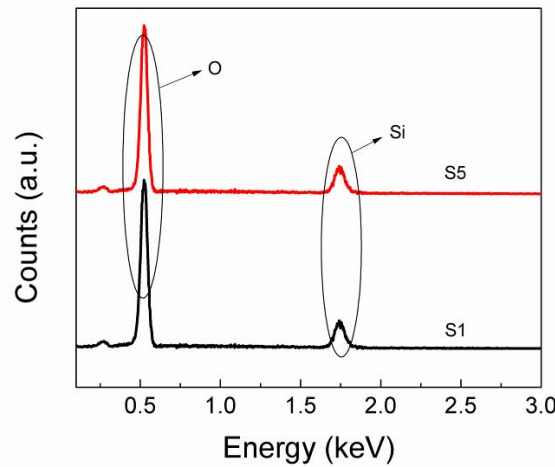


Figure 3.3 EDX data of substrates of **S1** and **S5**.

The surface properties of these spin-coated SiO_2 layers are explored by energy-dispersive X-ray spectroscopy (EDX) firstly. It is clear from EDX profiles in Figure 3.3 that **S1** and **S5** exhibit similar curves, where two peaks at 0.52 and 1.74 keV match elements of oxygen and silicon, respectively. The small peak at 0.27 keV is related to the carbon contamination arising from intrinsic sources of the SEM system. On the other hand, a contact angle measurement is performed, as shown in

Figure 3.4. 3 μL of H_2O is utilized for the measurement. **S1-S5** reveal identical contact angle values ranging from 48° to 55° suggesting that these spin-coated SiO_2 layers do not have any difference in surface energy. The results from both measurements demonstrate that **S1-S5** have the same surface properties and only differ in the surface roughness. This spin-coated layer is only 10 nm in thickness.

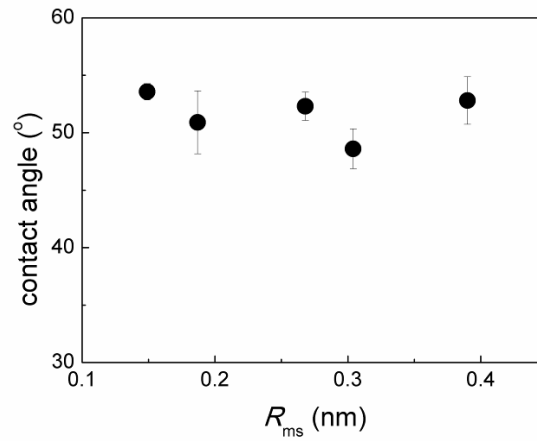


Figure 3.4 Contact angles of dielectric surfaces with different sub-nanometer roughnesses. 3 μL of H_2O is utilized for the measurement.

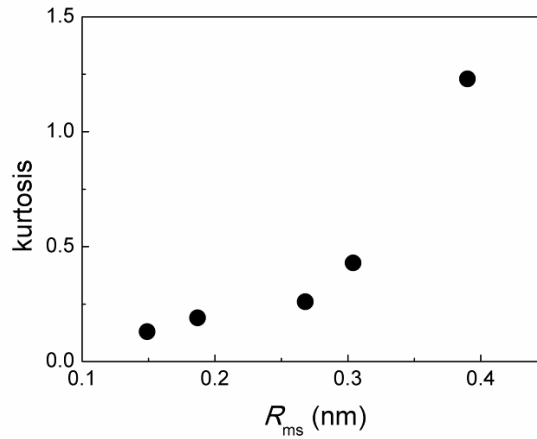


Figure 3.5 The dependence of kurtosis on the dielectric roughness. Gwyddion software is used for analysis.

Surface kurtosis describes the sharpness of the probability density of the height profile, and its definition is discussed in chapter 9.1.2. If the value of kurtosis is less

than 3, the investigated surface is platykurtotic with relatively few high peaks and low valleys. If it is larger than 3, the surface is leptokurtotic with relatively many high peaks and low valleys.^[13] A higher kurtosis will induce more nucleation sites.^[14] However, in this chapter, the kurtosis evaluated from AFM images is far lower than 3 for all dielectrics (**S1-S5**) (Figure 3.5). In particular, the kurtosis for **S1-S4** is even <0.5 . These results demonstrate that there are very few high peaks and low valleys. Therefore, the influence of surface kurtosis is negligible, but the surface roughness (R_{ms}) is selected as the key parameter to be studied.

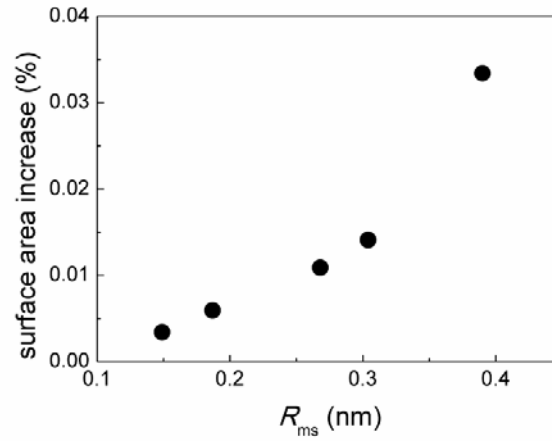


Figure 3.6 Surface area as a function of the roughness. AFM images with $8 \times 8 \mu\text{m}^2$ in area are analyzed for **S1-S5**, and the increase in surface area is defined as $(A-A_0)/A_0$, where A is the actual measured surface area by AFM and A_0 of $8 \times 8 \mu\text{m}^2$ is the scan size of the images. Gwyddion software is used for analysis.

For a bare wafer with 300 nm SiO_2 , the dielectric capacitance per unit area, C_i , is $11.510 \text{ nF cm}^{-2}$, but the increased surface area by surface roughness is not taken into account. All dielectrics **S1-S5** share the same dielectric thickness with the value of 310 nm. In an ideal case, $R_{ms}=0$, the value of C_i is $10.962 \text{ nF cm}^{-2}$. However, in this chapter the surface roughness of dielectric is precisely tuned so that the surface area increases, as shown in Figure 3.6. The increase in surface area is defined as $(A-A_0)/A_0$, where A is the actual measured surface area by AFM and A_0 of $8 \times 8 \mu\text{m}^2$ is the scan size of the images. Such an increase in surface area only ranges from 0.0034% (**S1**) to

0.033% (S5). Taking the effect of R_{ms} into consideration, the value of C_i for the dielectric investigated in this study is ranging from 10.962 (S1) to 10.958 nF cm⁻² (S5). Therefore, the capacitance variation is neglected.

3.3 Interfacial Microstructure of Organic Semiconductors

3.3.1 Semicrystalline Conjugated Polymers

Among organic semiconductors, donor-acceptor copolymers are of great interest, because their optoelectronic properties can be efficiently tuned by rational tailoring of electron-donating and electron-accepting units.^[15] One successful example is the copolymer utilizing cyclopentadithiophene (CDT) as the donor block and benzothiadiazole (BT) as the acceptor block.^[16-17] Poly[2,6-(4,4-bis(2-ethylhexyl)-4H-cyclopenta[2,1-b:3,4-b']dithiophene)-alt-4,7-(2,1,3-benzothiadiazole)] (PCPDTBT, Figure 3.7) has received extensive attention since its first report, because it performs well in both OPVs and OFETs.^[16] In particular, the HOMO level of this polymer (5.3 eV) is close to the work function of gold (5.1 eV) that is the most common electrode material, facilitating the charge carrier transport in OFETs. In this chapter, PCPDTBT is firstly deposited into a monolayer by dip-coating technique. Dielectrics with sub-nanometer roughness are employed to kinetically control the self-assembly of this conjugated polymer.

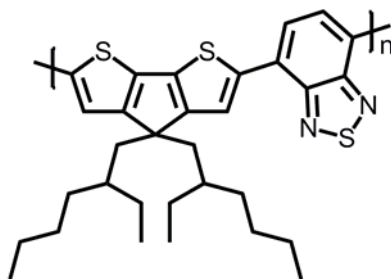


Figure 3.7 Chemical structure of poly[2,6-(4,4-bis(2-ethylhexyl)-4H-cyclopenta[2,1-b:3,4-b']dithiophene)-alt-4,7-(2,1,3-benzothiadiazole)] (PCPDTBT).

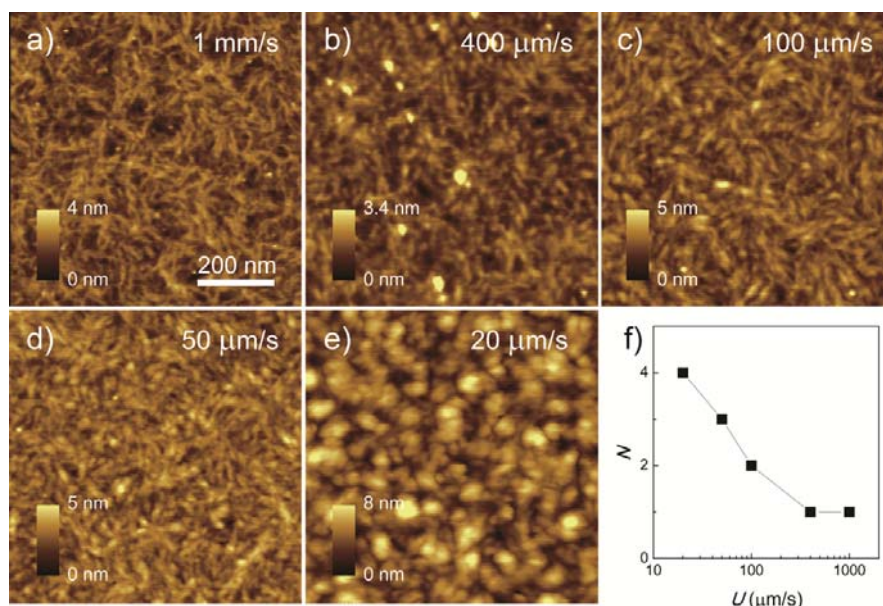


Figure 3.8 a-e) AFM images of PCPDTBT ultrathin films by dip-coating from 0.5 mg/mL chloroform solution at the pulling speeds (U) of 1000, 400, 100, 50 and 20 μm/s, respectively. f) The layer numbers (N) as a function of U . All images have the same scale bar.

PCPDTBT was synthesized using a general polymerization procedure according to a modified literature procedure.^[17] The molecular weight (M_n) and polydispersity index (PDI) by GPC are 40 K g/mol and 5 separately. The deposition of PCPDTBT ultrathin films can be controlled from monolayer to multilayers by dip-coating from 0.5 mg/mL chloroform solution. Commercial silicon wafers with 300-nm-thick thermally grown SiO_2 are used as the substrates. Five dip-coating speeds are chosen for the film deposition which are 1000, 400, 100, 50 and 20 μm/s, respectively. Figure 3.8 shows the topography of resultant PCPDTBT thin films. At 1 mm/s, a single molecular layer consisting of fine nanofibers is fabricated with ~2 nm in thickness (Figure 3.8a). This value is in agreement with the interlayer distance found previously for this copolymer by X-ray scattering.^[18] Therefore, it can be assumed that the polymer backbone of PCPDTBT is arranged edge-on towards the surface. The decrease in dip-coating speed obviously enlarges the fiber dimension. At 20 μm/s, fiber-like microstructure disappears, but larger domains with a stronger crystallinity are formed, as shown in Figure 3.8e. On the other hand, lower dip-coating speeds

induce the deposition of more molecules on the substrate resulting in the formation of multilayers (Figure 3.8f). In other words, the film thickness is strongly dependent on the dip-coating speed.^[10, 19] No further functionalization is applied to the dielectric surface, because the surface modification of dielectrics by self-assembled monolayers (SAMs) such as hexamethyldisilazane (HMDS) generally creates a hydrophobic surface that has a detrimental impact on the molecular deposition on the substrate.

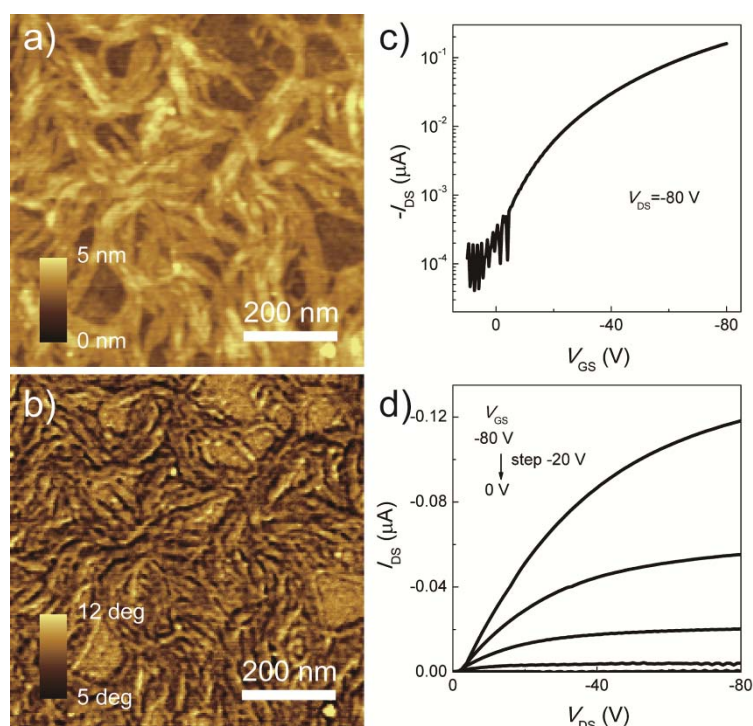


Figure 3.9 AFM height (a) and phase (b) images of PCPDTBT monolayer with the dielectric roughness of 0.187 ± 0.011 nm. Transfer (c) and output (d) characteristics of corresponding monolayer transistor.

The self-assembly of PCPDTBT monolayer on dielectrics with sub-nm roughness is investigated. The smoothest surface used here has the R_{ms} value of 0.187 ± 0.011 nm, which is little smaller than that of the commercial silicon wafer (0.197 ± 0.013 nm). As determined by AFM, the PCPDTBT monolayer deposited on such dielectric surface is also composed of nanofibers with 10 nm in diameter identical to that on silicon wafer (Figure 3.9a,b). This well-defined microstructure on the flat surface reveals a good self-assembly behavior of PCPDTBT facilitating the

charge carrier transport. OFET devices are fabricated based on such monolayer with a top-contact bottom-gate configuration. The specific transfer and output plots of the monolayer exhibit a typical linear/saturation behavior, as shown in Figures 3.9c,d. At a gate voltage (V_{GS}) of -80 V, the drain current ($-I_{DS}$) reaches 0.2 μA . The hole mobility (μ_h) of this monolayer transistor is $5.08 \pm 0.67 \times 10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, with the maximum value of $6.42 \times 10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. It must be emphasized that this μ_h value is not optimized but underestimated because i) no special surface treatment for the dielectric is applied, such as use of SAMs such as HMDS to decrease charge carrier trapping; ii) the mobility calculation is carried out for a fully covered monolayer which is not the case here. The on/off ratio of the monolayer is around 10^3 .

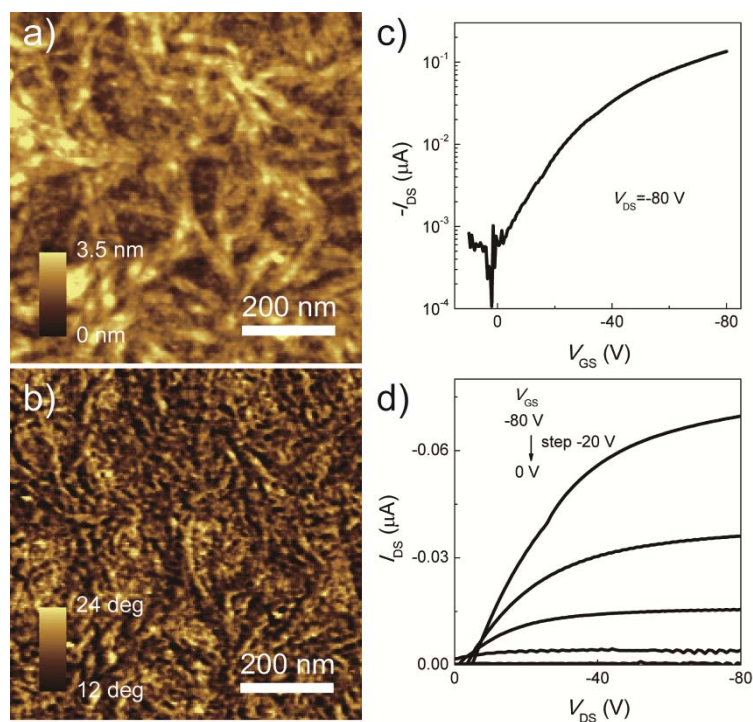


Figure 3.10 AFM height (a) and phase (b) images of PCPDTBT monolayer with the dielectric roughness of 0.268 ± 0.031 nm. Transfer (c) and output (d) characteristics of corresponding monolayer transistor.

A slight increase in R_{ms} to 0.268 ± 0.031 nm does not lead to a significant change in polymer self-assembly. The nanofiber based monolayer is still obvious with a minor reduction in fiber dimension as well as the appearance of small aggregates, as

determined by the AFM height and phase images (Figure 3.10a,b). Hence, it is reasonable to expect a decrease in charge carrier transport due to the less pronounced molecular organization. In comparison to $R_{\text{ms}} = 0.187 \pm 0.011$ nm, the PCPDTBT monolayer at $R_{\text{ms}} = 0.268 \pm 0.031$ nm exhibits lower drain currents under the same measurement parameters, as shown in Figure 3.10c,d. The saturation mobility extracted from transfer plots is $3.65 \pm 0.13 \times 10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ with on/off ratio of 10^2 - 10^3 . The decrease in mobility by 28% can be attributed to two aspects. On the one hand, more trapping sites are induced at semiconductor/dielectric interface by a higher R_{ms} so that the charge carrier transport is decreased. On the other hand, the surface scattering on charge carriers is intensified, hindering the movement of charge carriers along the working channel.^[4, 20]

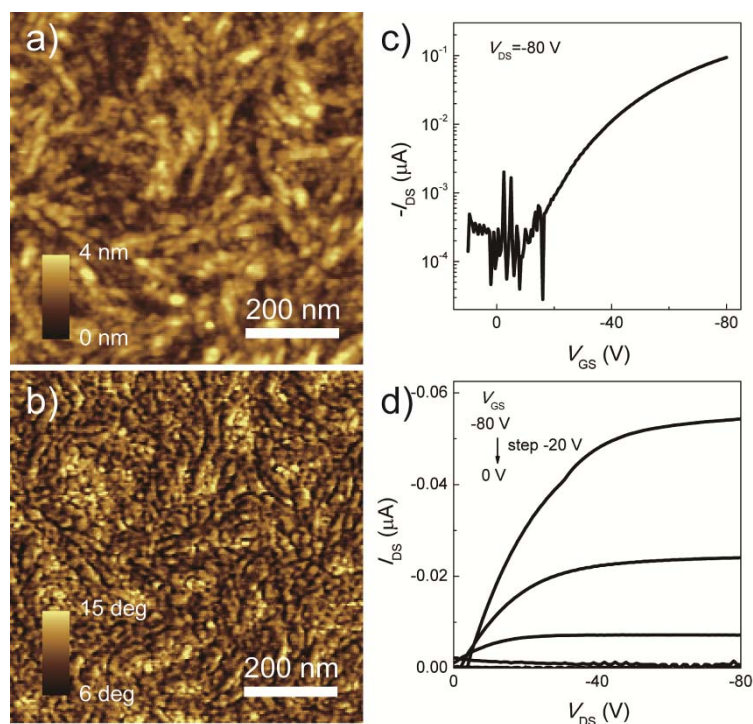


Figure 3.11 AFM height (a) and phase (b) images of PCPDTBT monolayer with the dielectric roughness of 0.304 ± 0.022 nm. Transfer (c) and output (d) characteristics of corresponding monolayer transistor.

With a further increase of the dielectric roughness to 0.304 ± 0.022 nm, the chain mobility of the conjugated polymer is continuously reduced lowering the propensity

to self-assembly. AFM images in Figure 3.11a,b show more aggregates although a fiber-like microstructure is still observed. These aggregates are composed of numerous small domains inducing more grain boundaries, structural defects and the formation of amorphous region. Consequently, the hole transport of PCPDTBT monolayer is gradually deteriorated with a charge carrier mobility of $3.40 \pm 0.59 \times 10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (Figure 3.11c,d). The output characteristics in Figure 3.11d reveal a nonlinear behavior of I_{DS} at low V_{DS} indicating contact resistance and charge injection limitation.^[21-22]

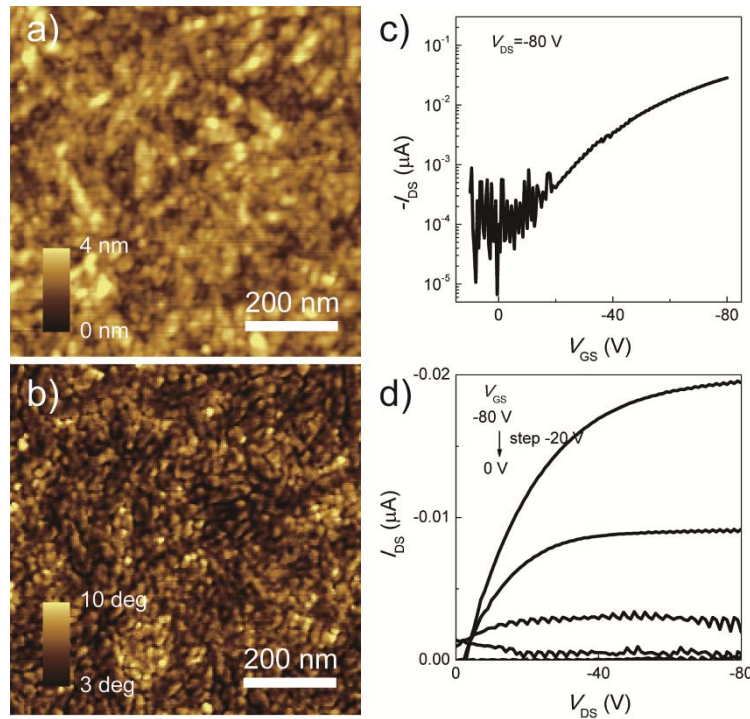


Figure 3.12 AFM height (a) and phase (b) images of PCPDTBT monolayer with the dielectric roughness of $0.390 \pm 0.037 \text{ nm}$. Transfer (c) and output (d) characteristics of corresponding monolayer transistor.

When a dielectric with higher R_{ms} value is utilized to deposit the PCPDTBT monolayer, the long-range ordering of PCPDTBT is significantly hindered, with a transition of the polymer self-assembly from an ordered (nanofibers) to a disordered microstructure (granular aggregations). (Figure 3.12a,b) This transition originates from the insufficient PCPDTBT chain mobility that cannot overcome the

roughness-induced barrier.^[23] The corresponding monolayer reveals not only a much poorer organization, but also more grain boundaries resulting in a low μ_h value of $1.01 \pm 0.22 \times 10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. This significant decline in hole mobility correlates well with the decrease in $-I_{DS}$ by approximately one order of magnitude from 0.2 to 0.03 μA (Figure 3.12c,d). Furthermore, the transfer curve at low V_{GS} exhibits an obvious trapping effect as well as a higher turn-on voltage. In addition, both transfer and output characteristics indicate a stronger effect of contact resistance and charge injection limitation.^[10]

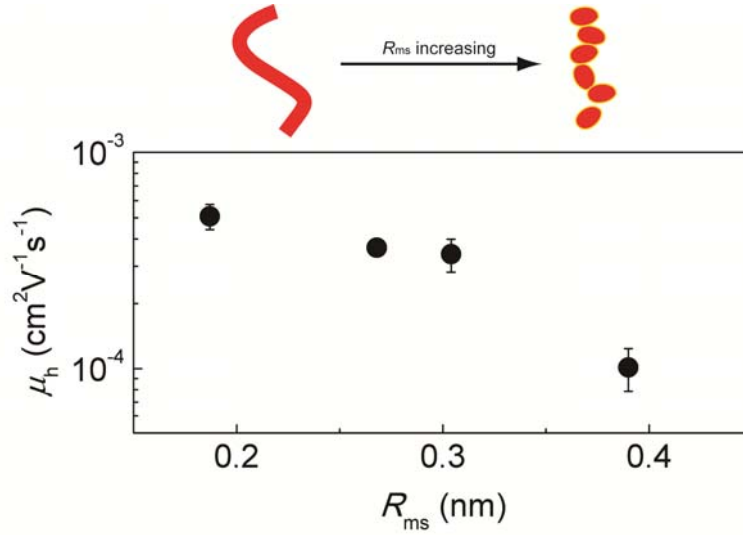


Figure 3.13 The dependence of hole mobility of PCPDTBT monolayer on the dielectric roughness.

Table 3.1 The on/off ratio (I_{on}/I_{off}) and threshold voltage (V_{th}) of PCPDTBT monolayer on dielectrics with various R_{ms} .

R_{ms}	0.187±0.011	0.268±0.031	0.304±0.022	0.390±0.037
I_{on}/I_{off}	10^3	$10^2 \sim 10^3$	$10^3 \sim 10^4$	$10^2 \sim 10^3$
V_{th} (V)	-20~-15	-5~0	-25~-5	-20~-10

The dependence of transistor performance of a PCPDTBT monolayer on the dielectric roughness is summarized in Figure 3.13 and Table 3.1. It can be clearly seen that the hole mobility is reduced with increasing the value of R_{ms} , which is in good

agreement with the reported “roughness valley” theory.^[4] Besides the increased density of charge trapping and surface scattering induced by a higher R_{ms} , the molecular ordering is another factor responsible for the significant decline in charge carrier transport, as shown in Figure 3.13 (top figure). In contrast to the highly organized monolayer (nanofibers) on the smooth dielectric ($R_{\text{ms}} = 0.187 \pm 0.011$ nm), the molecular self-assembly is severely inhibited by the roughness-induced barrier ($R_{\text{ms}} = 0.390 \pm 0.037$ nm) with the formation of aggregates. The low degree of molecular ordering and structural defects induced by dielectric roughness consequently hinder transport of charge carriers. Although the hole mobility is strongly dependent on the dielectric roughness, both on/off ratio and threshold voltage of PCPDTBT monolayer remain almost unchanged (Table 3.1), which benefits from the fact that the large molecular dimension of polymers seems to be effective to enable bridging of disordered regions.^[24]

Although a precise control of molecular self-assembly and charge carrier transport of PCPDTBT monolayer is realized by using a sub-nm dielectric roughness, the OFET performance of PCPDTBT thin films is relatively low with the saturation mobility on the order of $10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. There are three possible reasons for such behavior. First of all, it is related to the intrinsic electrical property of PCPDTBT. It is reported that the field-effect mobility record of PCPDTBT bulk films is only on the order of $10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[16] Moreover, the molecular ordering is relatively low so that the density of grain boundaries is high, which causes more energy barriers for charge carrier transport. Additionally, the dielectric is not functionalized, and the hydroxyl groups at the SiO_2 surface trap charge carriers.^[25] To investigate the mechanism of charge transport in transistors, a semiconducting polymer with higher mobility is desired.

The fluorination of the conjugated backbone is an efficient way to fine tune energy levels and improve the transistor performance. Theoretical studies indicated that the fluorinated BTs, FBTs, could significantly increase the planarity of the structure and decrease torsional disorder compared with that of BTs.^[26] In the case of a BT-oligothiophene copolymer, it was found that replacing the hydrogen atoms at the

5,6-positions of BT with fluorine not only facilitated the formation of highly ordered microstructures but also led to higher transistor performance with the hole mobility of around $0.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[27-28] More recently, a FBT based polymer, FBT-Th₄(1,4) (Figure 3.14 a), with a maximum field-effect mobility of $1.92 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ was reported by modulating the positions of alky chains on thiophenes.^[29] Therefore, the impact of interfacial microstructure on charge carrier transport is investigated by choosing FBT-Th₄(1,4) as the second model compound.

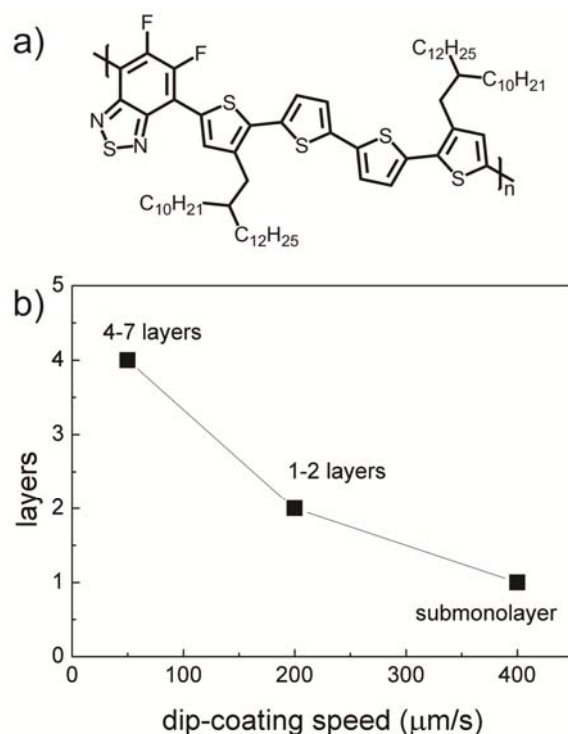


Figure 3.14 a) Chemical structure of FBT-Th₄(1,4). b) Thickness of deposited FBT-Th₄(1,4) films as a function of dip-coating speed. Chloroform is used as solvent, and FBT-Th₄(1,4) concentration is 0.5 mg/mL.

The synthesis procedures of FBT-Th₄(1,4) are described elsewhere.^[29] The molecular weight is $M_n=23.2 \text{ K g/mol}$ with $M_w/M_n=1.9$. Deposition of FBT-Th₄(1,4) thin films in a monolayer precision is performed by dip-coating from 0.5 mg/mL chloroform solution. The pulling speed exerts pronounced effect on the layer number, as shown in Figure 3.14b. At 400 $\mu\text{m/s}$ a polymer submonolayer can be fabricated consisting of fibrous nanostructures with the thickness of $\sim 2.4 \text{ nm}$ (Figure 3.15).

Furthermore, lower pulling speeds (200 and 50 $\mu\text{m/s}$) allow the deposition of more molecules on the substrate leading to the formation of multilayers. Herein, polymer thin films with three thicknesses are fabricated which are submono-, 1-2 and 4-7 layers. In the case of “4-7 layers”, the minimum height is ~ 12 nm and the maximum value is ~ 20 nm. Therefore, this kind of multilayer is called “4-7 layers”.

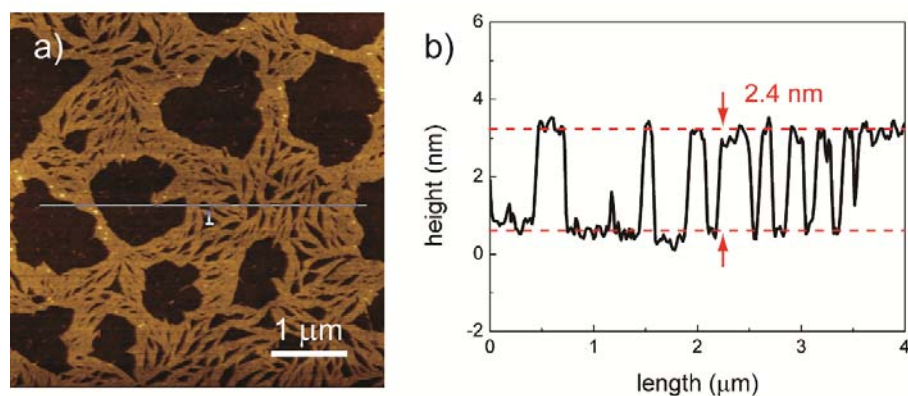


Figure 3.15 a) AFM image and b) the corresponding height profile of FBT-Th₄(1,4) submonolayer on the flat surface (S1). The submonolayer thickness is around 2.4 nm.

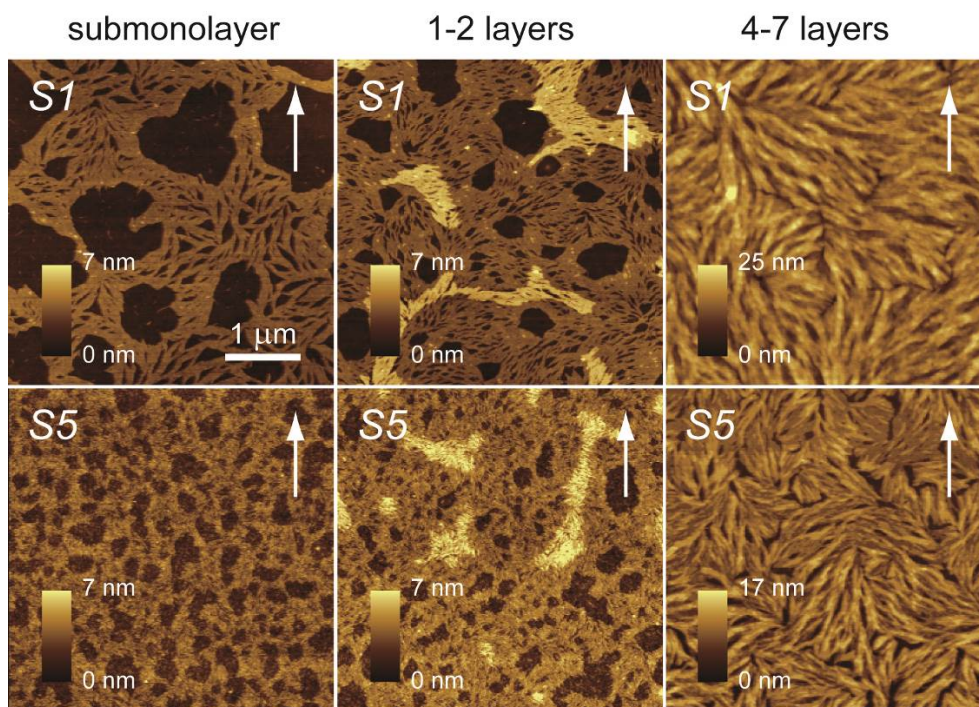


Figure 3.16 AFM images of FBT-Th₄(1,4) thin films dip-coated on S1 ($R_{\text{ms}}=0.149\pm0.006$) and S5 ($R_{\text{ms}}=0.390\pm0.037$ nm). All images have the same scale bar. The white arrows indicate the dip-coating direction.

Figure 3.16 shows the influence of dielectric roughness on the topography of FBT-Th₄(1,4) thin films with different thicknesses. After deposition, the organic semiconducting layer is immediately annealed at 100 °C for 30 min to remove the residual solvent and then cooled down to room temperature in nitrogen atmosphere. This annealing temperature is low and does not cause any effect on the deposited layers (Figure 3.18). The flat dielectric surface facilitates the self-assembly of the polymer resulting in the formation of long-fiber nanostructures at 400 μm/s (submonolayer). The random distribution of the FBT-Th₄(1,4) fibers does not imply any obvious preferential orientation of the polymer chains due to the processing. The average dimensions of fibers on **S1** ($R_{ms}=0.149\pm0.006$) are 71 nm in diameter, 635 nm in length and 2.4 nm in thickness, as shown in Figure 3.16 and 3.17. In contrast to the well-defined microstructure on **S1**, the rough surface, **S5** ($R_{ms}=0.390\pm0.037$ nm), induces the formation of clusters of much smaller size with fiber dimensions of 75% and 81% less in diameter and length, respectively. This disruption in polymer self-assembly can be ascribed to a higher number of nucleation sites and the limitation in fiber growth caused by high.^[11-12] Moreover, the submonolayer coverage on **S5** (70%) is slightly higher than that on **S1** (57%).

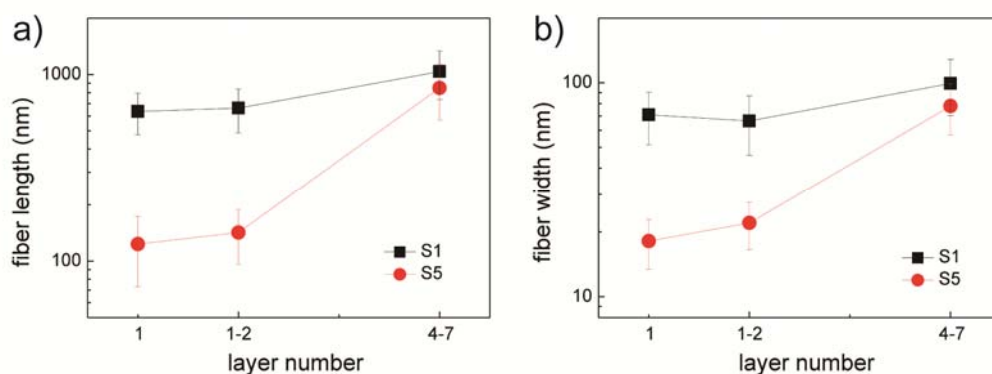


Figure 3.17 Fiber dimensions of FBT-Th₄(1,4) on the top film as a function of layer thickness and dielectric roughness. The analysis is obtained from 100 fibers for each sample.

A slower pulling speed (200 μm/s) improves the FBT-Th₄(1,4) monolayer

coverage and even induces the growth of the second layer, but the polymer nanofibers exhibit identical dimensions as the submonolayer (400 $\mu\text{m/s}$) when deposited on the dielectric of same surface roughness. Furthermore, the negative influence of high R_{ms} (**S5**) on the microstructure can be still clearly observed (Figure 3.16 and 3.17). At 50 $\mu\text{m/s}$, FBT- $\text{Th}_4(1,4)$ films with 4-7 molecular layers are deposited on the dielectric. It is interesting that the microstructure of FBT- $\text{Th}_4(1,4)$ multilayers seems independent of dielectric roughness. The fiber dimensions on **S5** obviously increase with values of 78 nm in diameter and 848 nm in length, which is similar to the sample on **S1**, as shown in Figure 3.16 and 3.17.

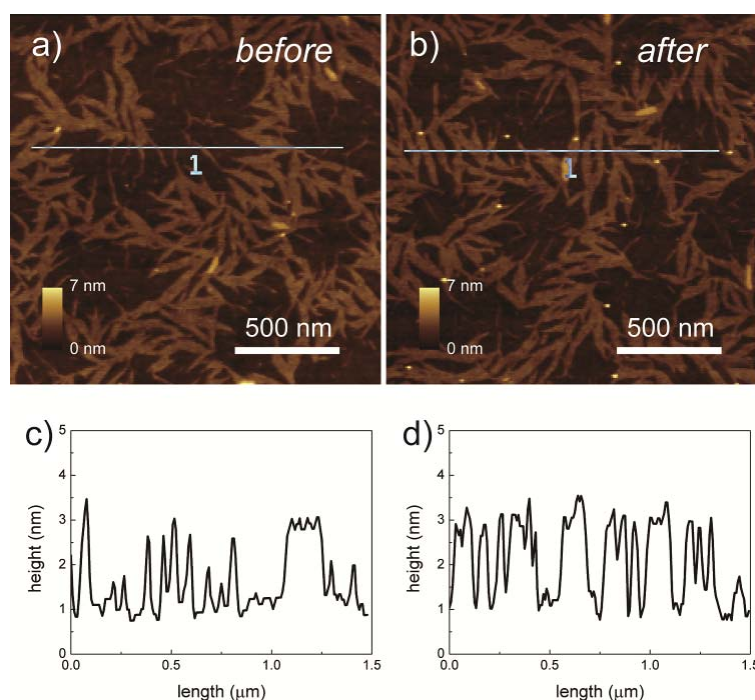


Figure 3.18 AFM images of FBT- $\text{Th}_4(1,4)$ submonolayers before (a) and after (b) annealing at 100 $^{\circ}\text{C}$ for 30 min. The films are dip-coated from 0.5 mg/mL chloroform solution on bare wafer with the speed of 400 $\mu\text{m/s}$. c-d) Corresponding height profiles for a) and b).

It has to be emphasized that these results based on AFM characterization describe only the film topography, and this comparison has to be handled with care since for thicker films the buried microstructure might differ. Recent studies on

dip-coated poly(2,5-bis(3-hexadecylthiophen-2-yl)thieno[3,2-b]thiophene) (PBTBT) revealed no change of the first monolayer during microstructure evolution of the bulk film.^[10] The same film growth can be expected in the current work. To directly explore the microstructure of the buried interfacial layer, FBT-Th₄(1,4) 4-7 layers are transferred from the dielectric surface with an assistance of poly(acrylic acid) (PAA), as shown in Figure 3.19a. Afterwards, the dielectric surface with FBT-Th₄(1,4) residuals (side *A*) and the bottom of PAA/GBT-Th₄(1,4) film (side *B*) are more closely inspected by AFM. For the sample on **S1**, both sides (*A* and *B*) show the same microstructure as on the top surface of FBT-Th₄(1,4) 4-7 layer film on **S1** as well as the submonolayer on **S1** (Figure 3.16 and 3.19b-c). On the contrary, mainly aggregates or eventually short fibers are observed on side *A* and *B* after the transfer of the sample from **S5**. This microstructure is identical to the FBT-Th₄(1,4) submonolayer on **S5** (Figure 3.16 and 3.19d-e), but completely different from the top surface of the 4-7 layer film on **S5**. The similarity of the microstructures for the buried interfacial layer in thicker films and submonolayers proves that the variation of dip-coating speed has basically no influence on the microstructure dimensions of the layers close to the dielectric surface which is consistent with previous report.^[10] More importantly, it is revealed that the buried interfacial layer is sensitive to the dielectric roughness in the same way as submonolayers although the top microstructure of thicker films appears independent on R_{ms} .

GIWAXS measurements provide more structural information on the FBT-Th₄(1,4) 4-7 layers (Figure 3.20). Multilayers on **S1** and **S5** display identical diffraction patterns confirming that the sub-nanometer roughness has a minor effect on the edge-on polymer organization in the entire film. An interlayer distance of 2.41 nm is calculated from the main reflection *100* (assigned to Miller index) positioned in the out-of-plane for $q_z=0.26 \text{ \AA}^{-1}$ and $q_{xy}=0 \text{ \AA}^{-1}$, which is consistent with the submonolayer thickness obtained from AFM characterization. The full width at half maximum (FWHM) of this reflection is used to determine the out-of-plane coherence length. FBT-Th₄(1,4) 4-7 layers on **S1** exhibit an only slightly larger coherence length of 14 nm in comparison to the film on **S5** (11 nm). The small decrease indicates the

reduced ordering at the dielectric surface. Since the corresponding π -stacking reflection is not evident in the GIWAXS pattern due to the intralayer disorder,^[29] the in-plane coherence length cannot be extracted.

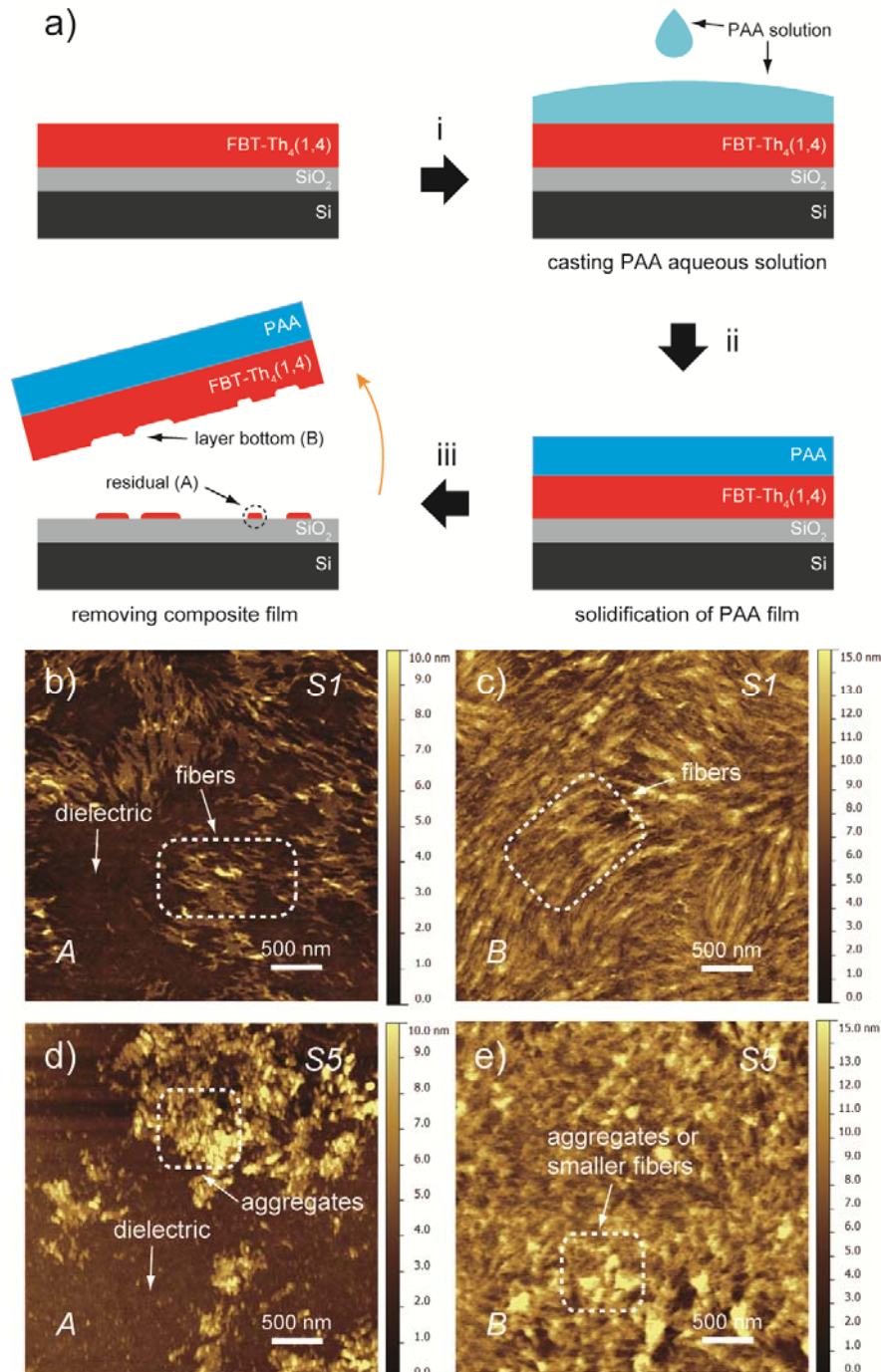


Figure 3.19 a) Schematic illustration of the transfer process of the FBT-Th₄(1,4) 4-7 layers from the dielectric surface. (i) 35% poly(acrylic acid) (PAA) aqueous solution is cast on top of the organic semiconductor layer. (ii) PAA film is solidified overnight

at room temperature. (iii) The PAA/FBT-Th₄(1,4) composite film is removed from the dielectric. Both the dielectric with FBT-Th₄(1,4) residuals (side *A*) and the bottom of PAA/FBT-Th₄(1,4) film (side *B*) are inspected to gain information about the microstructure of the buried interfacial semiconducting layer. AFM images of the buried interfacial microstructures of FBT-Th₄(1,4) 4-7 layers deposited on **S1** (b,c) and **S5** (d,e). All images have the same scale bar.

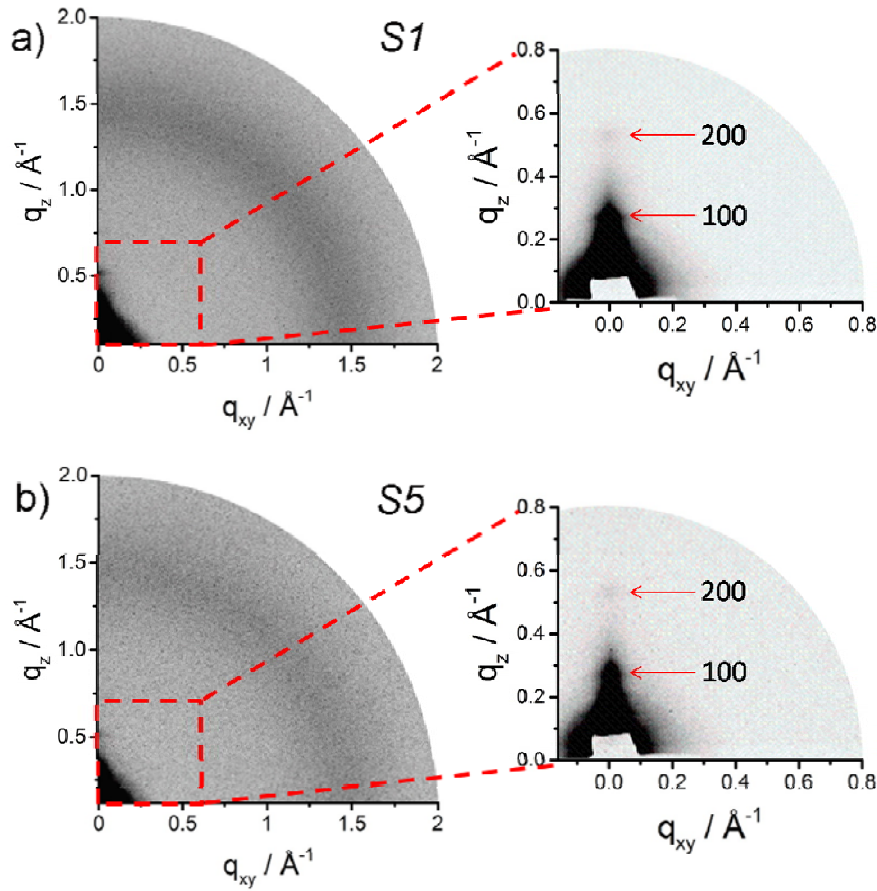


Figure 3.20 GIWAXS for FBT-Th₄(1,4) 4-7 layers deposited on **S1** (a) and **S5** (b). Insets are enlarged patterns indicating two main reflections.

The analysis of the intra-crystalline disorder (paracrystalline disorder) has been performed for FBT-Th₄(1,4) 4-7 layers on the basis of the *100* peak from GIWAXS patterns (Figure 3.20). The paracrystalline disorder can be calculated by using the following equation:

$$g = \sqrt{\frac{\Delta_q}{2\pi q_o}}$$

where q_o and Δ_q are the center position and breadth of the only diffraction peak respectively.^[30] The paracrystalline disorder is $g = 3.50\%$ for sample on **S1** and $g = 4.45\%$ for sample on **S5**. These values are between 2-5 % confirming a small amount of disorder. More importantly, the paracrystalline disorder is identical for both surface roughnesses, indicating that the out-of-plane molecular organization in polymer film remains principally unchanged with increasing dielectric surface roughness. Combining the GIWAXS and AFM results, it is concluded that only the interfacial layers near the dielectric are markedly disrupted by the sub-nanometer R_{ms} , while the subsequent layers possess the same high polymer order.

The surface roughness variation within sub-nanometer range allows precise control of the interfacial microstructure of the semiconducting layer. This approach paves the way to investigate the intrinsic role of the first layers on the charge carrier transport in the case of solution-processed thicker films. To evaluate the charge carrier transport of dip-coated layers, OFET devices are fabricated with bottom-gate top-contact configuration. Au charge-injecting and -extracting source and drain electrodes are evaporated vertically to the dip-coating direction so that the current is measured along the processing direction. Herein, the electrical measurements of the organic transistors are performed in the saturation regime on the basis of the following careful considerations. Firstly, the investigated semiconducting layers are quite thin (less than 20 nm). By applying a high gate voltage of -80 V the charge carriers are tightly confined only in the first or first two layers adjacent to the dielectric even for films with 4-7 layers.^[31] Secondly, operation conditions close to $V_{GS}-V_T=V_{DS}$ lead the channel just to become “pinched”. Therefore, it is reasonable to assume that the conducting channel in the saturation regime for FBT-Th₄(1,4) 4-7 layers is also basically at or close to the interfacial layer (the first or first two layers) due to the high gate voltage. In other words, for FBT-Th₄(1,4) 4-7 layers no significant differences in charge carrier transport between linear and saturation regimes should be expected.

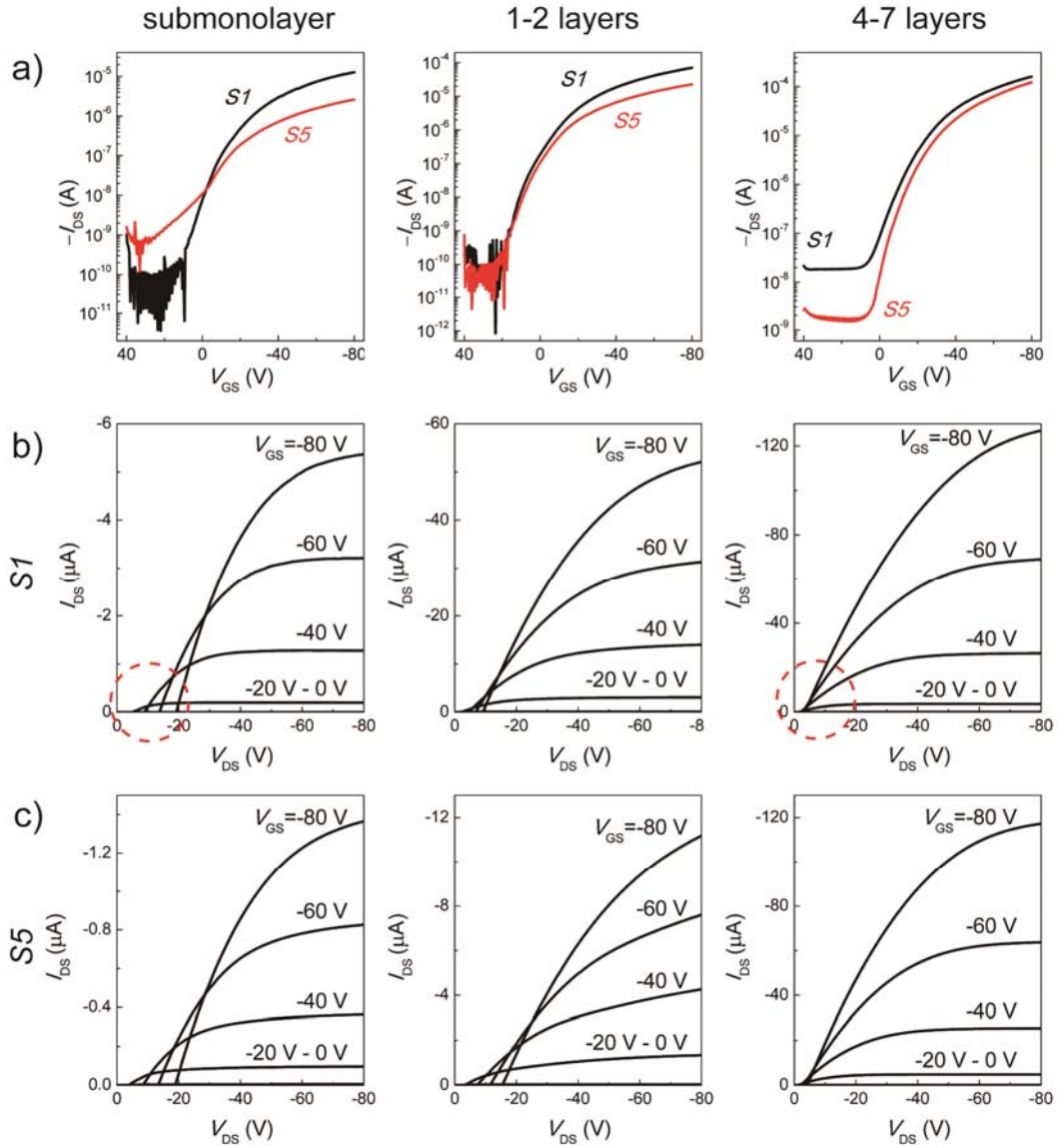


Figure 3.21 a) Transfer and b) output characteristics of various FBT-Th₄(1,4) layers deposited on S1 and S5. In a), $V_{DS} = -80$ V.

The transfer and output characteristics of various FBT-Th₄(1,4) layers are shown in Figure 3.21 indicating a typical linear/saturation behavior in all cases. The saturation field-effect mobility (μ) and other relevant FET parameters as a function of sub-nanometer roughness (S1-S5) are summarized in Table 3.2. FBT-Th₄(1,4) submonolayer is found to be sufficient to create a conducting channel for charge carriers, and its FET response characteristic is strongly dependent on dielectric roughness. The hole mobility of the submonolayer on S1 is extracted from transfer curve with the value of $0.030 \pm 0.004 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. In spite of the smaller fibers caused

by the higher R_{ms} , the submonolayer of FBT-Th₄(1,4) on **S5** can still ensure a charge carrier migration because of ordered regions which are efficiently interconnected by long polymer chains.^[30] The mobility drops by roughly one order of magnitude compared with **S1** ($\mu_h=0.005 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$). This noticeable decrease in transistor performance is also confirmed by transfer curves, where the drain current at the gate voltage (V_{GS}) of -80 V for the submonolayer on **S1** is ~10 times higher than that on **S5** (Figure 3.21a).

Table 3.2 Hole mobility (μ_h , $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$), on/off ratio (I_{on}/I_{off}) and threshold voltage (V_{th} , V) data for FBT-Th₄(1,4) layers dip-coated on **S1-S5**.

layers		S1	S2	S3	S4	S5
sub-mono	μ_h	$2.95\pm0.37\times10^{-2}$	$1.98\pm0.56\times10^{-2}$	$1.15\pm0.26\times10^{-2}$	$0.73\pm0.06\times10^{-2}$	$0.48\pm0.03\times10^{-2}$
	I_{on}/I_{off}	10^6	$10^4\sim10^6$	10^5	$10^4\sim10^6$	$10^4\sim10^5$
	V_{th}	-7~-5	-5~0	-3~-2	-7~0	-2~0
1-2	μ_h	$1.28\pm0.16\times10^{-1}$	$0.86\pm0.25\times10^{-1}$		$0.71\pm0.26\times10^{-1}$	$0.48\pm0.08\times10^{-1}$
	I_{on}/I_{off}	$10^6\sim10^7$	$10^5\sim10^7$		$10^5\sim10^7$	$10^5\sim10^6$
	V_{th}	-8~-1	-5~0		-2~6	-3~6
4-7	μ_h	$3.65\pm0.82\times10^{-1}$	$3.49\pm0.24\times10^{-1}$	$2.66\pm0.05\times10^{-1}$		$3.41\pm0.96\times10^{-1}$
	I_{on}/I_{off}	10^4	$10^4\sim10^6$	10^6		$10^5\sim10^6$
	V_{th}	-10~-3	-14~-4	-10~-5		-12~-5

In comparison to the submonolayer, 1-2 layers show an improved hole transport due to higher film coverage (75% for **S1** and 84% for **S5**) and the accumulation of more charge carriers from the second layer. The hysteresis effect of FBT-Th₄(1,4) 1-2 layers on **S1** and **S5** is shown in Figure 3.22. In transfer plots, the black curve represents the measurement from 20 to -80 V while the red curve indicates the measurement from -80 to 20 V. In output plots, black curve represents the measurement from 0 to -80 V while red curve indicates the measurement from -80 to 0 V. The device on **S1** exhibits a very small hysteresis with the threshold voltage change (ΔV_{th}) of 1.3 V. The rough dielectric (**S5**) leads to a stronger hysteresis with $\Delta V_{th}=2.7 \text{ V}$ involving higher density of trapping sites. In addition, the difference in hole mobility is declining to less than 3 times (from 0.128 ± 0.016 for **S1** to

$0.048 \pm 0.008 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for **S5**) which corresponds to the drain current variation at $V_{\text{GS}} = -80 \text{ V}$ (Figure 3.21a and Table 3.2). For comparison, FBT- $\text{Th}_4(1,4)$ 4-7 layers are dip-coated on the bare wafer ($R_{\text{ms}} = 0.197 \pm 0.013 \text{ nm}$), and the resultant transistor exhibits an identical OFET performance confirming the trend of the study (Table 3.3).

Table 3.3 Transistor performance of FBT- $\text{Th}_4(1,4)$ 4-7 layers dip-coated on bare wafer under the same conditions as **S1-S5**.

dielectric	R_{ms} (nm)	U^a ($\mu\text{m/s}$)	μ_h ($\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$)	V_{th} (V)	$I_{\text{on}}/I_{\text{off}}$
S2	0.187 ± 0.011	50	0.35 ± 0.02	-14~-4	$10^4 \sim 10^6$
bare wafer	0.197 ± 0.013	50	0.43	-5	10^4

^a U is the dip-coating speed.

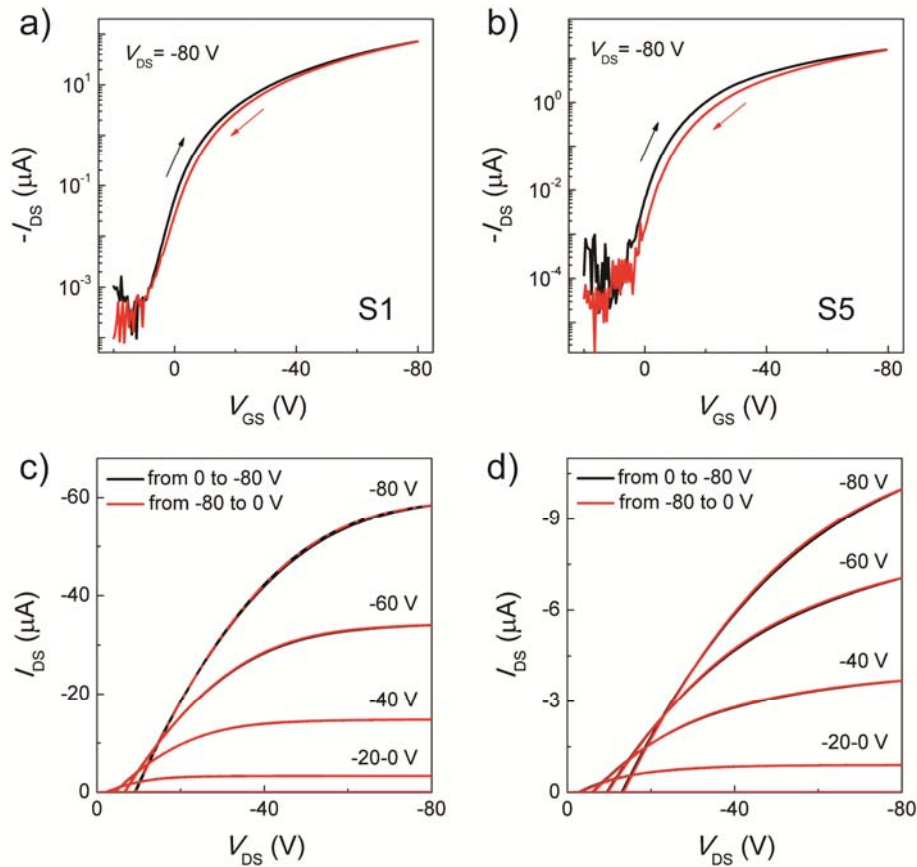


Figure 3.22 Hysteresis characterization for FBT- $\text{Th}_4(1,4)$ 1-2 layers on **S1** (a, c) and **S5** (b, d). The V_{GS} step in the transfer curve and V_{DS} step in the output curve are -0.5 V, and the sweeping rates are 0.4, 0.2, 0.1 and 0.1 V/s for a-d).

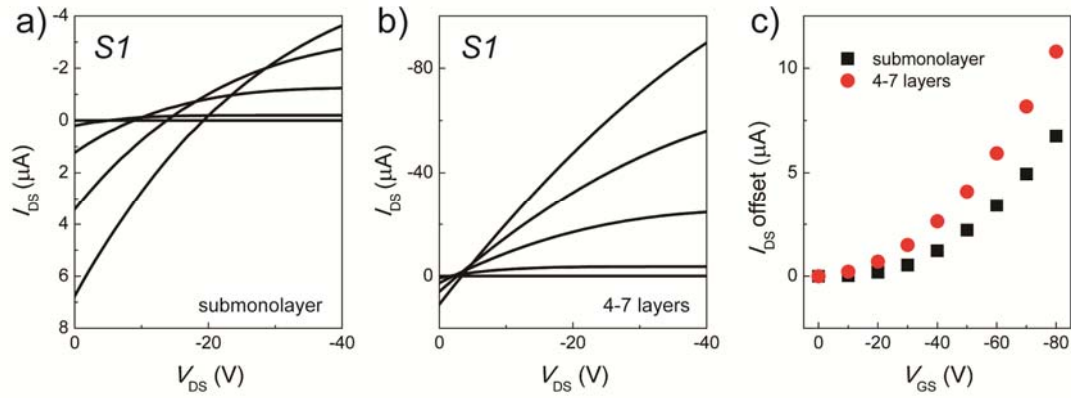


Figure 3.23 a,b) Enlarged range from Figure 3.21 of the output characteristics for FBT-Th₄(1,4) films on **S1** at low V_{DS} . c) I_{DS} offset as a function of V_{GS} .

Figure 3.21 b,c exhibits the output characteristics of FBT-Th₄(1,4) transistors. It is observed that at low V_{DS} the drain currents do not intersect with each other and show an obvious I_{DS} offset (Figure 3.23 a,b). I_{DS} offset is defined as the drain current with different gate voltage at $V_{DS} = 0$ V, which is a typical gate-induced leakage current effect.^[32] This undesirable feature originates from the expansion of the source and drain electrodes by the semiconductor accumulation layer. An efficient strategy for improving such an effect is spatially confining the organic semiconductor materials in the intended channel region, such as the patterning semiconducting layer, which has been proven by several groups separately.^[32-34] However, sometimes the leakage cannot be completely eliminated.^[35] The I_{DS} offset of 4-7 layers is higher than that of submonolayer independent on V_{GS} confirming the origin of the gate leakage.^[32] Additionally, it seems that the output characteristic of 4-7 layers is significantly improved compared to the submonolayer (Figures 3.23 a,b). This can be attributed to much higher drain current for the 4-7 layers.

During OFET measurement, a relatively high gate current is observed. In order to elucidate the influence of gate current on the extraction of mobility value, an attempt to suppress the gate leakage is made by removing the FBT-Th₄(1,4) which is in contact with the gate electrode at the sample edge using a chloroform-soaked cotton swab, as shown in Figure 3.24a. OFET performances of two samples (submonolayer on **S1**, 1-2 layers on **S1**) are evaluated before and after cleaning the

gate-contacting semiconductor, and a decrease in gate current is observed after cleaning (Figure 3.24 b,c). In particular, the gate current of FBT- $\text{Th}_4(1,4)$ 1-2 layers dramatically decreases by one order of magnitude after cleaning. At the same time, the drain current remains unchanged after posttreatment for both samples. Table 3.4 summarizes the gate leakage and OFET performances before and after cleaning. It is found that the hole mobility (μ_h), threshold voltage (V_T) and on/off ratio ($I_{\text{on}}/I_{\text{off}}$) remain almost unchanged for both samples. For all transistors in this chapter, the drain current is always at least one order of magnitude higher than the gate leakage. Therefore, it is reasonable that such relatively low gate current does not influence the drain current. These results demonstrate that the influence of gate leakage on the extracted parameters is negligible in this chapter.

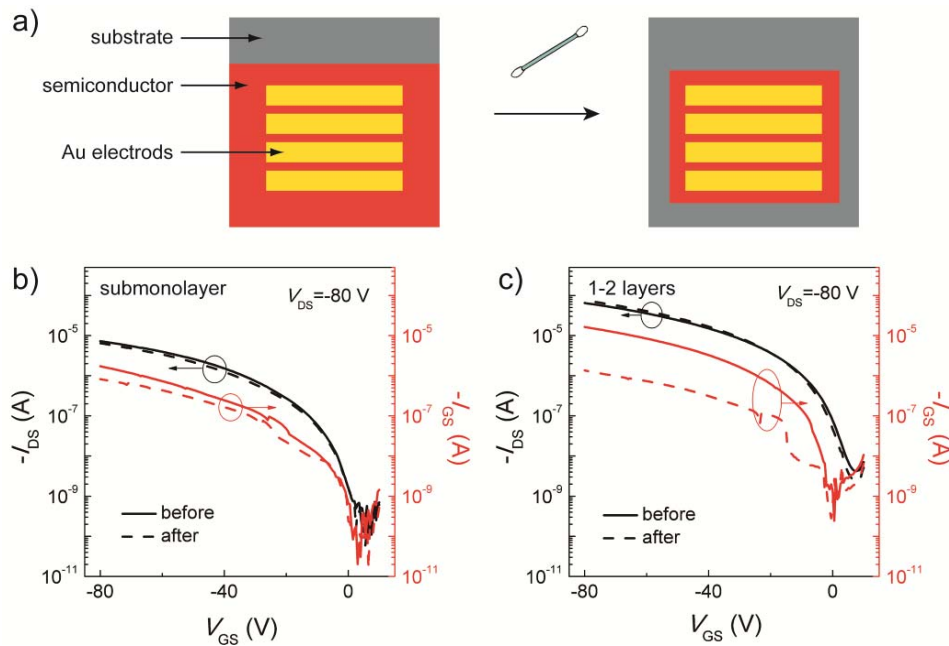
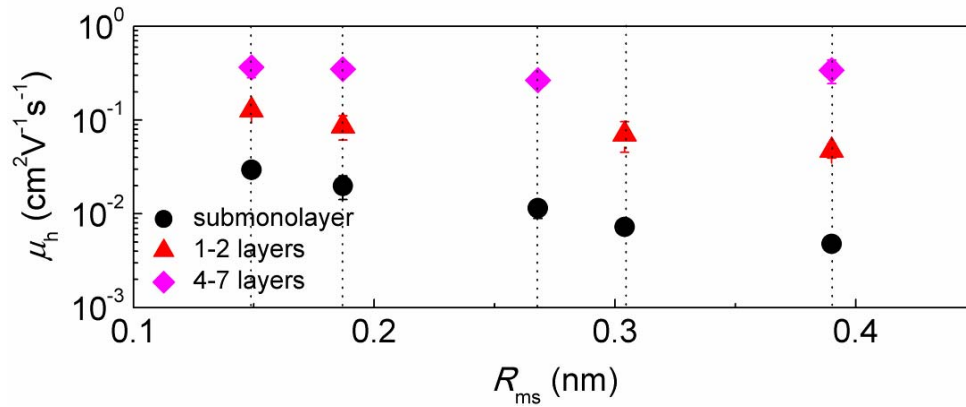


Figure 3.24 a) Schematic illustration of cleaning the perimeter of the semiconducting layer for suppression gate leakage. Transfer characteristics of FBT- $\text{Th}_4(1,4)$ submonolayer (b) and 1-2 layers (c) before and after cleaning. The solid and dash lines represent the drain currents before and after cleaning, respectively. A source-drain voltage of -80 V is applied.

Table 3.4 Gate leakage and OFET performance of FBT-Th₄(1,4) submonolayer and 1-2 layers before and after swabbing the perimeter of the semiconducting film.

sample	cleaning	$-I_{GS}$ (A)	μ_h (cm ² V ⁻¹ s ⁻¹)	V_{th} (V)	I_{on}/I_{off}
submono	before	1.72×10^{-6}	0.016	-7	10^4
	after	8.17×10^{-7}	0.015	-8	10^4
2-3	before	1.64×10^{-5}	0.12	-1	10^4
	after	1.35×10^{-6}	0.14	-2	10^4

There are mainly three reasons for the decline in field-effect mobility in the cases of submono- and 1-2 layers. Firstly, the fiber dimension is dramatically reduced by the higher dielectric roughness, which not only induces more structural defects but also restricts the migration of charge carriers (Figure 3.16, 3.17 and 3.21). Secondly, the rough surface increases the density of trapping sites, as indicated by a slightly larger hysteresis for the FBT-Th₄(1,4) 1-2 layers on **S5** (Figure 3.24).^[36] Finally, the charge carrier transport is hindered by surface scattering effects caused by the surface roughness.^[37]

**Figure 3.25** Hole mobility of FBT-Th₄(1,4) thin films with different thicknesses as a function of dielectric roughness.

In comparison to the monolayer, FBT-Th₄(1,4) 4-7 layers provide more pathways for charge carrier transport exhibiting the maximum hole mobility of 0.51 cm² V⁻¹ s⁻¹. It is interesting that the field-effect mobility of FBT-Th₄(1,4) 4-7 layers is independent on the dielectric roughness although the self-assembly of interfacial layer is

significantly hindered by higher R_{ms} , as shown in Figure 3.25. These results convincingly demonstrate that the interfacial microstructure of conjugated polymers has no influence on charge carrier transport in multilayer transistors.

In Figure 3.25, it is obvious that there is a missing point (**S4**, $R_{ms}=0.30$ nm) for FBT-Th₄(1,4) 4-7 layers, because the polymer ($M_n=23$ K, the “old” batch) was run out due to the intensive studies and the need of good statistics (which means many measurements). Therefore, another batch was synthesized following the same procedure. However, the molecular weight of “new” batch is slightly increased to $M_n=28$ K. The 4-7 layers of this batch were deposited on **S3** and **S4** by dip-coating from 0.5 mg/mL chloroform solution. The 4-7 layers of the “new” batch ($M_n=28$ K) on **S3** exhibit an identical charge carrier transport to the “old” one ($M_n=23$ K). More importantly, the mobility of the “new” batch ($M_n=28$ K) on **S4** is $0.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Therefore, these results provide further evidence that the interfacial microstructure has no impact on the charge carrier transport in multilayers, but they are not plotted into Figure 3.25 due to the difference in molecular weight.

3.3.2 Amorphous Conjugated Polymer

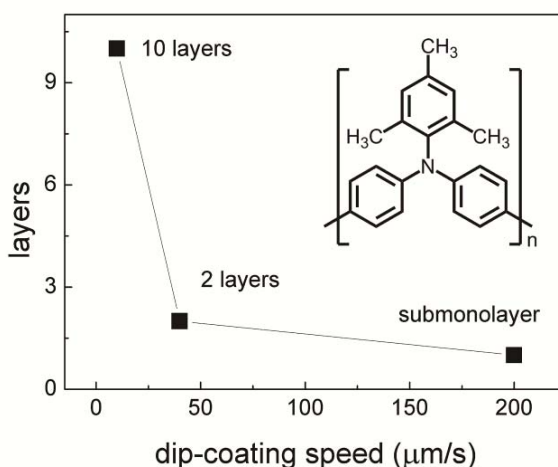


Figure 3.26 Thickness of deposited poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine] (PTAA) thin films as a function of dip-coating speed. Chloroform is used as solvent, and PTAA concentration is 1 mg/mL. The inset is the chemical structure of PTAA.

In order to elucidate the effect of dielectric roughness alone and further verify the above conclusion, a control sample, poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine] (PTAA, Figure 3.26) that is a truly amorphous conjugated polymer, is investigated. In spite of its amorphous nature, PTAA thin films were reported to exhibit the field-effect mobility of 10^{-3} - 10^{-2} $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$.^[38] PTAA used here was purchased from Sigma with $M_n=7000$ - 10000 . Similar to FBT-Th₄(1,4), dip-coating can control the film thickness of PTAA in a monolayer precision, as shown in Figure 3.26. A single molecular layer of PTAA with the thickness of ~ 4 nm is deposited by dip-coating from 1 mg/mL chloroform solution at 200 $\mu\text{m/s}$. A lower dip-coating speed induces the deposition of more layers. At 20 $\mu\text{m/s}$, the layer number of dip-coated thin films can reach 10.

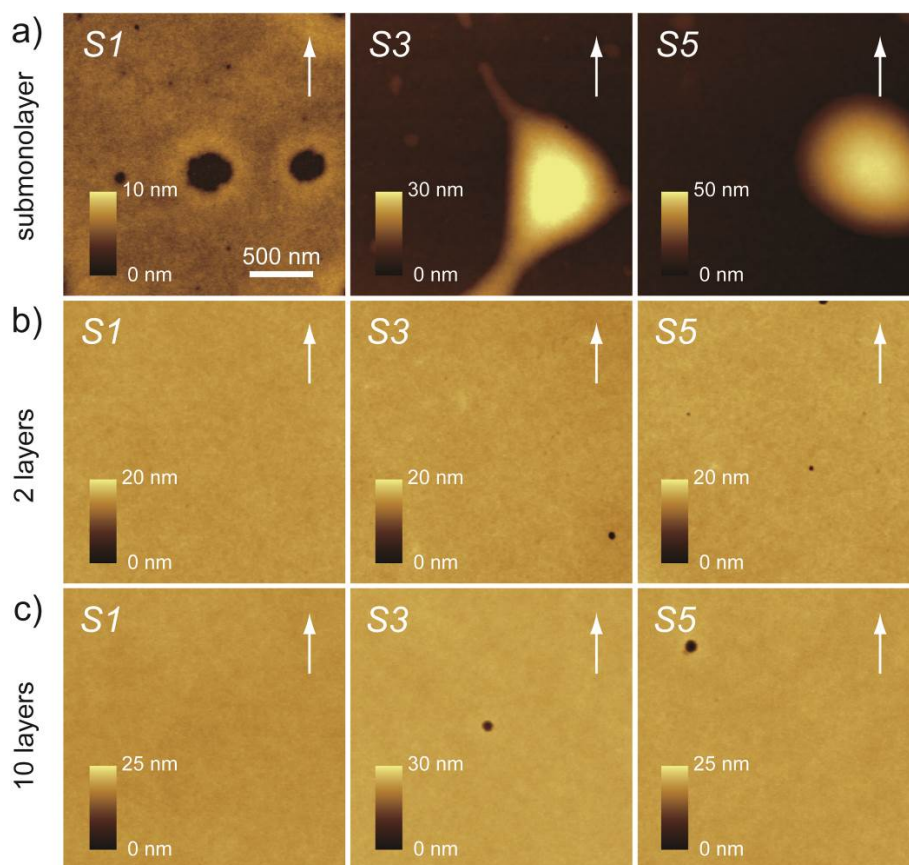


Figure 3.27 AFM images of PTAA thin films on **S1-S5** with different thicknesses. Dip-coating is used for film deposition with the speeds of 200, 40 and 10 $\mu\text{m/s}$ for a-c, respectively. All images have the same scale bar. The white arrows indicate the dip-coating direction.

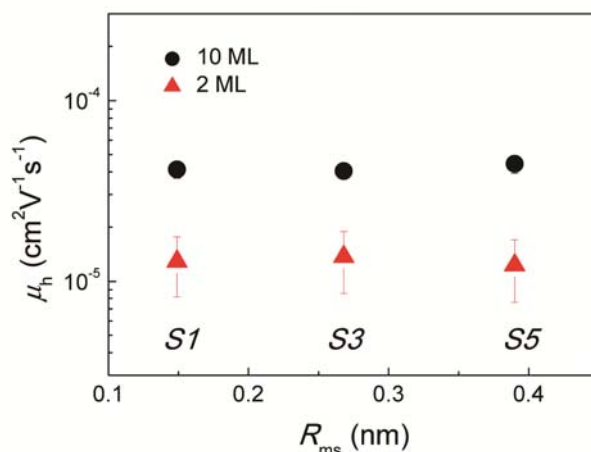


Figure 3.28 Relation between hole mobility and dielectric roughness for PTAA thin films with different thickness.

The morphology of PTAA thin films from mono- to multilayers is characterized by AFM in tapping mode. The dielectric roughness is found to affect the microstructure of PTAA submonolayer. On the flat surface such as **S1** a homogenous film-like monolayer is deposited, while on the rough surface (**S3** and **S5**) an inhomogenous film is obtained consisting of micro-sized aggregates (Figure 3.27a). It must be emphasized that both monolayer and aggregates are composed of identical irregular nanoscale granules due to the amorphous nature of PTAA. On the contrary, this difference in microstructure caused by dielectric roughness vanishes with increasing film thickness. It can be clearly seen from Figures 3.27b and c that the topography of PTAA multilayers is identical to each other, independent of the dielectric roughness. Furthermore, the effect of dielectric roughness on the charge carrier transport is also investigated for PTAA thin films with different thicknesses. Due to the discontinuous layers for submonolayers on the rough surfaces **S3** and **S5**, the transistor performance is measured starting from 2 molecular layers. As expected, the hole mobilities scarcely depend on the R_{ms} value in both cases of PTAA 2 and 10 layers (Figure 3.28). This is reasonable since PTAA as an amorphous polymer exhibits a roughness-independent microstructure which is believed to dominate the charge carrier transport. The hole mobility value of $\sim 4 \times 10^{-5} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for PTAA 10

layers is much lower than the previous report.^[38] This is related to a large degree of energetic disorder and a high trap density on bare SiO₂ surface.^[39-40]

In comparison to semicrystalline FBT-Th₄(1,4) that can be tuned from ordered to disordered microstructure only at the interfacial layer, the molecular ordering of amorphous PTAA is independent of the dielectric roughness, especially for the interfacial layer adjacent to the dielectric. However, the corresponding electrical characterizations indicate that the charge carrier transport in PTAA follows the similar trend to FBT-Th₄(1,4). Therefore, these results can be seen as additional evidence to support the conclusion in section 3.3.1: interfacial microstructure has a negligible effect on charge carrier transport for conjugated polymers independent of the crystallinity.

3.3.3 Crystalline Cyano Substituted Perylenediimide

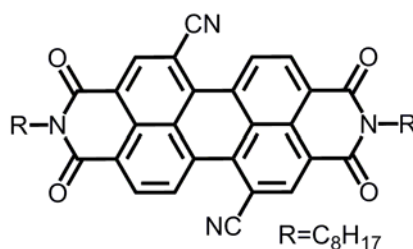


Figure 3.29 Chemical structure of N,N'-bis(n-ctyl)-x:y,dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI₈-CN₂).

The long polymer chains of conjugated polymers have the capability of creating sufficient pathways for charge carriers even though the microstructures are highly disordered.^[24] In this case, the decrease in transistor performance caused by a disordered microstructure could be compensated by the long polymer chains, and the relationship between microstructure and charge carrier transport is not straightforward enough, which critically affects the evaluation of the intrinsic role of interfacial microstructure. To make an unambiguous conclusion in this chapter, a small molecule, N,N'-bis(n-ctyl)-x:y,dicyanoperylene-3,4:9,10- bis(dicarboximide) (PDI₈-CN₂, Figure

3.29) is studied. There are two other reasons for the choice of this cyano substituted perylenediimide. On the one hand, the crystallinity of PDI₈-CN₂ is significantly higher than the polymers so that a different microstructure formation can be obtained. On the other hand, PDI₈-CN₂ favors mainly the electron conduction in contrast to the hole transporting FBT-Th₄(1,4) and PTAA. In addition, this small molecule holds great promise for practical applications because of the unique combination of high-yield and scalable synthesis, chemical stability, satisfying field-effect mobility, and solution processibility.

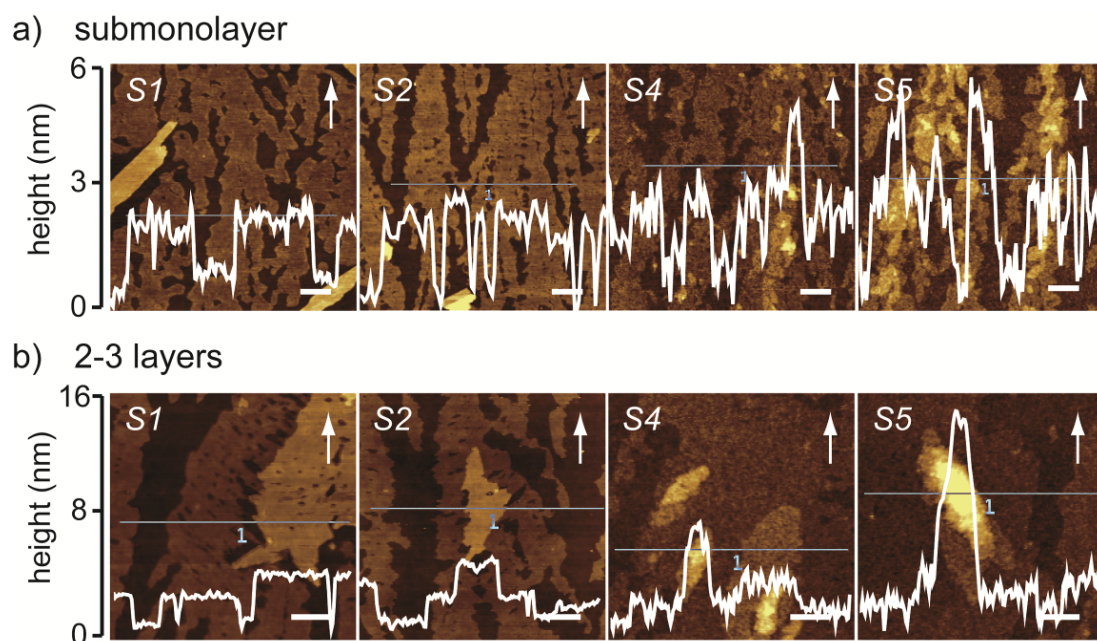


Figure 3.30 AFM images of PDI₈-CN₂ submonolayer and 2-3 layers dip-coated on dielectrics **S1-S5**. The height tick labels on the left side of the AFM images are related to the height plots (white) in AFM images. The scale bars in AFM images correspond to 500 nm. The dip-coating speeds are 100 and 50 $\mu\text{m/s}$ for submonolayer and 2-3 layers, respectively. The white arrows indicate the dip-coating direction.

PDI₈-CN₂ thin films are processed by dip-coating from 0.5 mg/mL chloroform solution onto **S1-S5**. A submonolayer with ~ 2 nm in thickness is deposited at the dip-coating speed of 100 $\mu\text{m/s}$. Compared with FBT-Th₄(1,4), the PDI₈-CN₂ domains seem to be extended to a certain extent in the dip-coating direction. Figure 3.30a

shows the effect of dielectric roughness on the self-assembly of PDI₈-CN₂ submonolayer. The flat surfaces with $R_{\text{ms}} < 0.2$ nm (**S1** and **S2**) induce large crystal domains on a micrometer scale. However, the domain size of crystalline submonolayer is reduced starting from $R_{\text{ms}} = 0.268 \pm 0.031$ nm (**S3**). In the meantime, the aggregation in the formation of nanoparticles appears. On **S4** and **S5**, the surface of dip-coated submonolayer becomes almost as rough as the dielectric, and the size of the aggregates remarkably increases corresponding to the film roughness of PDI₈-CN₂ submonolayer (Figure 3.31). It must be emphasized that the film coverage of the monolayer remains almost independent of dielectric roughness. Therefore, these results demonstrate that a rough dielectric not only increases the density of nucleation on the surface but also inhibits film growth into large domains.^[11]

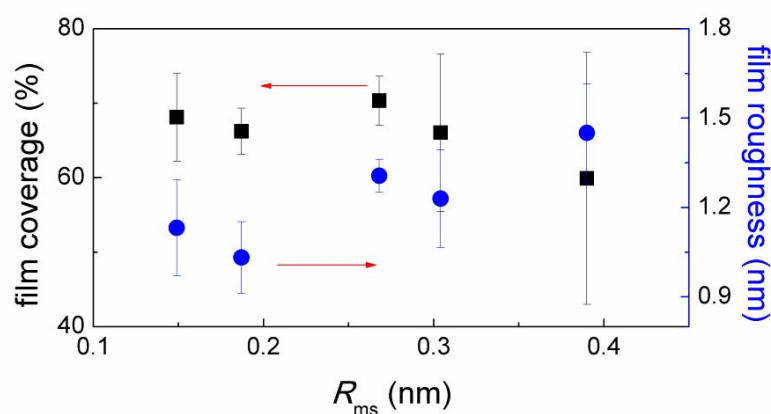


Figure 3.31 Film coverage and roughness of PDI₈-CN₂ submonolayer deposited on **S1-S5**. The broad coverage error bars results from a large distribution in coverage. During AFM measurement, we randomly selected several areas for scanning.

To gain information on the molecular order, the PDI₈-CN₂ submonolayer is characterized by TEM and selected-area electron diffraction (SAED). TEM bright-field images in Figure 3.32 show a highly ordered monolayer on **S1**, and a less ordered aggregate on **S5** consist of several layers with much smaller domains, which confirms the existence of detrimental effect of a dielectric roughness on the monolayer molecular organization. The corresponding SAED patterns also exhibit a significant difference in domain size and molecular crystallinity between

submonolayers on **S1** and **S5** (Figure 3.32c,d). The submonolayer on **S1** exhibits distinct strong intensity spots indicating high crystallinity and pronounced order within the investigated area. It has to be emphasized that the spot-like diffraction pattern is characteristic for domains which are larger than the diffracted area. The analysis of the pattern exposes almost the same unit cell parameters ($b=0.483$ nm and $c=1.699$ nm) as reported in the literature.^[41] Moreover, these data indicate that on **S1** the PDI₈-CN₂ molecules are organized in an edge-on fashion, which is favorable for the charge carrier transport because of its coincidence with the π -stacking direction. On the contrary, the isotropic scattering intensities in the SAED pattern of submonolayer on **S5** reveal a polycrystalline structure as well as the presence of several domains in the diffracted area. Due to the same diffracted area for both **S1** and **S5**, it is suggested that the domain size is noticeably reduced with increasing R_{ms} , which is in a good agreement with AFM characterization.

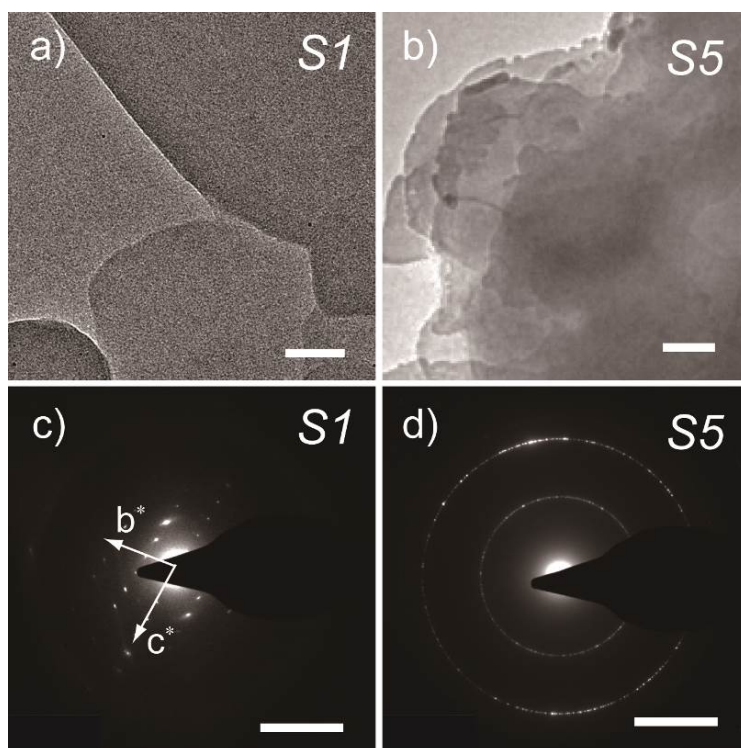


Figure 3.32 TEM bright-field images of PDI₈-CN₂ submonolayer deposited on **S1** (a) and **S5** (b). c-d) Corresponding electron diffraction patterns of a-b). The size of the diffracted area are the same for c) and d). The scale bars are 100 nm and 5 nm⁻¹ for TEM and electron diffraction, respectively.

Compared to FBT-Th₄(1,4), the charge carrier transport of PDI₈-CN₂ submonolayer is dependent on the dielectric roughness to a higher extent. At first, the charge carrier transport of macromolecules is less sensitive to the microstructure, grain boundaries and crystallinity than small molecules.^[29, 42-43] It was reported that a few conjugated polymers with macroscopically poor ordering exhibited good charge carrier transport with the mobility above $0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[29, 44-46] On the other hand, the larger molecular dimension of polymers enables bridging of disordered regions - in this way the boundary density is decreased, in comparison to highly crystalline small molecules.^[24] Figure 3.33 and Table 3.5 summarize the OFET performance of PDI₈-CN₂ submonolayer as a function of R_{ms} . It is found that the average mobility is reduced from $3.00 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at $R_{\text{ms}} = 0.149 \pm 0.006 \text{ nm}$ (**S1**) to $7.54 \times 10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at $R_{\text{ms}} = 0.187 \pm 0.011 \text{ nm}$ (**S2**). Compared to this slight decrease, $R_{\text{ms}} = 0.268 \pm 0.031 \text{ nm}$ (**S3**) seems a critical value for the electron transport, at which the electron mobility of PDI₈-CN₂ submonolayer is dramatically reduced by more than 20 times. Afterwards, the rougher surfaces (**S4** and **S5**) impair the electron transport, resulting in a mobility of around $10^{-5} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. The origin of such a significant mobility drop can be seen in: firstly, a larger number of nucleation sites induced by high R_{ms} inhibit the domain growth and thus create more grain boundaries,^[4, 7] so that the pathway of charge carriers is severely disrupted.^[47] Secondly, at semiconductor/dielectric interface, the increased trapping states and surface scattering effect are also the possible reasons for low electron mobility.^[37]

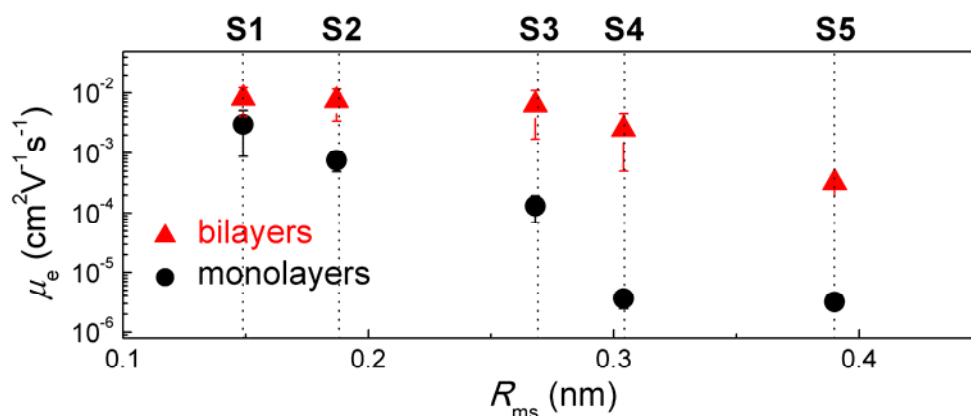


Figure 3.33 The relation between charge carrier transport and dielectric roughness.

Table 3.5 Electron mobility (μ_e , $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$), on/off ratio ($I_{\text{on}}/I_{\text{off}}$) and threshold voltage (V_{th} , V) data for PDI₈-CN₂ submonolayer and 2-3 layers dip-coated on **S1-S5**.

layers		S1	S2	S3	S4	S5
sub-mono	μ_e	$3.00 \pm 2.12 \times 10^{-3}$	$7.54 \pm 2.64 \times 10^{-4}$	$1.32 \pm 0.63 \times 10^{-4}$	$3.63 \pm 1.19 \times 10^{-6}$	$3.17 \times 10^{-6}^{\text{a}}$
	$I_{\text{on}}/I_{\text{off}}$	$10^2 \sim 10^3$	10	10	10	$10 \sim 10^2^{\text{a}}$
	V_{th}	-50 ~ -5	-80 ~ -50	-80 ~ -20	-70 ~ -30	-20 ^a
2-3	μ_e	$8.12 \pm 4.05 \times 10^{-3}$	$7.49 \pm 4.08 \times 10^{-3}$	$6.33 \pm 4.61 \times 10^{-3}$	$2.50 \pm 2.00 \times 10^{-3}$	$3.21 \pm 0.49 \times 10^{-4}$
	$I_{\text{on}}/I_{\text{off}}$	10^3	10^3	10^2	$10 \sim 10^3$	$10^2 \sim 10^3$
	V_{th}	-10 ~ -5	-20 ~ -5	-30 ~ -8	-40 ~ -15	-25 ~ -10

^aOnly one working device out of 20 transistors.

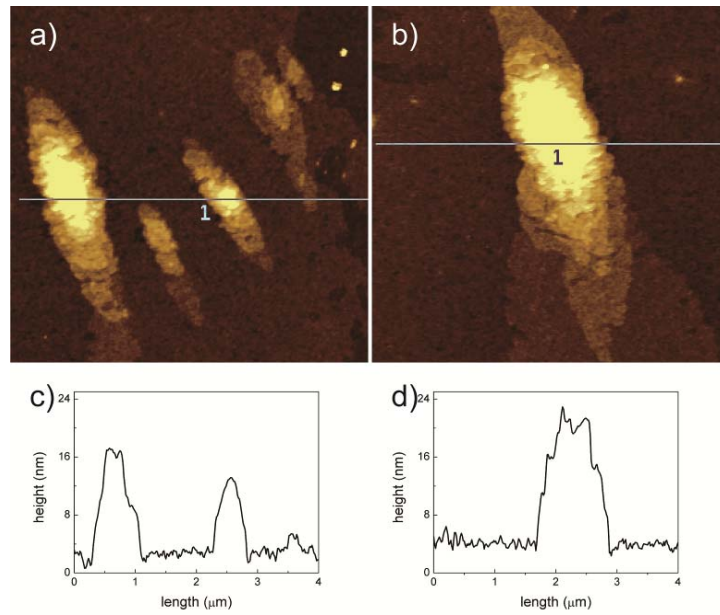


Figure 3.34 AFM images ($4 \mu\text{m} \times 4 \mu\text{m}$) and corresponding height plots of PDI₈-CN₂ 2-3 layer deposited on **S4** (a,c) and **S5** (b,d).

The lower dip-coating speed of $50 \mu\text{m/s}$ allows deposition of 2-3 layers. The height plots of the corresponding AFM images in Figure 3.30b reveal that the thickness of dip-coated film is 2-4 nm, confirming growth of a second layer on **S1** and **S2**. On the other hand, the low pulling speed efficiently enhances the film coverage and domain size on **S4**. It has to be noted that a higher R_{ms} causes the increase in film roughness as well as the formation of 15-nm-thick aggregates (Figures 3.30b and 3.34). On **S5**, the aggregation behavior is more obvious with the particle size of >20 nm in thickness and $>3 \mu\text{m}$ in length. Compared with the submonolayer, the transistor performance of PDI₈-CN₂ 2-3 layer is less dependent on the dielectric roughness. At

$R_{\text{ms}}=0.149\pm0.006$ nm (**S1**), a maximum electron mobility of 1.28×10^{-2} $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ is obtained (Table 3.5), which is in the same range as previous reports for solution-processed PDI₈-CN₂.^[41, 48-49] When the dielectric roughness decreases to 0.304 ± 0.022 nm (**S4**), the average mobility only slightly declines from 8.12×10^{-3} $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ to 2.50×10^{-3} $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. Even for the highest R_{ms} (**S5**), the decrease in electron mobility is only approximately one order of magnitude and less drastic than observed for the submonolayer ($\sim10^3$). Compared with literature, in which the entire film microstructure of crystalline small molecules such as pentacene was critically affected by the dielectric roughness on a nanometer scale,^[4-6] the interfacial microstructure of PDI₈-CN₂ is well controlled in a higher precision. More importantly, these results provide additional evidence that the interfacial microstructure has no impact on charge carrier transport in multilayers, independent of the chemical structure and film microstructure of organic semiconductors, and nature of charge carriers.

3.4 Proposed Mechanism for Charge Carrier Transport

It is concluded in this chapter that the microstructure at the semiconductor/dielectric interface has a minor impact on the charge carrier transport in solution-processed field-effect transistors. This finding seems contradictory to the common knowledge, but it is convincingly proven by using a semicrystalline FBT-Th₄(1,4), an amorphous PTAA and a crystalline PDI₈-CN₂. All of these achievements can be attributed to the fabrication of dielectrics with surface roughness on a sub-nanometer scale that allows the precise modulation of only interfacial microstructure. The mechanism for charge carrier transport at the interfacial layer is proposed, as shown in Figure 3.35. In the case of a monolayer, the higher surface roughness reduces the domain size within the entire film. As the only possible pathway for the migration of charge carriers, this poorly ordered monolayer yields low transistor performance (Figure 3.35a). In the case of multilayers, the applied gate voltage theoretically leads to the accumulation of charge carriers within mainly the

first few monolayers at semiconductor/dielectric interface,^[31, 50] although a broader distribution up to four or five layers was reported due to the three-dimensional charge carrier transport.^[51-52] It is worth pointing out that the sub-nm dielectric developed in this chapter, for the first time, allows the fine modulation of spatial molecular microstructure. Different from previous reports,^[4-7] the molecular organization of the next layers is gradually self-recovered with larger domain dimensions as the influence of the sub-nanometer R_{ms} decreases. Consequently, in this scenario the charge carriers have the possibility of by-passing structure defects at the interface so that the transport is mainly determined by the highly ordered layers on top of the interfacial monolayer with small domains, as illustrated in Figure 3.35. In this case, the contribution of the interfacial layer is negligible. This chapter, for the first time, precisely modulates spatial molecular microstructure and provides direct evidence for the minor impact of interfacial microstructure of organic semiconductors.

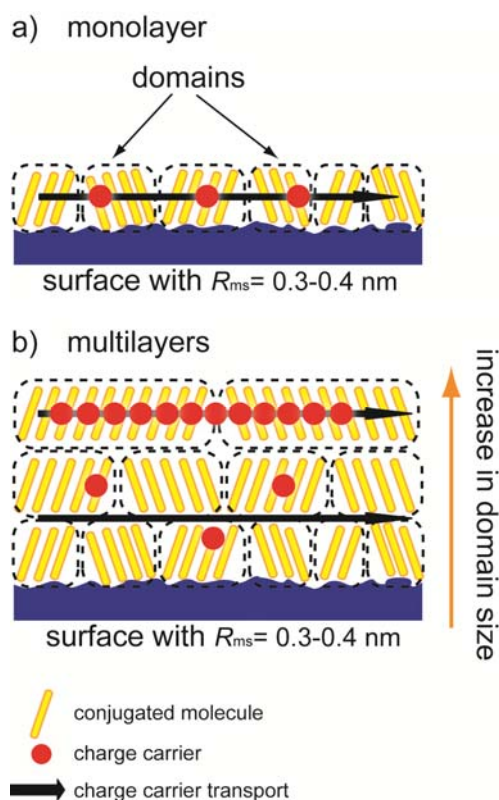


Figure 3.35 Scheme proposed as explanation for the impact of interfacial microstructure on charge carrier transport. Conjugated molecules are deposited into monolayer (a) and multilayers (b).

3.5 Conclusion

In this chapter, dielectrics with surface roughness in an extremely narrow range from 0.15 to 0.39 nm are prepared in order to investigate the impact of the interfacial microstructure on the charge carrier transport. A sub-nanometer roughness is found to allow a kinetic control of molecular microstructure of polymer monolayer (PCPDTBT) from nanofibers to nanoaggregates, and the hindrance of self-assembly induced by dielectric roughness leads to lower transistor performance. In order to comprehensively investigate the impact of interfacial microstructure on charge carrier transport, three different types of organic semiconductors including including a semicrystalline polymer (FBT-Th₄(1,4)), an amorphous polymer (PTAA) and a highly crystalline small molecule (PDI₈-CN₂) are studied by using dielectrics with sub-nm surface roughness. In the case of monolayer, the microstructure and domain size is highly dependent on the dielectric roughness. A higher R_{ms} generally reduces the domain size leading to poor OFET performance. Interestingly, the influence of the dielectric roughness on a sub-nm scale is only confined to the interfacial layer without affecting the upper layers, which is confirmed by both AFM and GIWAXS. More importantly, electrical measurements demonstrate that organic semiconductor multilayers exhibit identical charge carrier transport independent of dielectric roughness indicating that the interfacial microstructure only has a minor impact on the charge carrier transport in organic transistors for ordered multilayers. In contrast to this behavior, purely amorphous PTAA does not reveal even for bilayers any effect of the roughness on the microstructure and thus charge carrier transport. It is assumed that when the interfacial layer possesses a disordered microstructure, the charge carrier transport takes place in the upper layers with ordered microstructure compensating the current between source and drain electrodes.

It seems that our observations are opposed to the common knowledge that the first few monolayers adjacent to the dielectric dominate the charge carrier transport.^[53-54] However, it is worth noting that this common knowledge was mainly

concluded from small molecules by organic molecular beam deposition that unavoidably caused spatial inhomogeneity in thin films. For instance, it was revealed that the second monolayer showed a lower lateral coherence length than the first monolayer.^[8] Another general feature was the dynamic transition from layer-by-layer growth to rapid roughening with increasing film thickness severely hindering the self-organization of top layers as well as their charge carrier transport.^[55-56] In other words, the molecular organization of semiconducting layer at the dielectric interface is often better than that of upper layers. In such a case, there is no doubt that the transistor performance will be obviously decreased if the interfacial microstructure becomes disordered, because it is almost unlikely for charge carriers to jump into and move in the disordered upper layers. This could mislead the understanding on the intrinsic role of the interfacial microstructure. On the contrary, in this chapter, the precise control of only the interfacial microstructure, without affecting subsequent layers, is realized for the first time, which gives an additional insight into the mechanism of the charge carrier transport at the interfacial layer.

Interface engineering is a novel approach towards high-performance OFETs.^[57] In this chapter, the intrinsic role of interfacial microstructure is revealed, which not only allows a further understanding of charge carrier transport, but also has a practical significance in organic electronics. For example, the flexible substrates such as poly(ethylene terephthalate) (PET) can be rationally modified, so that the resultant surface roughness is within a sub-nm range. Despite of the decrease in interfacial microstructure, the performance of the whole transistor remains unchanged. More importantly, the cohesion/adhesion between the organic semiconductor and dielectric can be effectively enhanced holding a great potential in high-stability devices.^[58] Besides the semiconductor/dielectric interface, the interface between semiconductor and source/drain electrodes is also of vital importance. In a bottom-contact transistor, the film microstructure on the dielectric is usually different from that on the electrodes, inducing considerable contact resistance. To solve this contact problem, most studies are focusing on the surface modification of electrodes by self-assembled monolayers (SAMs),^[59-60] but little attention has been paid to the surface roughness of

electrodes, which can be another powerful tool to fabricate high-performance OFET devices. Therefore, I will put my future focus on the effect of electrode roughness on both contact resistance and transistor performance.

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Chapter 4

Interfacial Microstructure of Sublimed Small Molecule Semiconductor

4.1 Introduction

In chapter 3, organic semiconductors including a highly crystalline small molecule as well as semicrystalline and amorphous polymers are deposited by solution processing on the dielectrics with sub-nm surface roughness to study the intrinsic role of interfacial microstructure on the charge carrier transport. However, strong π -interactions between conjugated molecules generally exist so that aggregation in solution can take place before and during processing.^[1-3] This phenomenon could affect the conclusion in chapter 3. On the contrary, thermal sublimation in vacuum is able to avoid these external influencing factors, so that the impact of interfacial microstructure can be further investigated.

As well-known crystalline organic semiconductors with good charge carrier mobility and stability, oligothiophenes and their derivatives were able to form high-quality thin films with only a few single molecular layers, providing an excellent opportunity to explore the relation between film thickness and mobility in a monolayer precision.^[4-8] In this chapter, α,ω -dihexylsexithiophene (α,ω -DH6T, Figure 4.1) is deposited by thermal sublimation in vacuum from mono- to multilayers

on the dielectric of a controlled surface roughness within a sub-nanometer scale. This approach allows a closer inspection of the evolution of the microstructure and charge carrier transport. Compared with the monolayer, both microstructure and charge carrier transport of α,ω -DH6T multilayers are less dependent on the dielectric roughness. This chapter confirms that the conclusion drawn from chapter 3 bears a general significance which are not only applicable probably for most organic semiconductors but also independent on the deposition technique.

4.2 Sublimed α,ω -Dihexylsexithiophene Mono- and Multilayers

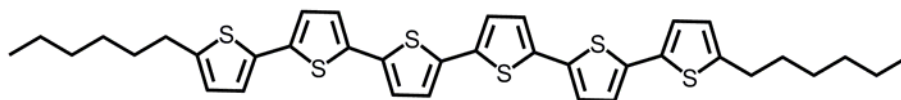


Figure 4.1 Chemical structure of α,ω -DH6T.

To date, extensive effort on organic molecular beam deposition (OMBD) studies has been made to understand the growth mechanisms during deposition for a large amount of molecules by using various substrates and different deposition parameters.^[9-12] However, these reports have not been correlated to the charge carrier transport in transistors. There are no studies focusing on the effect of the spatial inhomogeneity on the charge migration. The reason is that it is difficult to precisely control the molecular ordering or microstructure by OMBD only at the interface. Herein, α,ω -DH6T (Figure 4.1) thin films from monolayer to multilayers are deposited by thermal sublimation in vacuum, and their spatial inhomogeneity and corresponding charge carrier transport are investigated. α,ω -DH6T is chosen as the model compound due to its two key advantages. On the one hand, charge carriers can be shielded by the alkyl chains from the dielectric interface reducing the density of the trapping sites at the interface.^[5] On the other hand, the strength of intermolecular interactions between the conjugated cores can be enhanced by the alkyl chains promoting the crystallinity of the semiconducting layers.^[5]

Table 4.1 The root-mean-square surface roughness (R_{ms}) of the dielectric **S1-S5**.

dielectric	S1	S2	S3	S4	S5
R_{ms} (nm)	0.149±0.006	0.187±0.011	0.268±0.031	0.304±0.022	0.390±0.037

The surface roughness of the SiO_2 dielectric is accurately modulated as described in chapter 3. The surface roughness (R_{ms}) ranges from 0.15 to 0.39 nm (Table 4.1). The detailed characterizations of the surface properties of modified SiO_2 are in chapter 3 confirming that the only difference among **S1-S5** is the surface roughness.

In the first step, α,ω -DH6T ultrathin films with a single molecular layer (monolayer, ML) are fabricated. The microstructure is characterized by AFM in tapping mode, as shown in Figure 4.2. The monolayer coverage is $\sim 70\%$, defined as 0.7 ML. This monolayer consists of isolated disk-like grains, and the height profile exhibits a thickness of ~ 2.9 nm. This value is in agreement with the d-spacing of α,ω -DH6T films found by GIWAXS confirming a lamellar organization of the rod-like molecules.^[13]

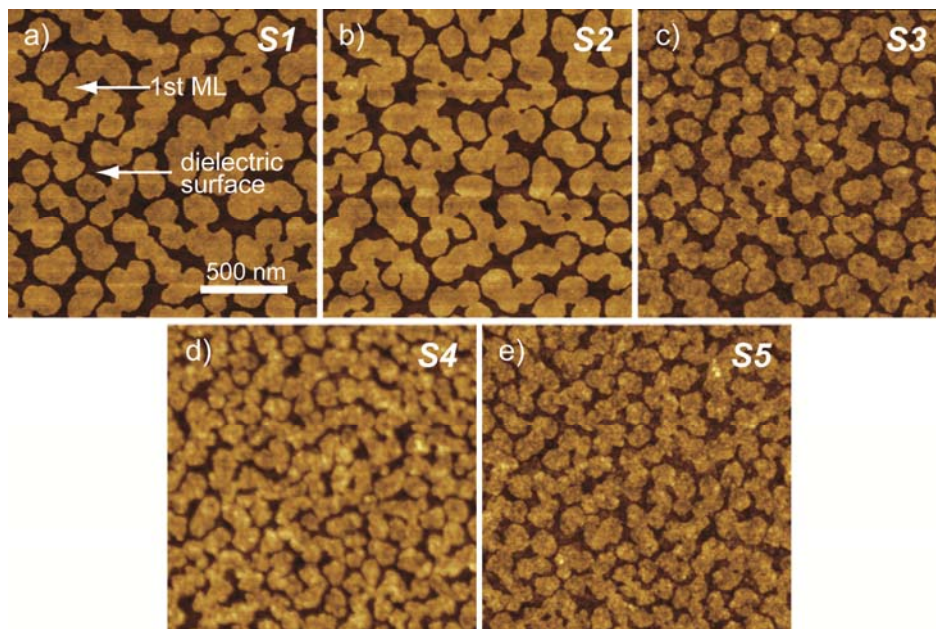


Figure 4.2 AFM images of α,ω -DH6T 0.7 ML on **S1-S5** by thermal sublimation in vacuum. All images have the same scale bar.

The dielectric roughness critically affects the microstructure of α,ω -DH6T 0.7

ML (Figure 4.2). The film roughness of the deposited 0.7 ML is gradually increased with R_{ms} due to the rougher dielectric surface and limited molecular self-assembly (Figure 4.3a). More importantly, it is obvious from Figure 4.3b that the grain size is strongly dependent on R_{ms} . With a slight increase in R_{ms} from 0.149 ± 0.006 nm (**S1**) to 0.187 ± 0.011 nm (**S2**), a reduction in grain size is clearly observed from 211 to 162 nm. When deposited on **S5** ($R_{ms} = 0.390 \pm 0.037$ nm), the size of the disc-like islands continuously drops to 125 nm. However, these isolated grains are not connected over a long range so that there is no sufficient conduction channel established allowing a charge carrier migration between source and drain electrodes.

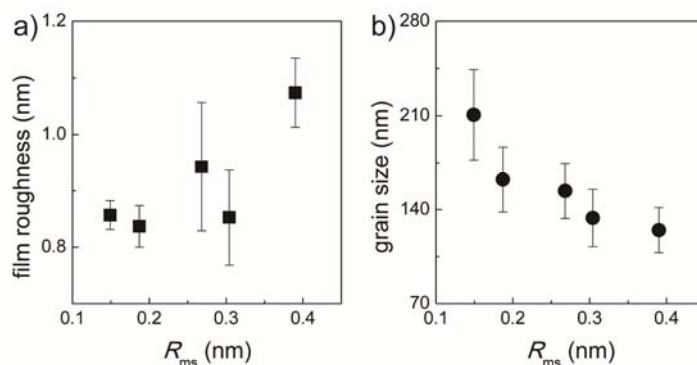


Figure 4.3 a) Film roughness and b) grain size of α,ω -DH6T 0.7 ML.

Deposition of further α,ω -DH6T molecules on the dielectric surface leads to a slow coalescence of the isolated circular grains and finally to a fully covered single molecular layer. Based on the first monolayer, the second layer begins to grow, as shown in Figure 4.4. The corresponding AFM images exhibit that the coverage of the second layer is approximately 50-65% (Figure 4.5b), defined as 1.5 ML. In comparison with 0.7 ML, the microstructure evolution of α,ω -DH6T 1.5 ML is far more distinct. It must be noted that the growth mechanism of the first layer significantly differs from that of subsequent layers. The first layer is directly deposited on the SiO_2 surface under the influence of molecule-dielectric interactions, while the other layers are grown on top of the α,ω -DH6T monolayer under the impact of molecule-molecule interactions. On **S1**, the isolated grains with 389 nm in diameter are deposited, and few aggregates appear on their top indicating the starting growth of

the third layer. The dark background in the AFM images represents the fully covered first monolayer. It is obvious from Figure 4.5a that the grain size on **S2** is dramatically declined to 223 nm. Dielectrics with higher R_{ms} values generate compact plate-like grains with the size reduction from 214 nm at $R_{ms} = 0.268 \pm 0.031$ nm (**S3**) to 127 nm at $R_{ms} = 0.390 \pm 0.037$ nm (**S5**). The decline in grain size reaches 67 % for the second layer of 1.5 ML, compared with the value of 41 % for 0.7 ML. Such variation can be related to the difference between molecule-molecule and molecule-dielectric interactions.

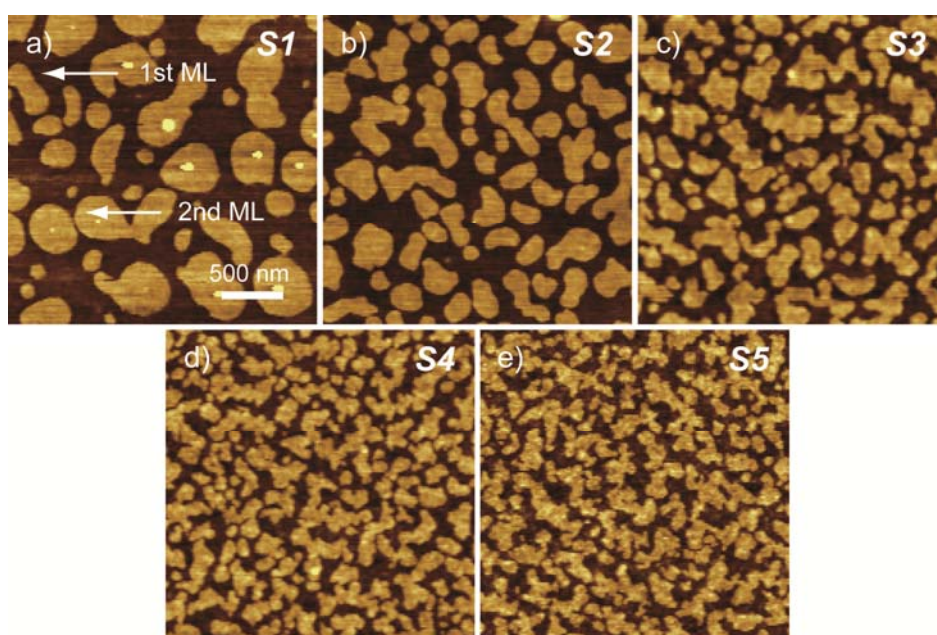


Figure 4.4 AFM images of sublimed α,ω -DH6T 1.5 ML on **S1-S5**. All images have the same scale bar.

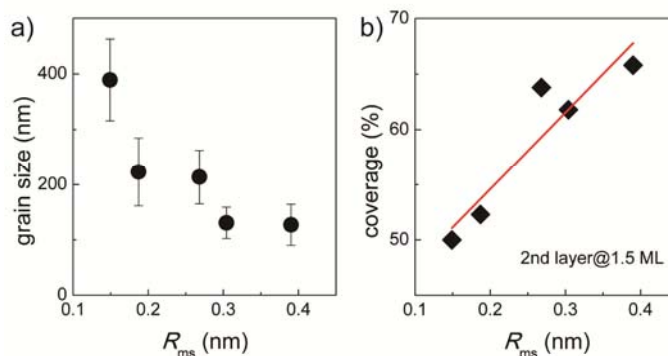


Figure 4.5 a) Grain size of α,ω -DH6T 1.5 ML. b) The film coverage of the second layer of α,ω -DH6T 1.5 ML.

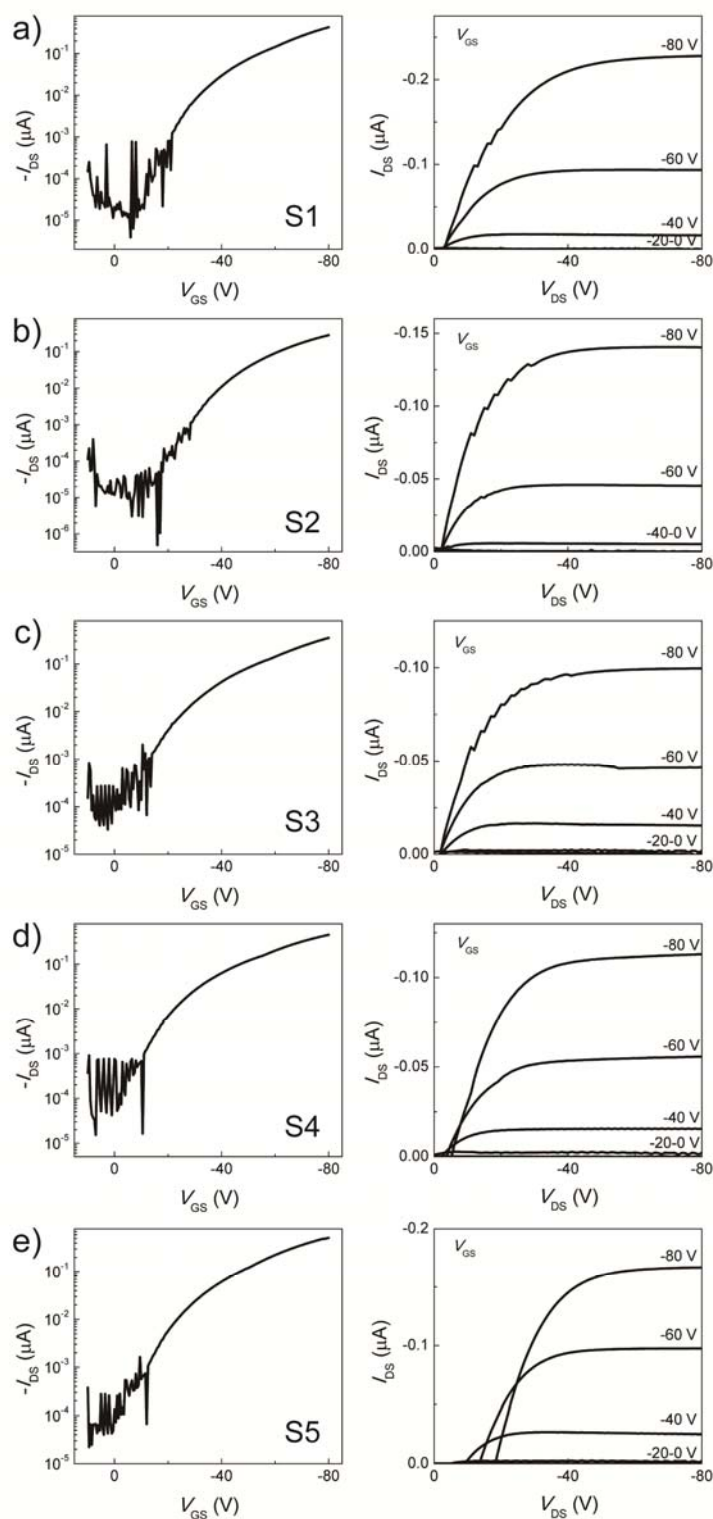


Figure 4.6 Transfer and output characteristics of DH6T 1.5 ML on **S1-S5**. Drain-source voltage (V_{DS}) of -80 V is applied in all cases. In the output curves of Figure e, a large drain current offset that is defined as the drain current at different V_{GS} and $V_{DS}=0$ V is observed. This can be attributed to the gate-induced leakage current.^[14]

To gain information about the charge carrier migration in the 1.5 ML, OFET devices are fabricated in a top-contact bottom-gate configuration. Source and drain electrodes are deposited by Au evaporation with 60 nm in thickness. The transfer and output characteristics depict typical linear/saturation behavior for all transistors (Figure 4.6). Since the second layer of 1.5 ML does not form a long-range connection, it is believed that the charge carrier transport is primarily determined by the first monolayer. The transistors for **S1** show an average hole mobility of $2.04 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ with the maximum value of $2.25 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. This value is identical to the previous report for α, ω -DH6T on non-functionalized SiO_2 .^[5] It seems reasonable to expect a lower transistor performance for **S5** because of smaller grain size, higher density of trapping sites at the semiconductor/dielectric interface and stronger surface scattering effects on charge carriers. Surprisingly, transistors for **S5** exhibit similar mobilities with an average value of $1.47 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. This behavior can be related to the size and linkage between domains in the second layer. The islands of the second layer on the rough dielectric **S5** are smaller than on **S1**, but interconnected over a relatively longer range due to a higher film coverage (Figures 4.5b), which is beneficial for bridging over structural defects of the first monolayer creating additional pathways for the charge carriers.^[6] The on/off ratio is also independent of the dielectric roughness, with a value of 10^4 . Additionally, the output plots of 1.5 ML on **S5** at low V_{DS} present a large I_{DS} offset, defined as the drain current at different V_{GS} and $V_{\text{DS}} = 0 \text{ V}$, originating from the gate-induced leakage current (Figure 4.6e).^[14]

In previous studies, relatively thick films of between 50 nm and 150 nm were usually deposited on the dielectrics with surface roughness in the nanometer range leading to the microstructure change in the entire film.^[15-19] In contrast, sub-nm dielectric roughness realizes the control of only interfacial microstructure revealing its intrinsic role in charge carrier transport (chapter 3). As a result, the growth of sublimed α, ω -DH6T multilayers is controlled by sub-nm dielectric roughness. The topographies of α, ω -DH6T 3 monolayers (3 ML) are present in Figure 4.7. The dark isolated spots with tens of nanometers in size represent the completely covered second layer. A higher dielectric roughness causes a smaller grain size in the third layer that is

indicated by dash circles in Figure 4.7. Additionally, few aggregates grow on the top of the third layer suggesting the nucleation of the forth layer, whereby the density of these nucleation points becomes higher on the dielectric with a higher R_{ms} value. In comparison to α,ω -DH6T monolayer, it seems that the roughness-dependence of molecular self-assembly for 3 ML becomes weaker.

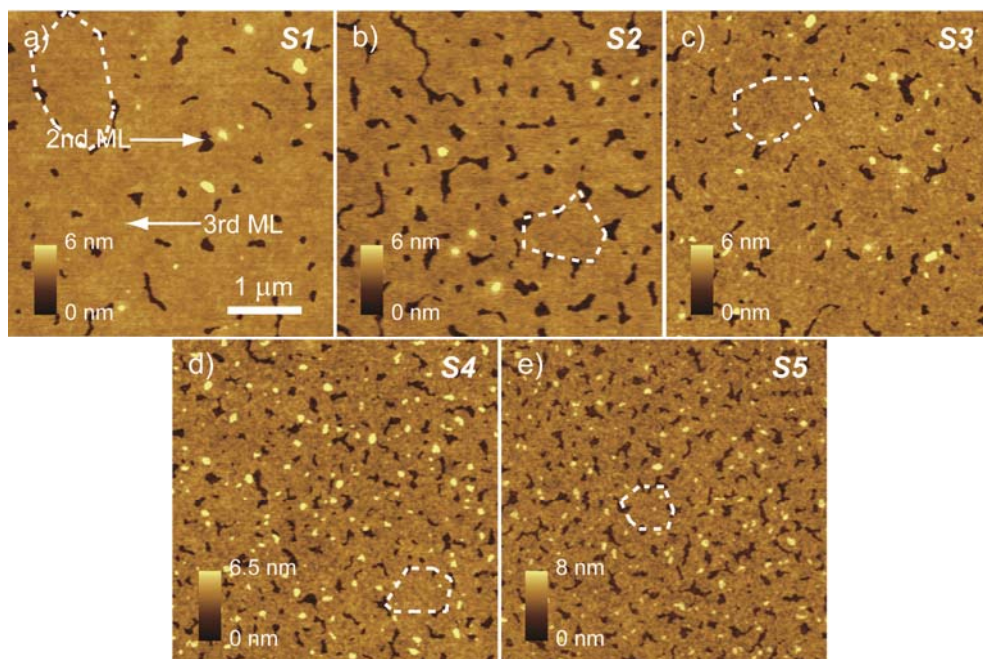


Figure 4.7 AFM images of sublimed α,ω -DH6T 3 ML on **S1-S5**. All images have the same scale bar.

The additional layers build more pathways for charge carriers and therefore the field-effect mobility of α,ω -DH6T 3 ML is doubled compared with 1.5 ML. Figure 4.8 shows the transfer and output characteristics of α,ω -DH6T 3 ML on **S1-S5**. At $V_{DS}=-80$ V and $V_{GS}=-80$ V, the value of $-I_{DS}$ exhibits a gradual degradation from 1.45 to 0.75 μ A with increasing R_{ms} from 0.15 to 0.39 nm, which is ascribed to the smaller grain size (dash circles) and higher density of grain boundaries. At the same time, the turn-on voltage of the transistor for **S5** is increased due to induced trapping sites and the effect of surface scattering.^[16, 20] As the dielectric roughness increases, the average value of hole mobility only slightly is reduced from $4.48 \times 10^{-3} \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ at $R_{ms}=0.149 \pm 0.006$ nm (**S1**) to $2.86 \times 10^{-3} \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ at $R_{ms}=0.390 \pm 0.037$ nm (**S5**). In addition, all transistors of α,ω -DH6T 3ML show similar on/off ratio, with the value of 10^4 - 10^5

(Table 4.2).

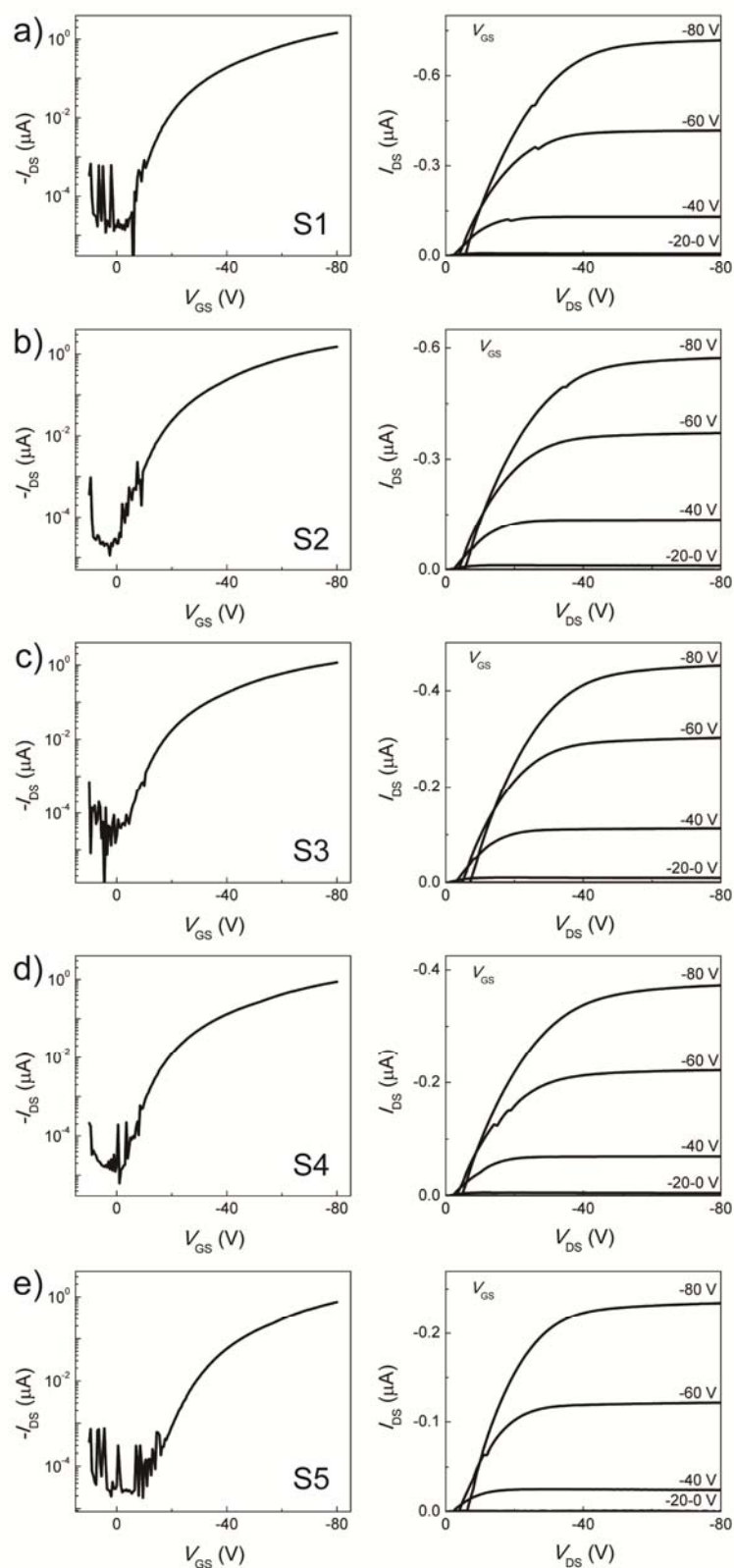


Figure 4.8 Transfer and output characteristics of DH6T 3 ML on **S1-S5**. Drain-source voltage (V_{DS}) of -80 V is applied in all cases.

Table 4.2 The on/off ratio of DH6T thin films deposited on different dielectrics.

dielectric	S1	S2	S3	S4	S5
1.5 ML	10^4	10^4	10^4	10^4	10^4
3 ML	10^5	10^4	10^4	10^4	10^4
10 ML	10^4	10^4	10^4	10^4	10^4

Finally, α,ω -DH6T 10 ML is fabricated with ~ 30 nm in thickness. AFM images in Figure 4.9 exhibit identical topographies with only slight differences in film coverage of the top layer indicating the independence of molecular self-assembly on the dielectric roughness for thicker films. Interestingly, the monolayer thickness of 3.9 nm on the top of 10 ML is higher (Figure 4.10) than that in the first interfacial molecular layer (~ 2.9 nm, Figure 4.2), which can be ascribed to the growth mode of Frank van der Merwe (FW) or layer by layer of sublimed α,ω -DH6T. In a FW mode, the interfacial adhesion between the first layer and substrate is stronger than that between the first layer and upper ones.^[21] Therefore, the molecule in the first layer tends to be lying-down on the substrate resulting in a smaller monolayer thickness. In contrast, the molecule in the upper layers prefers to stand up due to the weaker interaction, and a higher monolayer thickness is observed.

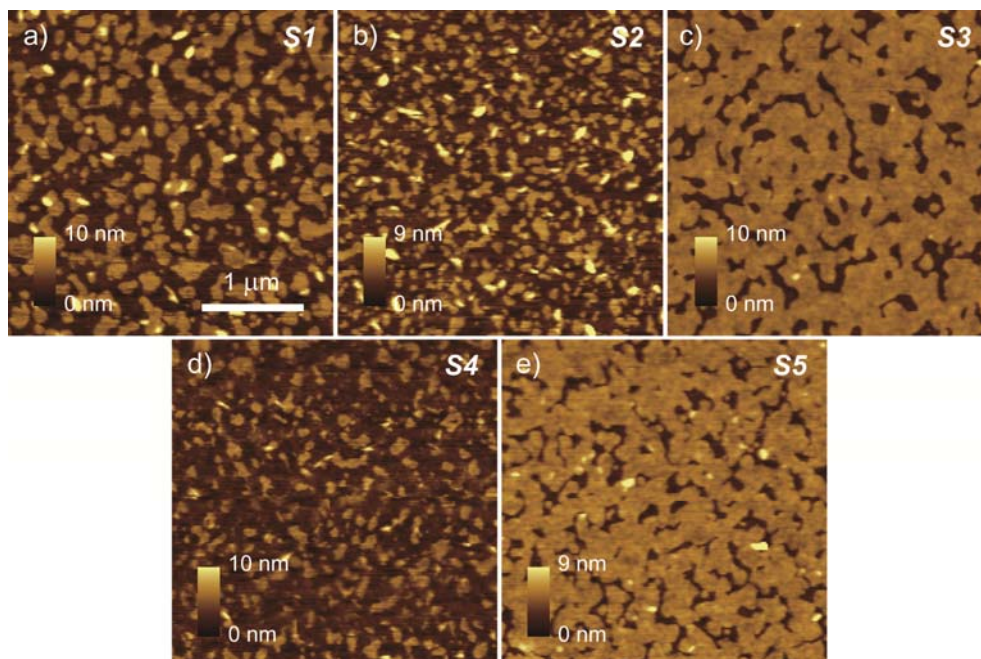


Figure 4.9 AFM images of sublimed α,ω -DH6T 10 ML on S1-S5. All images have the same scale bar.

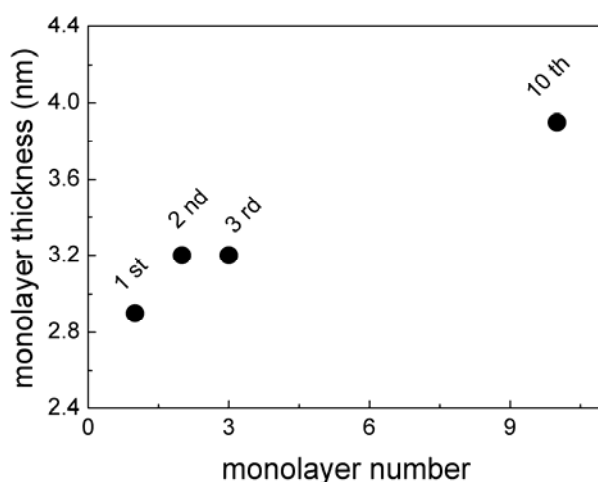


Figure 4.10 The thickness of the top monolayer. The monolayer closest to the dielectric surface is defined as the 1st monolayer.

To identify the influence of dielectric roughness on the molecular organization, GIWAXS measurement is performed. Film thicknesses of α,ω -DH6T below 10 nm do not yield reasonable X-ray scattering. Therefore, 10 ML films on **S1** and **S5** are characterized by GIWAXS, as shown in Figures 4.11a,b. In both cases, the GIWAXS pattern exhibits a well-defined organization which is confirmed by reflections up to the second order appearing on the meridional plane (q_z). For the sample on **S1** the first order peak is localized at $q_z = 0.19 \text{ \AA}^{-1}$ and $q_{xy} = 0 \text{ \AA}^{-1}$ indicating an interlayer distance of 3.30 nm (Figure 4.11a). An additional reflection on the off-equatorial at $q_z=0.44 \text{ \AA}^{-1}$ and $q_{xy}=1.29 \text{ \AA}^{-1}$ (labeled as peak “B” in Figure 4.11a) corresponds to a d-spacing of 0.445 nm and is assigned to the hexyl side chains. Furthermore, an off-equatorial π -stacking peak (peak “A” in Figure 4.11a) appears at $q_z=0.80 \text{ \AA}^{-1}$ and $q_{xy}=1.37 \text{ \AA}^{-1}$ which is related to a d-spacing of 0.38 nm and indicates a tilting of edge-on arranged molecules in respect to the substrate.

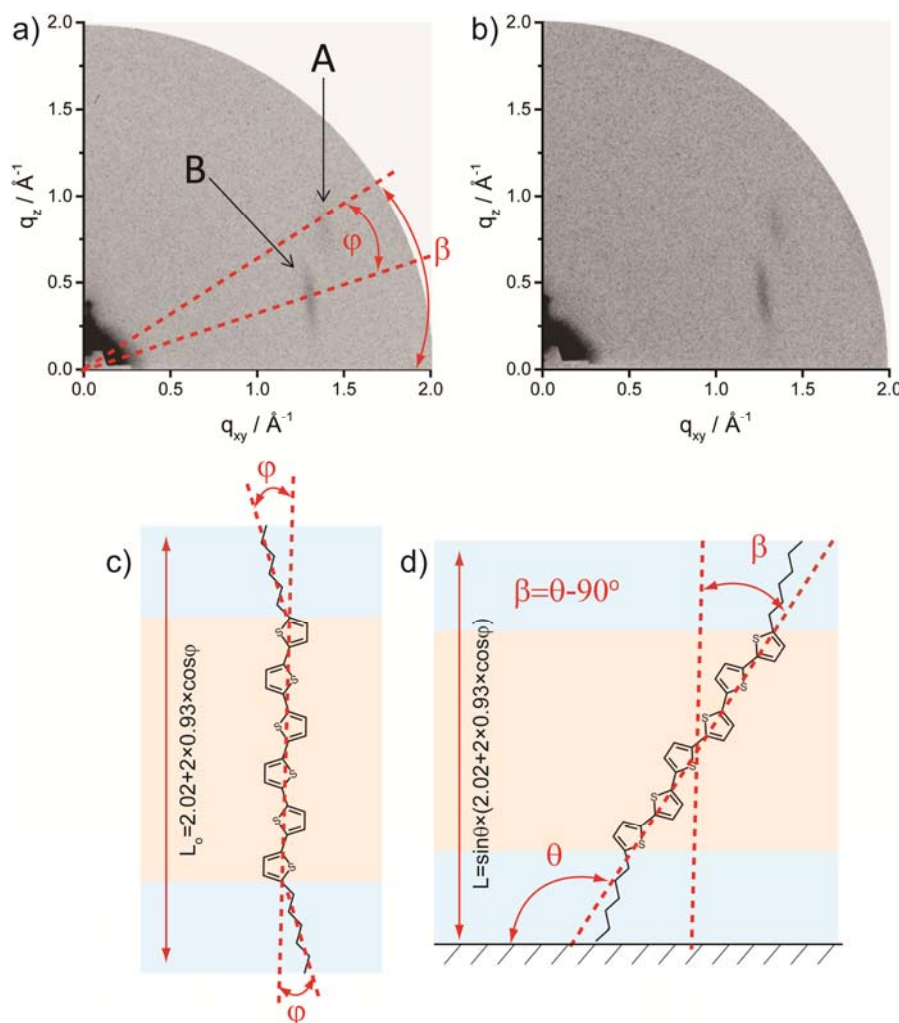


Figure 4.11 a-b) GIWAXS pattern of α,ω -DH6T 10 ML on **S1** and **S5**. Reflections indicated as A and B are assigned to π -stacking and alkyl chains, respectively. Schematic illustration of the surface organization of α,ω -DH6T: c) molecular conformation with alkyl chain tilting with respect to the α,ω -DH6T core, d) α,ω -DH6T tilting by an angle θ towards the substrate.

The precise conformation of the α,ω -DH6T molecules is evaluated on the basis of the following considerations (Figures 4.11 c,d). According to literature, the lengths of the conjugated thiophene core of 2.02 nm and each hexyl group of 0.93 nm are assumed.^[22] An angle between molecular core and substituents of $\phi = 32^\circ$ is estimated according to $\cos \phi = 0.38 \text{ nm} / 0.45 \text{ nm}$, with 0.38 nm as the closest π -stacking distance and 0.45 nm as the intermolecular distance between alkyl chains (Figures

4.11a and c). Taking the calculated angle φ into account, the length of the α,ω -DH6T molecule (L_0) can be determined: $L_0 = 2.02 + 2 \times 0.93 \times \cos \varphi = 2.02 + 2 \times 0.93 \times \cos 32^\circ = 3.59$ nm (Figure 4.11c). Based on results obtained for unsubstituted sexithiophene (6T) which is typically tilted by $\theta = 111.3^\circ$ on the surface a monolayer thickness of α,ω -DH6T is given by the projection on the $L_0 \sin \theta$ axis, leading to $3.59 \text{ nm} \times \sin 111.3^\circ = 3.34$ nm (Figure 4.11d). The calculated theoretical value is in agreement with the result obtained from GIWAXS (3.30 nm) for the film on **S1**. The interlayer distance of 3.15 nm for α,ω -DH6T 10 ML on **S5** is slightly smaller. A slight decrease in d-spacing is also found for the alkyl chains with 0.45 nm and π -stacking with 0.39 nm. Since the angle (φ) between the α,ω -DH6T core and the alkyl chain remains unchanged ($\cos \varphi = 0.39 \text{ nm} / 0.45 \text{ nm}$), the decrease in the interlayer distance for **S5** might be attributed to a larger molecular tilting (larger angle θ) with respect to the surface. In addition, the interlayer reflection for **S5** shows a minor reduction in full width at half maximum ($\text{FWHM} = 3.7 \times 10^{-3}$) compared with **S1** ($\text{FWHM} = 5.4 \times 10^{-3}$) indicating a larger coherence length ($\text{CL}_{\text{IL}} = 36$ nm) for **S5** than **S1** ($\text{CL}_{\text{IL}} = 25$ nm). At the same time, however, both α,ω -DH6T films on **S1** and **S5** exhibit almost the same in-plane coherence length in the π -stacking direction of $\text{CL}_\pi = 13$ nm. Since the main charge carrier transport takes place in-plane of the film, it is reasonable to expect a roughness-independent transistor performance.

In comparison with the ultrathin 1.5 and 3 ML films, α,ω -DH6T 10 ML exhibits a significantly improved charge carrier transport. At $V_{\text{DS}} = -80$ V and $V_{\text{GS}} = -80$ V, the value of $-I_{\text{DS}}$ for 10 ML is one order of magnitude higher than that for 3 ML (Figure 4.12). Moreover, the drain current at low V_{GS} in the transfer characteristics becomes smoother (Figure 4.12). α,ω -DH6T 10 ML devices for **S1** and **S5** show identical transfer curves. The mobility values range from 0.06 to 0.07 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ independent of the dielectric roughness. These results are in good agreement with chapter 3. The maximum mobility reaches $7.23 \times 10^{-2} \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$, which is, to the best of my knowledge, the highest mobility for α,ω -DH6T on non-functionalized SiO_2 dielectric without annealing treatment.^[5]

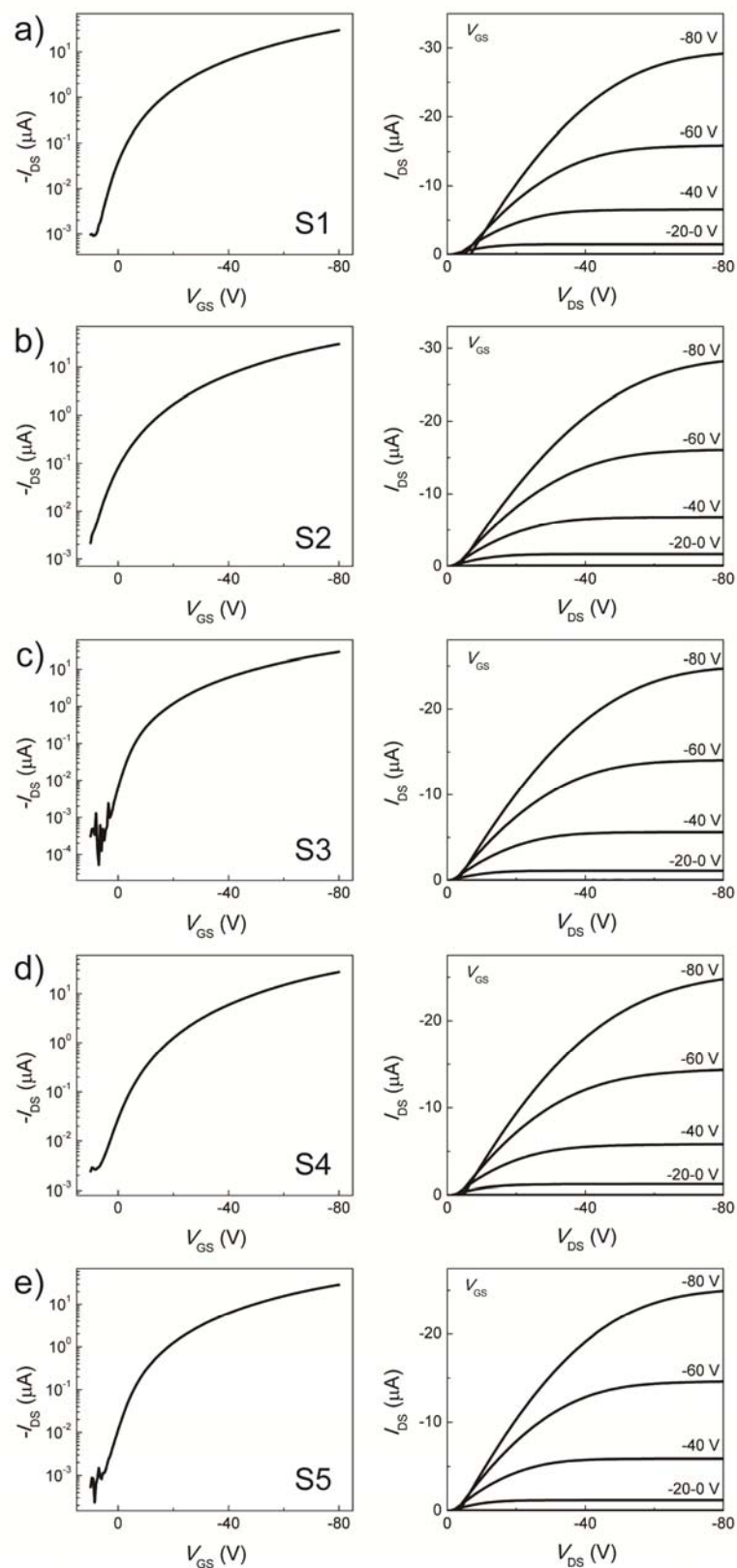


Figure 4.12 Transfer and output characteristics of DH6T 10 ML on S1-S5.

Drain-source voltage (V_{DS}) of -80 V is applied in all cases.

4.3 Role of Interfacial Microstructure on the Charge Carrier Transport

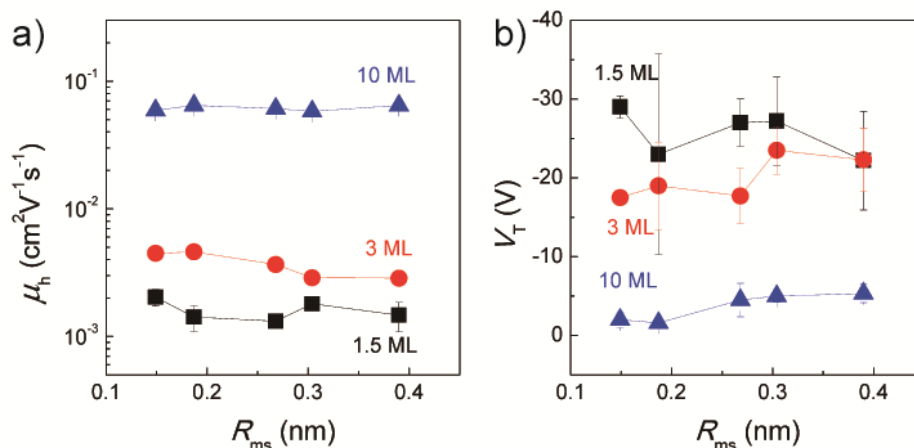


Figure 4.13 Hole mobility (a) and threshold voltage (b) of α,ω -DH6T thin films with different thicknesses as a function of dielectric roughness.

Vacuum sublimation used in this chapter effectively avoids the molecular aggregation in solution induced by the strong π -interactions of conjugated molecules, and provides a better chance to investigate the intrinsic role of interfacial microstructure. Figure 4.13 summarizes the OFET relevant parameters, including the saturation hole mobility (μ_h) and threshold voltage (V_T), as a function of dielectric roughness for α,ω -DH6T thin films with different thicknesses. The deposition of more layers obviously increases the hole mobility and effectively decreases the threshold voltage due to the generation of more pathways for the migration of charge carriers. The dielectric roughness on a sub-nanometer scale only has an influence on the microstructure of the interfacial layer, without affecting upper layers, and the mobility of multilayers is roughness independent, as shown in Figure 4.13a. These results indicate the negligible impact of interfacial microstructure on charge carrier transport strongly supporting the conclusion in chapter 3. This observation originates from sufficient pathways for charge carriers created in upper layers of multilayers. In other words, the disordered domains at the interfacial layer drive charge carriers

through upper layers with ordered domains, and three-dimensional (3D) conduction channel is formed.^[23] Interestingly, in contrast to solution processed monolayers, the mobility of thermally sublimed α,ω -DH6T 1.5 ML seems also barely dependent on the R_{ms} value within the investigated range. In spite of the roughness-dependent domain size for 1.5 ML, the interconnection of domains in the second layer compensates the effect of dielectric roughness on charge carrier transport.

4.4 Conclusion

The evolution of microstructure and charge carrier transport in α,ω -DH6T transistors has been investigated layer by layer by controlling the surface roughness of the dielectric on a sub-nm scale. Compared with the study in chapter 3 by solution processing, a similar roughness-dependence of the microstructure (grain size) is observed for thermally sublimed α,ω -DH6T monolayer (0.7 and 1.5 ML). However, the interconnection of domains in the second layer for 1.5 ML compensates the reduction in domain size of the first layer resulting in a roughness insensitive hole transport (within the investigated roughness range). The difference between solution processed and thermally sublimed monolayers can be attributed to the fact that solution processing allows conjugated molecules to pre-aggregate in solution before and during film deposition,^[24] while thermally sublimed molecules with more freedom can compensate the structural defects caused by the dielectric roughness. With the deposition of more layers, the influence of dielectric roughness on the microstructure of organic semiconductors disappears. GIWAXS for α,ω -DH6T 10 ML exhibits similar molecular organization such as interlayer and π -stacking distances independent of R_{ms} . At the same time, the impact of the dielectric roughness on the transistor performance is also negligible for 10 ML. The results presented in this chapter are in good agreement with chapter 3 providing more evidence that the interfacial microstructure has basically no impact on the charge carrier transport for thicker film. Therefore, a further progress of this finding has been taken on the

general significance applicable to all organic semiconductors independent of the deposition technique.

The importance of dielectric surfaces has been extensively proven by many research groups. On the surface of SiO₂, immobile Si-O⁻ ions exist, which are able to electrochemically trap the injected charge carriers.^[25] This is the reason why surface functionalization of SiO₂ by self-assembled monolayers is usually employed to reduce charge trappings and increase field-effect mobilities.^[25] These reports seem inconsistent with the conclusion obtained from chapter 3 and this chapter. However, what is changed by using sub-nm roughness is not the surface chemistry of the dielectric^[25] but the interfacial microstructure of the semiconducting layer, that is to say, it is the density of grain boundaries in the semiconductor that is varied. When the upper layers have less grain boundaries than the interfacial one, it is reasonable that charge carriers move to the upper layers with the formation of 3D conduction channel, and the transistor performance of the entire film is unaffected. In brief, the research object of previous studies is the surface property of the dielectric, and the object in chapter 3 and this chapter is the interfacial layer of the semiconductor close to the dielectric.

The conjugated molecule used in this chapter, α,ω -DH6T, possesses a layered two-dimensional (2D) growth mode (Frank-van der Merwe, FM), even for 10 ML. In comparison, most rod-like small molecules such as pentacene, have a three-dimensional growth, termed as island or Vollmer-Weber (VW) mode, where new molecular layers are formed before the completion of the underlying layers, or a Stranski-Krastanov (SK) growth mode with the combination of FM and VW.^[21, 26] On the other hand, the sublimation parameters such as deposition rate can also modulate the growth transition from 2D to 3D. In order to generalize the finding in this chapter, the organic semiconductors with various growth mode should be considered and investigated by using dielectric systems with surface roughness within a sub-nanometer range.

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Chapter 5

High Performance Conjugated Polymer Monolayer Transistors

5.1 Introduction

In chapter 1, the importance of the first few monolayers adjacent to the dielectric was emphasized. Furthermore, as indicated in chapters 3 and 4, a single molecular layer of organic semiconductors was able to provide sufficient pathways for charge carriers and create a conducting channel in monolayer transistors. Organic monolayer transistors are of particular interest, because they are not only an ideal platform to understand the transport mechanism but also own great potential in applications such as chemical and biological sensors with fast response and high sensitivity.^[1-3] Small molecules can be downscaled into monolayers as the active layer for OFETs by both vacuum thermal deposition and solution processing, leading to field-effect mobilities ranging from 10^{-2} to $1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[1, 4-13] Nevertheless, in comparison to their small molecule counterparts, it is still a great challenge to fabricate high-mobility monolayer transistors on the basis of conjugated polymers. In spite of considerable efforts on polymer monolayer transistors, only relatively low field-effect mobility could be obtained ($< 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$),^[14-19] even for a monolayer with well-defined microstructures ($1\text{-}6 \times 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$).^[20-21]

The self-organization behavior of conjugated polymers in solution has a pronounced influence on the film morphology and subsequent device performance. Aggregates that are induced by strong molecule-molecule interaction normally represent domains in which molecules are self-assembled in a good orientation.^[22] Therefore, higher aggregation can efficiently inhibit the formation of amorphous films and play a positive role in molecular ordering.^[23] Sometimes the nature of polymer aggregation was found to determine the polymer packing in thin films significantly influencing the OFET performance.^[24] It was reported that the self-assembly behavior of conjugated polymers in solution was strongly dependent on the used solvent and solution temperature allowing the fine control of film morphology and device performance.^[25-27] For instance, a strong aggregation in solution was found for a 5,6-difluorobenzothiadiazole based copolymer (FBT-Th₄(1,4)), and a proper control of aggregation by solution temperature resulted in excellent device performances in both OFETs and organic solar cells (OSCs).^[27-28]

In this chapter, a single molecular layer of a high-mobility conjugated polymer, FBT-Th₄(1,4), is deposited by dip-coating at room temperature allowing the fine control of the polymer domain size. This polymer monolayer exhibits a high crystallinity and a strong π - π stacking interaction in an edge-on fashion leading to an excellent charge carrier transport with the field-effect mobility over $3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. The optimization of the semiconductor/electrode interface and source/drain geometry is described in great details. This chapter proves the possibility of high performance polymer monolayer transistor, and opens up a new pathway for bottom-up organic electronics.^[10]

5.2 Fabrication of Polymer Monolayer

As mentioned in chapter 3, FBT-Th₄(1,4) is a high-mobility semicrystalline conjugated polymer with the field-effect mobility over $1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[27-28] In particular, a well-defined microstructure consisting of nanofibers can be deposited by

dip-coating, and the resultant FBT-Th₄(1,4) monolayer exhibit a hole mobility on the orders of $10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (chapter 3). It is widely reported that a higher molecular weight of semiconducting polymers is favorable for charge carrier transport because ordered regions in thin films can be more densely interconnected by longer polymer chains.^[29-33] Therefore, in this chapter, FBT-Th₄(1,4) with higher molecular weight ($M_n = 47.3 \text{ K g/mol}$) is processed in solution, and a high-mobility monolayer transistor is expected. In order to fabricate thin films by dip-coating, chloroform solution at a concentration of 0.5 mg/mL is prepared. It is clear from Figure 5.1 that the diluted FBT-Th₄(1,4) solution (chloroform, 0.025 mg/mL, 25 °C) shows identical UV-Vis absorption spectra to thin films indicating a strong aggregation of polymer chains in solution.^[27-28] There are a strong 0-0 transition peak at 700 nm and two resolved shoulders at 638 and 457 nm, respectively.

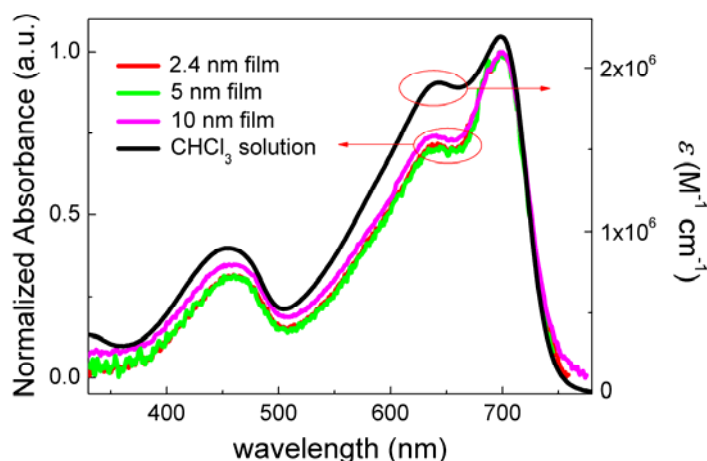


Figure 5.1 UV-Vis absorption spectra of FBT-Th₄(1,4) as thin films and in solution of chloroform (0.025 mg/mL, 25 °C). Thin films with the thickness of 2.4, 5 and 10 nm are deposited on quartz wafers by dip-coating from 0.5 mg/mL chloroform solution at 200, 100 and 50 $\mu\text{m/s}$, respectively.

By continuously tuning the dip-coating speed from 1000 to 50 $\mu\text{m/s}$, FBT-Th₄(1,4) ultrathin films from monolayer to multilayers fabricated by dip-coating from 0.5 mg/mL chloroform solution, and their morphologies are characterized by AFM in tapping mode, as shown in Figure 5.2. Herein the substrates for film deposition are

heavily doped silicon with thermally grown SiO₂ (SiO₂/Si). The dip-coating speed ranging from 1000 to 200 $\mu\text{m/s}$ induces the formation of FBT-Th₄(1,4) monolayers with ~ 2.4 nm in thickness (Figure 5.2e). At 1000 $\mu\text{m/s}$, the dip-coated polymer monolayer consists of nanofibers with 389 ± 138 nm in length and 48 ± 18 nm in width (Figure 5.2a and 5.3). It is evident from Figure 5.2b that a lower speed (400 $\mu\text{m/s}$) effectively increases the fiber size, and the dimension reaches 545 ± 149 nm in length and 61 ± 21 nm in width (Figure 5.3). Moreover, the dip-coating speed of 200 $\mu\text{m/s}$ results in a significant increase in the monolayer coverage from 62 % to 82 % and a continuous enhancement in both fiber length (724 ± 217 nm) and width (73 ± 26 nm) (Figure 5.2c and 5.3). The nuclei of the second layer starts to grow on top of the first one (Figure 5.2c,e), but the polymer thin film dip-coated at 200 $\mu\text{m/s}$ is still defined as monolayer since the coverage of the second layer is < 7 %. A low dip-coating speed provides more time for the molecular transition from a solution to solid state leading to larger domains (fibers).^[28] A further decrease in dip-coating speed (50 $\mu\text{m/s}$) leads to more molecules deposited on the substrate with the thickness of ~ 10 nm that is equivalent to four single molecular layers assuming an edge-on surface organization. However, the fiber dimension remains almost unchanged in comparison to that at 200 $\mu\text{m/s}$, as shown in Figure 5.3.

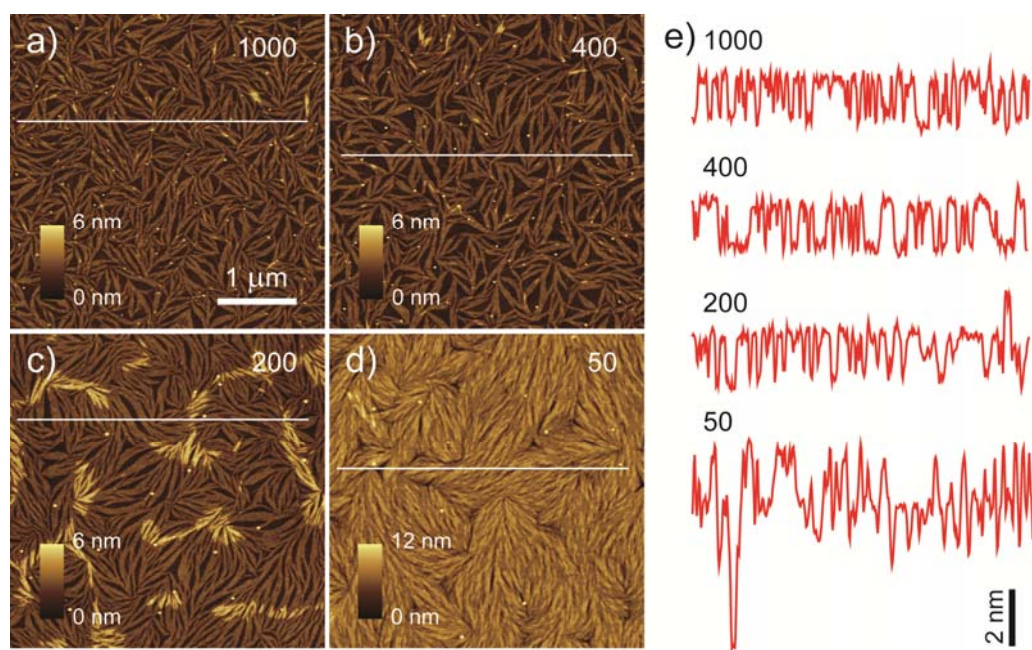


Figure 5.2 a-d) AFM images of FBT-Th₄(1,4) thin films from monolayer to

multilayers fabricated by dip-coating from a 0.5 mg/mL chloroform solution. The dip-coating speeds are 1000, 400, 200 and 50 $\mu\text{m/s}$ for a-d), respectively. All AFM images have the same scale bar. e) Corresponding height profiles of a-d).

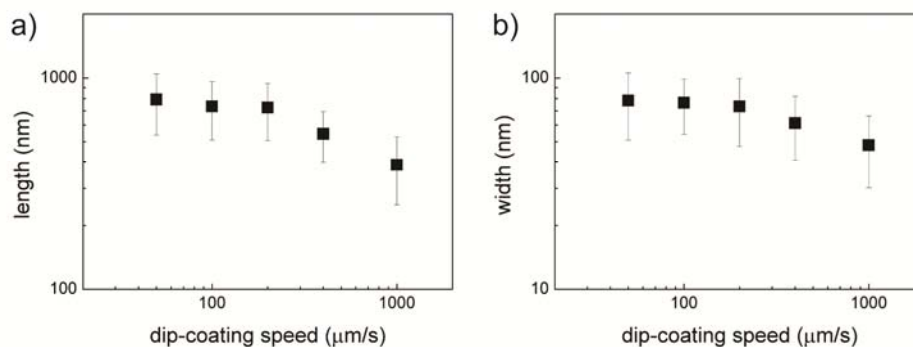


Figure 5.3 The analysis of fiber dimensions in which over 100 fibers are analyzed for each sample.

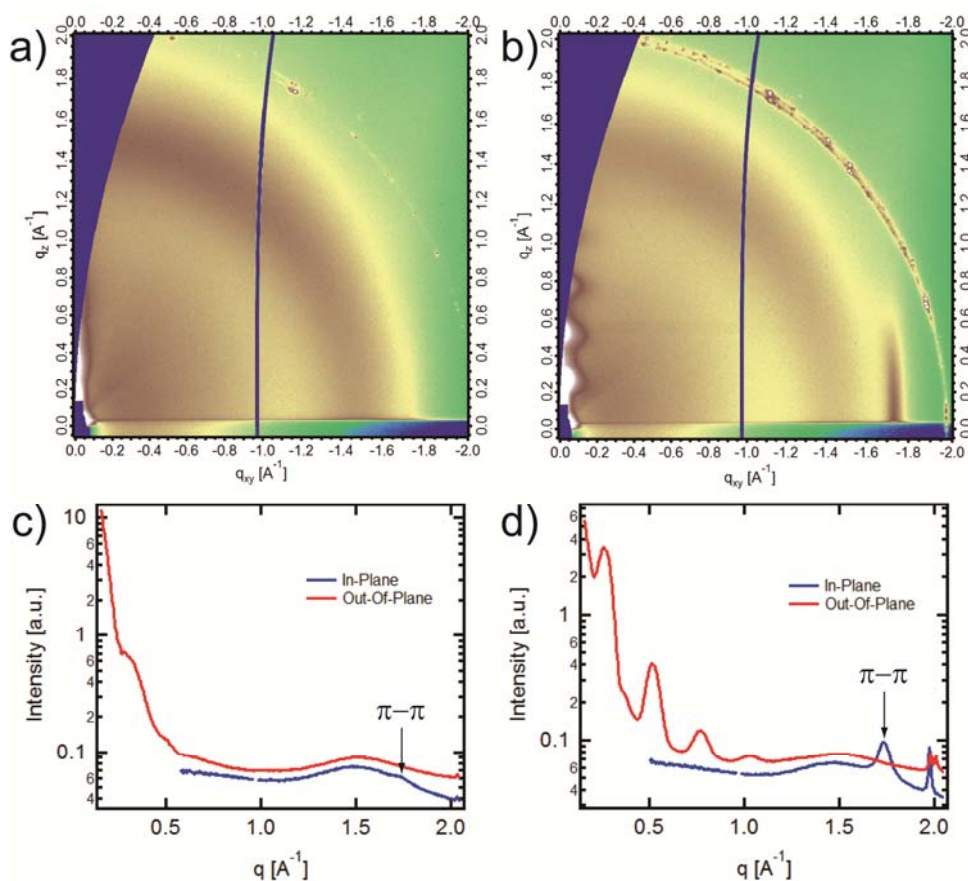


Figure 5.4 GIWAXS patterns of FBT-Th₄(1,4) mono- (a, 200 $\mu\text{m/s}$) and 4 layers (b, 50 $\mu\text{m/s}$). c-d) The out-of- and in-plane profiles of a-b). The peak at $q_{xy} = 2 \text{ \AA}^{-1}$ is the feature from Si dust on the sample.

To gain the structural information of FBT-Th₄(1,4) ultrathin films, GIWAXS experiments are performed for mono- and 4 layers which are dip-coated at 200 and 50 $\mu\text{m/s}$, respectively. Figure 5.4a shows the GIWAXS pattern for polymer monolayer, and a π -stacking distance of 0.36 nm is determined from in-plane reflections indicating high degree of molecular ordering in an edge-on fashion (Figure 5.4c). In comparison, polymer multilayers (4 layers) exhibit stronger diffraction intensities, as shown in Figure 5.4b. The out-of-plane profile (Figure 5.4d) indicates an interlayer spacing of ~ 2.4 nm revealing higher order reflections. It is clear from the in-plane profile that a stronger π -stacking peak appears at the same position as found for the monolayer ($q_{xy} = 1.7 \text{ \AA}^{-1}$).

5.3 Monolayer Transistors with Unfunctionalized Gold Electrodes

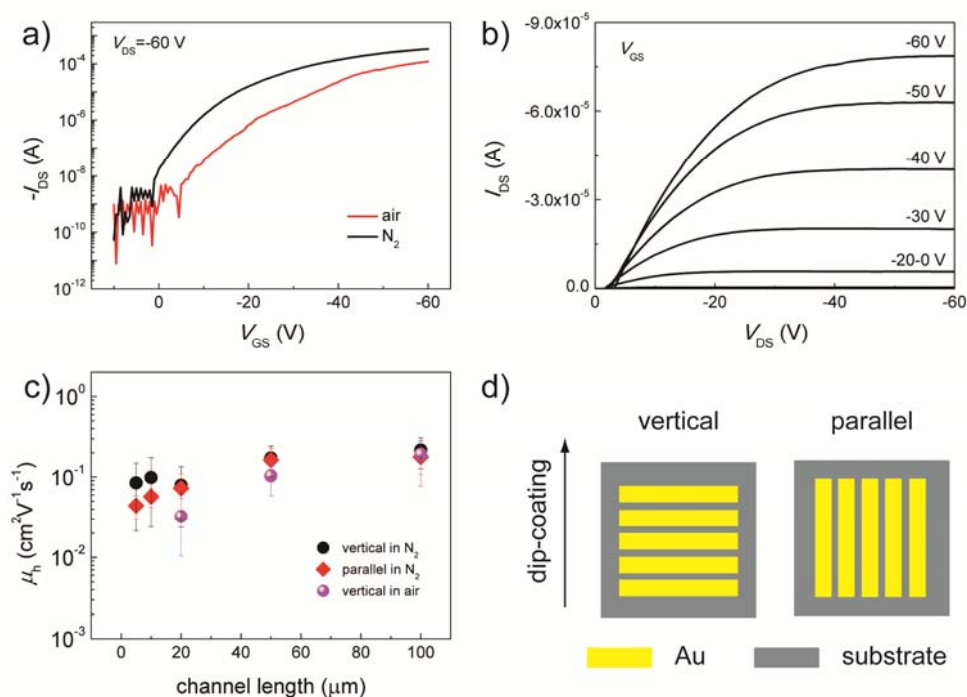


Figure 5.5 a,b) Transfer and output characteristics of FBT-Th₄(1,4) monolayer transistors under nitrogen atmosphere. In a), the red curve represents the transfer characteristics measured in air. c) Summary of hole mobility as a function of channel length. Over 120 devices were measured. d) Schematic illustration for the dip-coating procedure in which the channel is vertical or parallel to the dip-coating direction.

To quantitatively elucidate the charge carrier transport of FBT-Th₄(1,4) monolayers, OFET devices are fabricated with a bottom-contact bottom-gate (BCBG) configuration. Heavily doped silicon wafers with 300-nm-thick thermally grown SiO₂ as dielectric and pre-patterned 50-nm-thick Au electrodes as source and drain are utilized as substrates for the polymer monolayer deposition. In this chapter the SAM modification for the dielectric surface is not employed since the surface of modified dielectric by common SAMs such as HMDS is generally hydrophobic,^[34] which effectively hinders the molecular deposition onto the substrate during dip-coating. Due to the production of a polymer monolayer with higher coverage and larger fiber dimension, the dip-coating speed of 200 $\mu\text{m/s}$ is chosen for the monolayer deposition. After the deposition of the polymer monolayer, annealing at 100 $^{\circ}\text{C}$ for 0.5 h is performed to remove the residual solvent, but this post-treatment has no effect on both morphology and molecular organization, as proven in chapter 3 and literature.^[27] The monolayer transistors are measured in a glovebox under a nitrogen atmosphere, and the transfer and output characteristics of all devices exhibit a typical linear/saturation behavior, as shown in Figure 5.5 a,b. The saturation mobility is extracted from transfer plots with the average value of $0.27 \pm 0.12 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. The on/off ratio reaches 10^6 . Furthermore, the OFET characterizations are also performed under an ambient environment (red plots in Figure 5.5a). It is found that the hole mobility retains $\sim 70\%$ of the initial value after exposed in air within 30 min, which is in agreement with the literature.^[27] However, the moisture and O₂ molecules could induce some trapping sites at the semiconductor/dielectric interface leading to degradation in threshold voltage from -10 to -24 V. On the other hand, the charge carrier transport in FBT-Th₄(1,4) monolayer transistors is independent of the dip-coating direction, which can be attributed to the random orientation of nanofibers (Figure 5.2). Figure 5.5c summarizes the relationship between hole mobility and channel length after the measurement of over 120 devices. It is obvious that the charge carrier transport in polymer monolayer transistors is slightly improved with increasing channel length originating from the contact between polymer monolayer and Au electrodes.

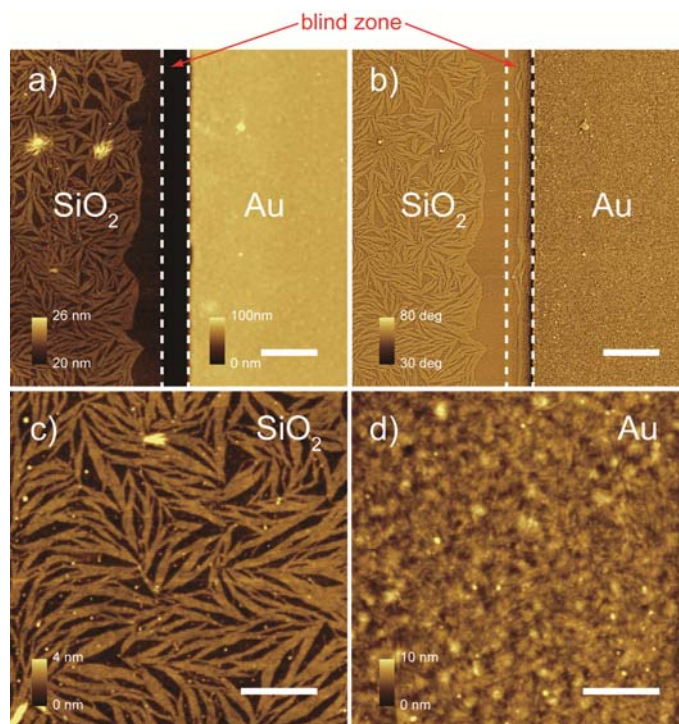


Figure 5.6 AFM height (a) and phase (b) images of the contact region, and enlarged images of FBT-Th₄(1,4) monolayer on surfaces of SiO₂ (c) and Au electrodes (d). The scale bars are 1 μm and 500 nm for a,b) and c,d), respectively. The height difference between SiO₂ and Au electrodes is 50 nm.

Figure 5.5b exhibits the output plots where a non-linear drain current appears at low drain voltage (V_{DS}). This could be another evidence for the contact problems between semiconductor and metal electrodes. To confirm this hypothesis, the topography of the contact region is characterized by AFM in tapping mode, as shown in Figure 5.6. The self-assembly of FBT-Th₄(1,4) monolayer is strongly dependent on the surface property of the substrate. On the SiO₂ surface, the polymer monolayer consists of nanofibers with $\sim 1\ \mu\text{m}$ in length (Figure 5.6c) well correlating with the morphology in Figure 5.2. On the contrary, the polymer self-organization is severely hindered on the surface of Au electrodes leading to the formation of nanoaggregates. This difference in microstructure, as well as the SiO₂/Au height difference, results in a poor connection of polymer monolayer at the interface critically affecting the charge carrier transport in monolayer transistor. This contact resistance can be reduced from two aspects. First, an electrode material that possesses a better compatibility with

organic semiconductors should be used instead of gold, which will be favorable for the self-assembly of FBT-Th₄(1,4) monolayer (section 5.4). Second, the surface of Au electrodes should be functionalized by SAMs, which will not only result in a better microstructure of FBT-Th₄(1,4) monolayer but also reduce the energy barrier of charge injection^[35] (section 5.5).

5.4 Monolayer Transistors with Graphene Electrodes

Graphene, a two-dimensional atomically thick carbon atom arranged in a honeycomb lattice, has an excellent compatibility with organic semiconductors enabling a low contact resistance and long-time operation.^[36] Furthermore, its work function (~ -4.5 eV^[37]) is more suitable for various organic semiconductors such as pentacene compared with metals leading to the improved carrier injection efficiency.^[38] Both advantages of graphene make it an ideal electrode material in organic electronics.^[39-40] In this section, thin films of exfoliated graphene with the thickness of 50 nm are pre-patterned on Si/SiO₂ wafer as the source and drain electrodes,^[41-42] and the experimental details are described in chapter 9.4.2.

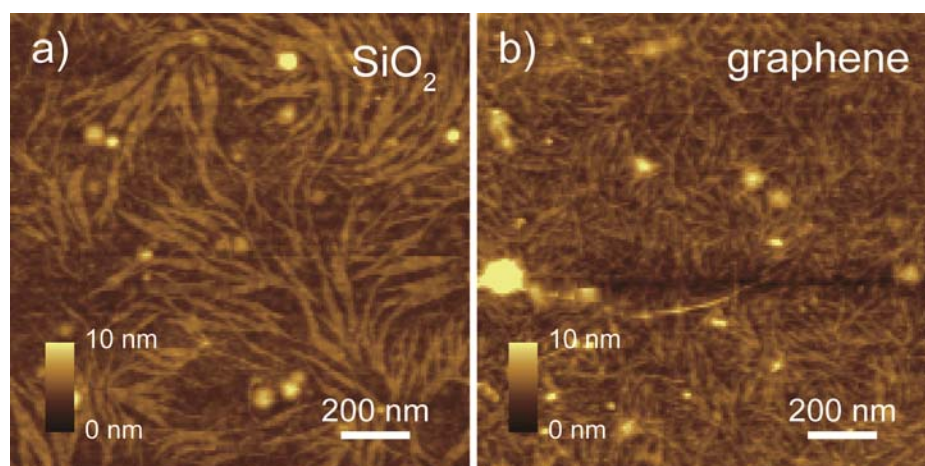


Figure 5.7 AFM height images of FBT-Th₄(1,4) monolayer on surfaces of SiO₂ (a) and graphene (b).

It was found that graphene has a remarkable impact on the self-assembly of organic semiconductors due to the strong π – π stacking interaction.^[43-45] For example,

pentacene molecules tended to stand up on the surface of SiO₂, but a face-on molecular orientation is induced on the surface of cleaned graphene.^[46] Figure 5.7 exhibits the influence of the graphene electrode on the morphology of FBT-Th₄(1,4) monolayer. In comparison to SiO₂, nanofiber networks with smaller dimension are observed on the graphene electrodes originating from the strong π - π stacking interaction between polymer and graphene. Such molecular ordering is still higher than that on Au surface (nanoaggregates, Figure 5.6d) indicating a better compatibility between graphene with conjugated polymer.

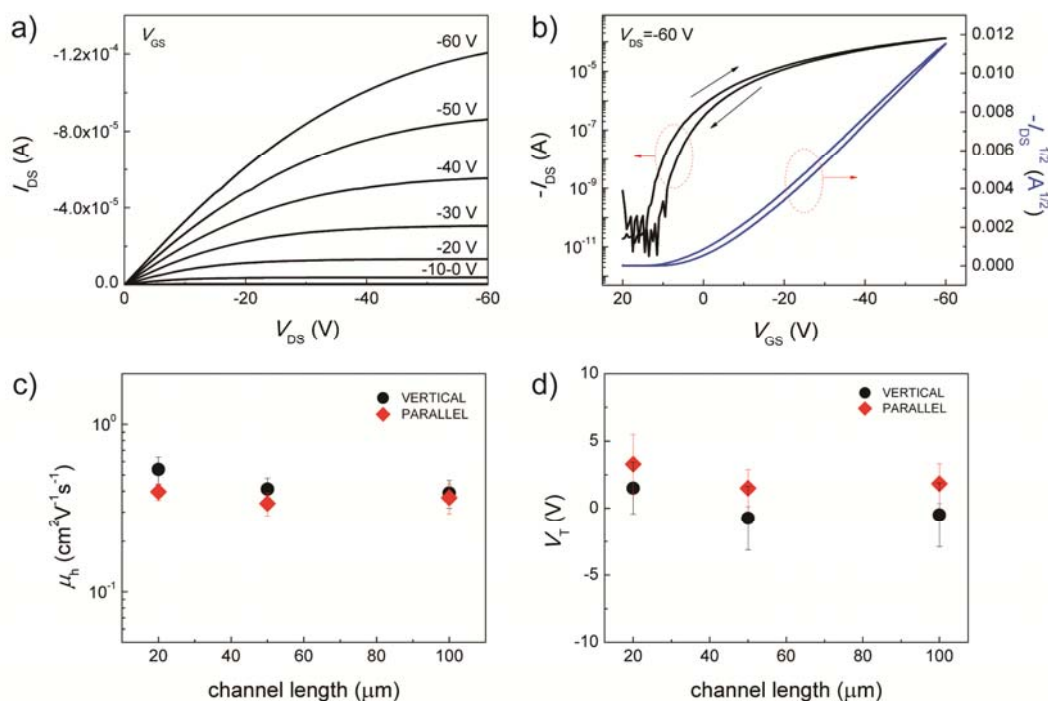


Figure 5.8 Output (a) and transfer (b) characteristics of FBT-Th₄(1,4) monolayer with graphene as source and drain (S/D) electrodes. The dependence of hole mobility (c) and threshold voltage (d) on the channel length, where monolayers are deposited with S/D electrodes vertical (black circles) or parallel (red diamonds) to the dip-coating direction.

The device performance of FBT-Th₄(1,4) monolayer transistors with graphene as electrodes is shown in Figure 5.8. It can be clearly seen from the output characteristics (Figure 5.8 a) that the drain current presents a linear behavior at low V_{DS} suggesting a

negligible contact resistance between polymer monolayer and graphene electrodes. The transfer plots in Figure 5.8b depict a minor hysteresis effect resulting from the unmodified SiO₂. Compared with Au electrodes, the application of graphene as electrodes leads to an improved charge carrier transport in polymer monolayer transistors. An average hole mobility of $0.41 \pm 0.10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ is obtained with the on/off ratio of 10^7 and the threshold voltage of 1 V after the measurement of 45 transistors. The highest mobility reaches to $0.73 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Graphene electrodes with three different channel lengths of 20, 50 and 100 μm are prepared. Both hole mobility and threshold voltage are almost independent on the channel length identical to the results with Au electrodes in section 5.3, as shown in Figure 5.8 c,d. In addition, transistors with graphene S/D vertical and parallel to the dip-coating direction confirm the isotropic charge carrier transport because of the random distribution of nanofibers in polymer monolayer (Figure 5.8 c,d).

5.5 Monolayer Transistors with Functionalized Gold Electrodes

In spite of enhanced compatibility between graphene with FBT-Th₄(1,4), it must be emphasized that the work function of Au (-5.1 eV) is much closer to the HOMO level of FBT-Th₄(1,4) than graphene (-4.5 eV).^[27, 47] Therefore, if the contact problem between polymer monolayer and Au electrodes can be solved, Au will be a better choice as electrode material than graphene in the case of FBT-Th₄(1,4). For BCBG OFET devices, the surface modification at semiconductor/electrodes is an effective way to solve this problem.^[35] Therefore, the Au electrodes on the pre-patterned substrate (section 5.3) are functionalized by 2,3,4,5,6-pentafluorothiophenol (PFBT) SAMs before monolayer deposition.^[48] PFBT SAMs has no obvious influence on the self-assembly of polymer monolayer in the channel (SiO₂).

Figure 5.9 shows the morphology of FBT-Th₄(1,4) monolayer on the Au surface modified with PFBT SAMs, and a longer range ordering is observed indicating the improved compatibility between semiconductor and electrodes. Transfer and output

characteristics of FBT-Th₄(1,4) monolayer transistor are shown in Figure 5.10 a,b exhibiting a typical linear/saturation behavior. The transfer plots are characterized in both linear and saturation regimes at V_{DS} of -2 and -30 V. The polymer monolayer exhibits an excellent hole transport with negligible hysteresis effect (Figure 5.10 a). The field-effect mobilities in both regimes are extracted from transfer plots, and the values of $\mu_{lin}=1.02 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $\mu_{sat}=2.08 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ are obtained. Near-ideal output plots are observed from Figure 5.10 b, especially at low V_{DS} , indicating a good contact between Au electrodes and polymer monolayer due to the application of PFBT SAMs modification. To evaluate the transistor performance of FBT-Th₄(1,4) monolayer more comprehensively, source/drain (S/D) electrodes with three geometries including ring, interdigitate and linear structures are employed for the OFET fabrication. The corresponding field-effect mobility, threshold voltage (V_T) and on/off ratio (I_{on}/I_{off}) are summarized in Table 5.1. It is found that almost all monolayer transistors exhibit the saturation mobility over $1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ independent of S/D patterns implying high robustness and good reproducibility of high-mobility FBT-Th₄(1,4) monolayer transistor. An isotropic mobility is illustrated for monolayer transistors with interdigitate and linear S/D patterns, which is in good agreement with the random orientation of FBT-Th₄(1,4) nanofibers. The average values of linear (μ_{lin}) and saturation mobility (μ_{sat}) are 0.90 ± 0.28 and $1.31\pm0.41 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ by testing over 80 devices. In a monolayer transistor, there should be theoretically no difference between transistor operation in linear and saturation regimes, because the monolayer is the only pathway for the charge carriers.^[49-50] However, it is believed that the saturation operation concentrates charge carriers closer to the dielectric and avoids the structural defects on the top of the monolayer to a large extent resulting in a slightly higher mobility than the linear regime. Figure 5.10 c,d shows the μ_{sat} and μ_{lin} distributions, and a maximum value up to $3.02 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ can be achieved for μ_{sat} , which is a new record for organic monolayer transistors. The average threshold voltage is $6.5\pm3.8 \text{ V}$, and the on/off ratio is greater than 10^8 . Such bulk-like transistor performances are attributed to the high crystallinity and strong π - π stacking interaction of the FBT-Th₄(1,4) monolayer.^[27]

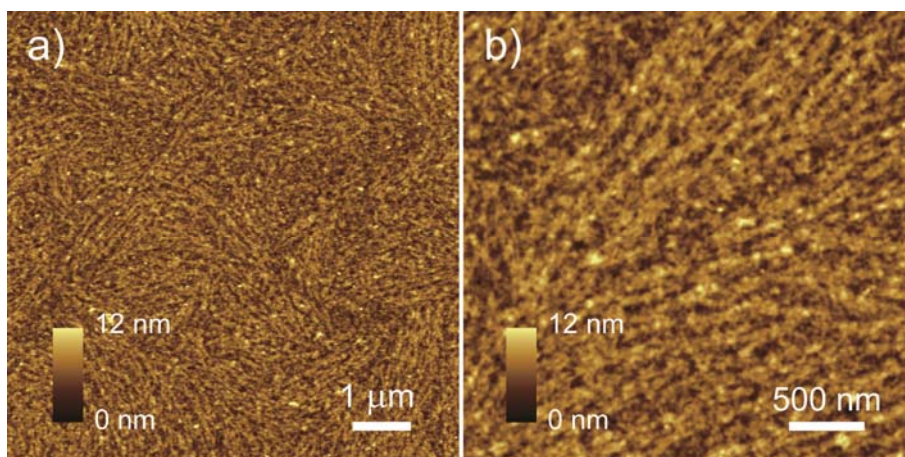


Figure 5.9 AFM height images of FBT-Th₄(1,4) monolayer on surfaces of Au electrodes modified by PFBT SAMs.

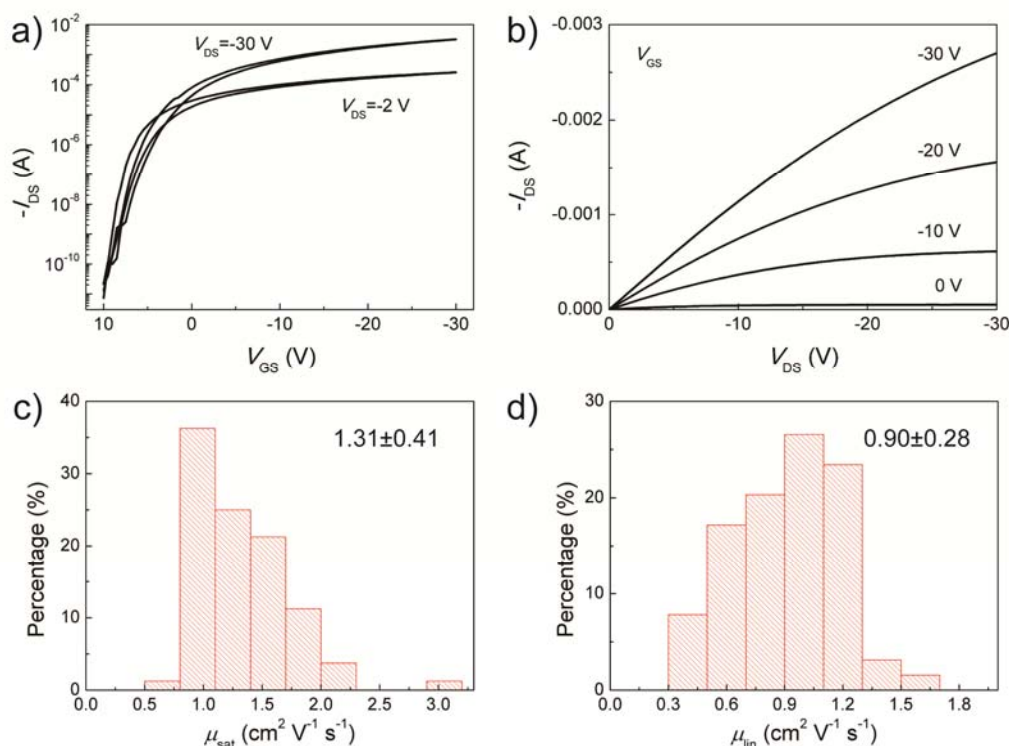


Figure 5.10 a-b) Transfer and output characteristics of a FBT-Th₄(1,4) monolayer ring transistor. The channel length and width are 10 and 2500 μm , respectively. The drain voltages used in a) are -2 and -30 V for the measurement in the linear and saturation regimes, respectively. c-d) The distribution of saturation and linear mobility (μ_{sat} and μ_{lin}) of FBT-Th₄(1,4) monolayer transistor. Over 80 transistors were measured.

It was reported that a single molecular layer of α,ω -DH6T was able to create sufficient conducting channels for charge carriers resulting in a bulk-like performance.^[4] A similar behavior is observed for FBT-Th₄(1,4). It is found that FBT-Th₄(1,4) multilayers dip-coated at 50 $\mu\text{m/s}$ do not further increase but exhibit identical OFET performance to the monolayer with the hole mobility of $\sim 2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. This result demonstrates that the charge carriers are mainly distributed in the first or the first few monolayers adjacent to the dielectric layer dominating the charge carrier transport in OFETs.^[51-52] Up to now, there are only few conjugated polymers such as polythiophenes and their derivatives that can work as high-performance monolayer transistors.^[15, 17, 19, 53] For most conjugated polymers, it is difficult to form a monolayer with well-defined microstructure and high degree of molecular ordering, which can be the reason for the extremely low transistor performance or even no observed field effect. However, the aggregation of FBT-Th₄(1,4) induces strong π - π intermolecular interactions, and a highly crystalline monolayer is grown leading to the bulk-like transistor performance.

Table 5.1 OFET performances of FBT-Th₄(1,4) monolayer transistors with three different geometries of source/drain (S/D) patterns.

S/D patterns	$\mu_{\text{sat}} (\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1})$	$\mu_{\text{lin}} (\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1})$	$V_{\text{T}} (\text{V})$	$I_{\text{on}}/I_{\text{off}}$
ring	1.39±0.48	0.99±0.32	8.7±2.5	10^7 - 10^8
interdigitate	1.17±0.32	0.88±0.20	8.6±2.3	10^7 - 10^8
linear	1.29±0.36	0.57±0.03	3.3±3.4	10^7 - 10^8
average ^{a)}	1.31±0.41	0.90±0.28	6.5±3.8	10^7 - 10^8

^{a)} Over 80 devices were measured.

The channel length (L) of the transistor is found to have a significant influence on the charge carrier mobility, and the mobility as function of L is as shown in Figure 5.11. Two types of ring structures are characterized. In the saturation regime, the value of μ_{sat} linearly increases with increasing the channel length at $L < 4 \mu\text{m}$ (ring

transistor, Figure 5.11 a). Subsequently, the mobility is growing less rapidly and then shows a trend of saturation. Similarly, the increase in channel length leads to the enhancement in linear mobility and then the mobility saturation (ring transistor, Figure 5.11 b). An identical channel-length-dependent mobility is observed for transistors with interdigitate electrodes, as shown in Figure 5.11 c,d. Such behavior can be attributed to the presence of contact resistance. These results demonstrate that the charge carrier transport is homogeneous through the polymer monolayer well correlating with the morphology in Figure 5.2.

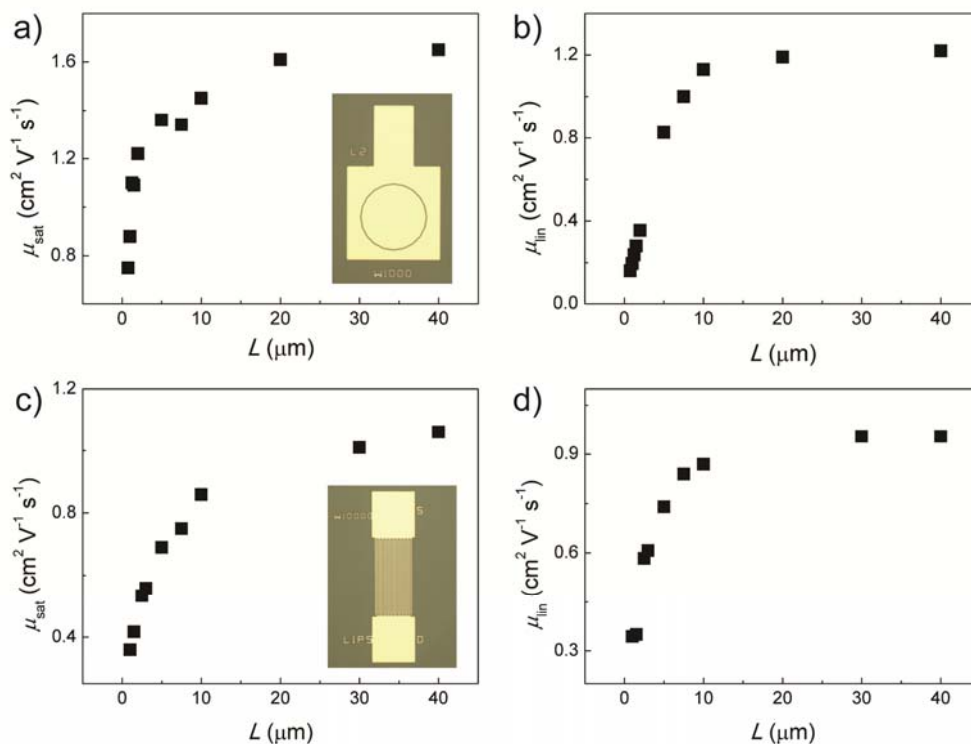


Figure 5.11 The influence of channel length on the saturation (a,c) and linear mobilities (b,d) of FBT-Th₄(1,4) monolayer. Both ring (a,b) and interdigitate transistors (c,d) are analyzed. The channel width is 1000 and 10000 μm for ring and interdigitate transistors, respectively. The insets in a,c) are the optical images of ring and interdigitate transistors.

5.6 Conclusion

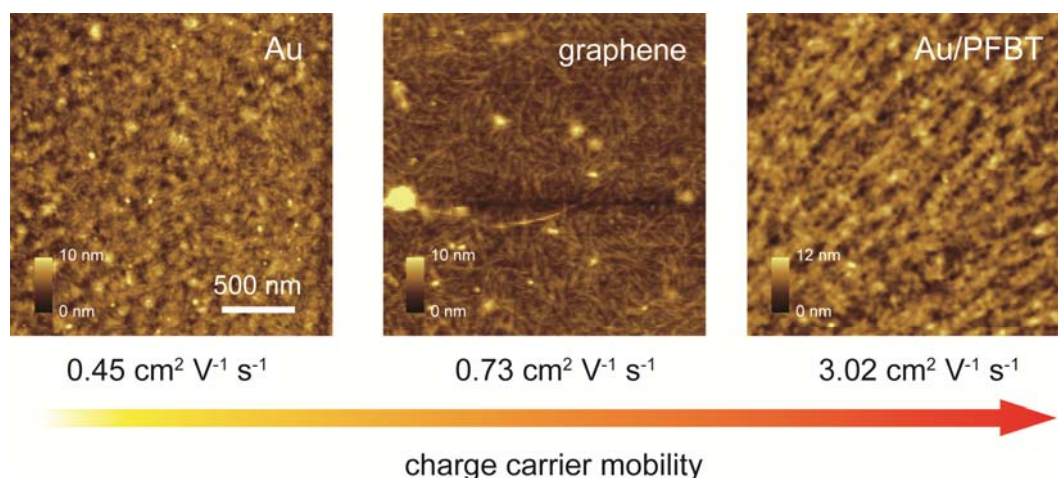


Figure 5.12 Influence of S/D electrodes on the self-assembly and charge carrier transport of FBT-Th₄(1,4) monolayer.

In conclusion, a high-mobility polymer monolayer transistor is fabricated by dip-coating. Three different S/D electrode materials including Au, graphene and Au with PFBT modification are utilized for the fabrication of monolayer transistor in order to investigate the charge carrier transport in polymer monolayer. It is demonstrated that 1) graphene can efficiently improve the compatibility between semiconductor and electrodes resulting in a remarkable enhancement in charge carrier transport from 0.45 to 0.73 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$; 2) Surface modification of Au electrodes with PFBT not only improves semiconductor/electrode compatibility, but also leads to an extraordinary field-effect mobility with the maximum value over 3 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ due to the matched work function. Figure 5.12 clearly exhibits the relationship between the microstructure of organic semiconductors and transistor performance, and the domains with larger size facilitate the charge carrier transport. The field-effect mobility of FBT-Th₄(1,4) monolayer reported in this chapter is the highest for an organic monolayer transistor so far, which can be attributed to the following factors. First, high-molecular-weight FBT-Th₄(1,4) shows an extraordinarily high crystallinity due to its strong aggregation, inducing the formation of an edge-on arrangement with

strong π -stacking intermolecular interactions. Second, the large molecular dimension of this high-molecular-weight polymer is able to interconnect the ordered domains and decrease the density of grain boundary, which is called as the bridging effect.^[22, 54-55] In this way, an efficient conducting channel for charge carriers is created.

In multilayer or bulk film OFETs, the application of a gate voltage generally leads to the accumulation of charge carriers extending a few nanometers from the dielectric interface into the semiconductor,^[56] but it is still possible that the charge carrier transport takes place not on the interfacial layer but on the upper layers in the presence of structural defects, as reported in literature. It is suggested that the charge carrier transport should be considered three-dimensional due to the existence of structural defects,^[57] in good agreement with the conclusion in chapter 3 and 4. This complex situation brings many difficulties to understand the fundamental mechanism of charge carrier transport in both experimental and theoretical studies. However, the high-mobility monolayer transistor presented in this chapter provides a near-ideal platform for such studies, because the charge carriers are confined into the only existed monolayer and their pathways are in two dimensions.

An organic monolayer transistor is a promising candidate in applications of chemical or biological sensors.^[1, 11, 58-59] For instance, an ammonia gas sensor was fabricated based on dithieno[2,3-d;2',3'-d']benzo[1,2-b;4,5-b']dithiophene (DTBDT) monolayer transistors, and an excellent device performance, including high sensitivity, fast response/recovery rate, good selectivity, low concentration detection ability, good reversibility and stability, was observed.^[60] In comparison, the mobility of FBT-Th₄(1,4) monolayer is around one order of magnitude higher than that of DTBDT monolayer implying a better sensor performance. It is reasonable to expect a higher mobility from a FBT-Th₄(1,4) monolayer because of its incomplete coverage, as shown in Figure 5.2c. In principle, experimental parameters such as solvent, solution temperature and dip-coating speed can be optimized in order to increase the monolayer coverage. However, the incomplete coverage of the monolayer can be considered as an advantage, because it exposes more dielectric interface outside. The analyte molecules can be adsorbed at the semiconductor/dielectric interface in an

easier way resulting in a higher response of the monolayer-based sensor. It is believed that high-mobility FBT-Th₄(1,4) monolayer transistor presented in this chapter holds a great potential toward low-cost, fast and portable electronic noses for environmental monitoring, gas detection and sensing for disease diagnosis.^[60-61]

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Chapter 6

Aggregation and Surface Organization of a Difluorobenzothiadiazole-Oligothiophene Copolymer by Solvent Tuning

6.1 Introduction

In chapter 3, the molecular self-assembly of FBT-Th₄(1,4) from mono- to multilayers were precisely controlled by solution processing leading to the formation of well-defined nanofibers. At the same time, chapter 5 demonstrated that the aggregation behavior of this conjugated polymer played a key role in the molecular self-assembly and crystallinity of the polymer monolayer so that an extraordinary high charge carrier mobility was determined in OFETs on the basis of a single molecular layer. The solvent that is utilized to dissolve conjugated polymers is another key element for the aggregation behavior, besides different solution processing methods introduced in chapter 1. For instance, the effective control of the aggregation of poly(N,N-bis-2-octyldodecyl-naphthalene-1,4,5,8-bis-dicarboximide-2,6-diyl-alt-5,5'-2,2'-bithiophene) (P(NDI2OD-T2)) in solution could be realized by using various solvents leading to different domain morphologies and charge carrier mobilities.^[1] Moreover, the aggregate states of poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3,2-b]thiophene) (PBTTT) in both solution and thin films with several

different solvents were characterized by UV-vis absorption.^[2] It was revealed that during film formation the good solvents primarily formed the ordered microstructure but poor solvents generated both ordered and disordered microstructures corresponding to the higher-mobility thin films from good solvents. In addition, the solvent boiling point was found to have a notable effect on the microcrystalline order and field-effect mobility of P3HT thin films.^[3-4]

In spite of these outstanding achievements in microstructure control, it is still a great challenge to adjust the surface orientation of conjugated polymers. As described in chapter 1.3.1, the polymer arrangement in an edge-on fashion with respect to the substrate is generally favorable for the charge carrier transport in transistors. Few reports attempted to realize the transition of polymer packing between face-on and edge-on by the modification of the chemical structure^[5] or molecular weight/regioregularity.^[6] However, such orientation control for a defined polymer is not achieved yet although the arrangement of a bulk-heterojunction thin film consisting of both donor and acceptor semiconductors can be effectively tuned from face-on to edge-on orientation by using a binary solvent mixture.^[7] In this chapter, the polymer surface arrangement in FBT-Th₄(1,4) thin films is successfully tuned from face-on to edge-on by using only a binary solvent mixture (chloroform and 1,2,4-trichlorobenzene) during solution processing. And the solvent-dependent pre-aggregation behavior of FBT-Th₄(1,4) in solution contributes to such orientation transition. More importantly, OFET measurements reveal that FBT-Th₄(1,4) thin films with edge-on molecular orientation exhibit two orders of magnitude higher charge carrier mobility than films with face-on orientation. This result demonstrates that the π - π stacking parallel to the substrate (edge-on) facilitates the charge carrier transport in OFET devices well correlating with literature^[5, 8]. Additionally, this chapter not only proves the possibility to control the polymer surface alignment by solvent tuning, but also reemphasizes the importance of molecular packing for charge carrier transport in OFET devices.

6.2 Pre-Aggregation of Difluorobenzothiadiazole-Oligothiophene Copolymer in a Binary Solvent

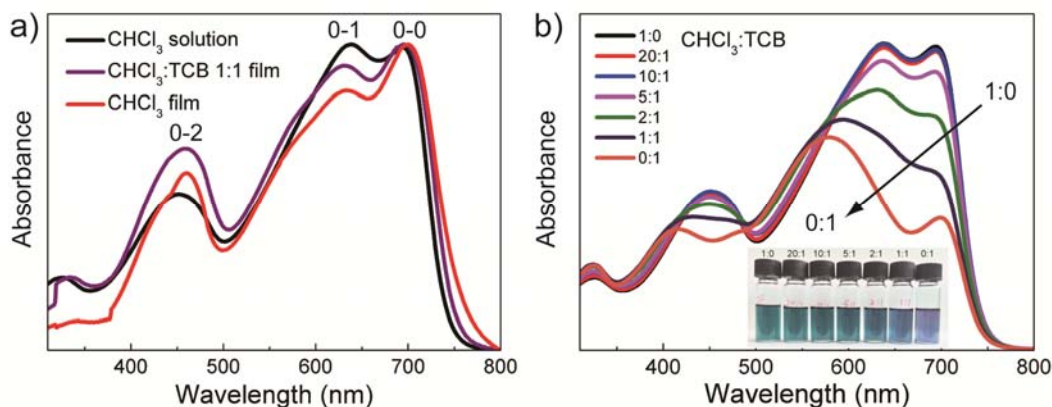


Figure 6.1 a) UV-visible absorption spectra of FBT-Th₄(1,4) thin film and solution with CHCl₃ as solvent. b) Evolution of absorption spectra of FBT-Th₄(1,4) solutions in mixed solvents of CHCl₃ and TCB. The volume ratio of CHCl₃ to TCB ranges from 1:0 to 0:1. The concentration is 1.4 μ M for all solutions. All spectra are measured at RT. The inset shows the solvatochromism effect.

The difluorobenzothiadiazole-oligothiophene copolymer used in this chapter, FBT-Th₄(1,4)^[9-10], is the same as reported in chapter 3. The molecular weight is $M_n=23.2$ K g/mol with $M_w/M_n=1.9$. This polymer is soluble in common solvents such as chloroform (CHCl₃), chlorobenzene, dichlorobenzene and 1,2,4-trichlorobenzene (TCB). FBT-Th₄(1,4) exhibits unexpected strong interchain aggregation in solutions at room temperature (RT),^[9-10] which is confirmed by UV-vis absorption (Figure 6.1a). FBT-Th₄(1,4) thin film drop-cast from a CHCl₃ solution at 1.4 μ M onto quartz substrate shows 0-0 absorption peak at 700 nm and two well-resolved shoulder peaks as 0-1 and 0-2 at 633 and 460 nm, respectively. It is found that a FBT-Th₄(1,4) solution in CHCl₃ shows similar absorption spectra as its film at room temperature indicating established strong aggregates in solution. The absorption of thin films is almost independent of processed solvent. Different from the literature where a warm solution was prepared to separate the aggregation,^[9] this chapter utilizes different

solvents to control the self-assembly of FBT-Th₄(1,4) in solution. Figure 6.1b presents the dependence of absorption on TCB content. With the addition of TCB ranging from 4.8 vol.% (20:1) to 16.7 vol.% (5:1), almost identical spectra are obtained with only slight change in the density ratio of 0-0 and 0-1 peaks. When CHCl₃:TCB reaches 2:1, absorbance of the former 0-1 peak at 638 nm becomes notably weaker, and a new peak at 580 nm appears gradually. With 100 vol.% TCB (0:1), the 0-1 peak disappears completely. The color change of solutions from dark green to dark orchid is indicated in the inset of Figure 6.1b.

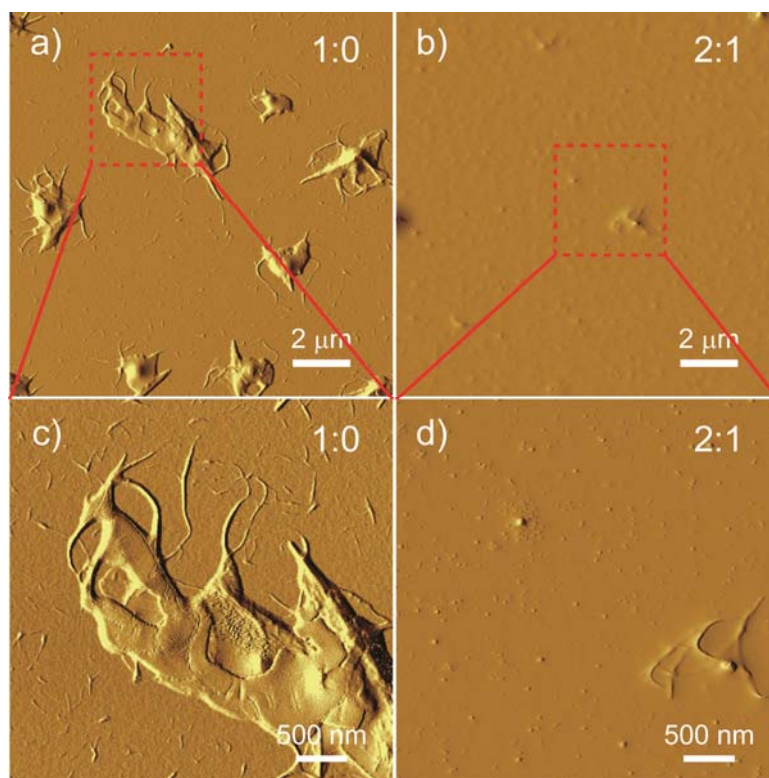


Figure 6.2 AFM amplitude images of FBT-Th₄(1,4) thin films at a very diluted concentration of 5.4 nM. c,d) are the enlarged images of a,b). CHCl₃:TCB is 1:0 and 2:1 for a,c) and b,d), respectively.

To elucidate the impact of FBT-Th₄(1,4) pre-aggregation on the molecular self-assembly in thin films, a very diluted FBT-Th₄(1,4) solution at 5.4 nM is drop-cast on the SiO₂/Si wafer. As shown in Figure 6.2a, several aggregates on a micrometer scale are deposited from CHCl₃ solution well correlated with the strong

pre-aggregation in solution. It has to be emphasized that few well-defined nanofibers are observed on the edge of the aggregates implying a good molecular self-organization. In contrast, the addition of TCB into CHCl_3 solution (CHCl_3 :TCB 2:1) induces the formation of a relatively smooth thin film with the disappearance of well-defined microstructures indicating that TCB efficiently reduces the polymer aggregation and has a significant influence on the self-assembly of FBT- $\text{Th}_4(1,4)$.

6.3 Surface Organization of Difluorobenzothiadiazole-Oligothiophene Copolymer in Thin Films

A systematic study of the influence of TCB on FBT- $\text{Th}_4(1,4)$ self-assembly is performed by drop-casting thin films from solutions with various CHCl_3 :TCB ratios. The substrates (Si/SiO₂ commercial wafers) are functionalized by HMDS SAMs to reduce the density of trapping sites for charge carriers.^[11] Solutions with a concentration of 0.5 mg/mL are utilized for film deposition. During drop-casting, a solvent vapor atmosphere (CHCl_3) is employed for the fine adjustment of the evaporation rate of the solution allowing the formation of well-defined microstructures.^[12-13] Furthermore, solvent vapor effectively minimizes the dewetting effects, and results in the deposition of macroscopically homogenous thin films facilitating the fabrication of OFET devices. Due to the extremely high boiling point of TCB (214.4 °C), the maximum TCB content of 50 vol.% is chosen in this chapter (CHCl_3 :TCB 1:1). At a higher TCB content (50 vol.%), polymer thin films will be dried in more than two weeks. In order to remove residual solvent, thin films are annealed at 100 °C for 30 min under a nitrogen atmosphere. This posttreatment has no impact on the film morphology and molecular ordering.^[9]

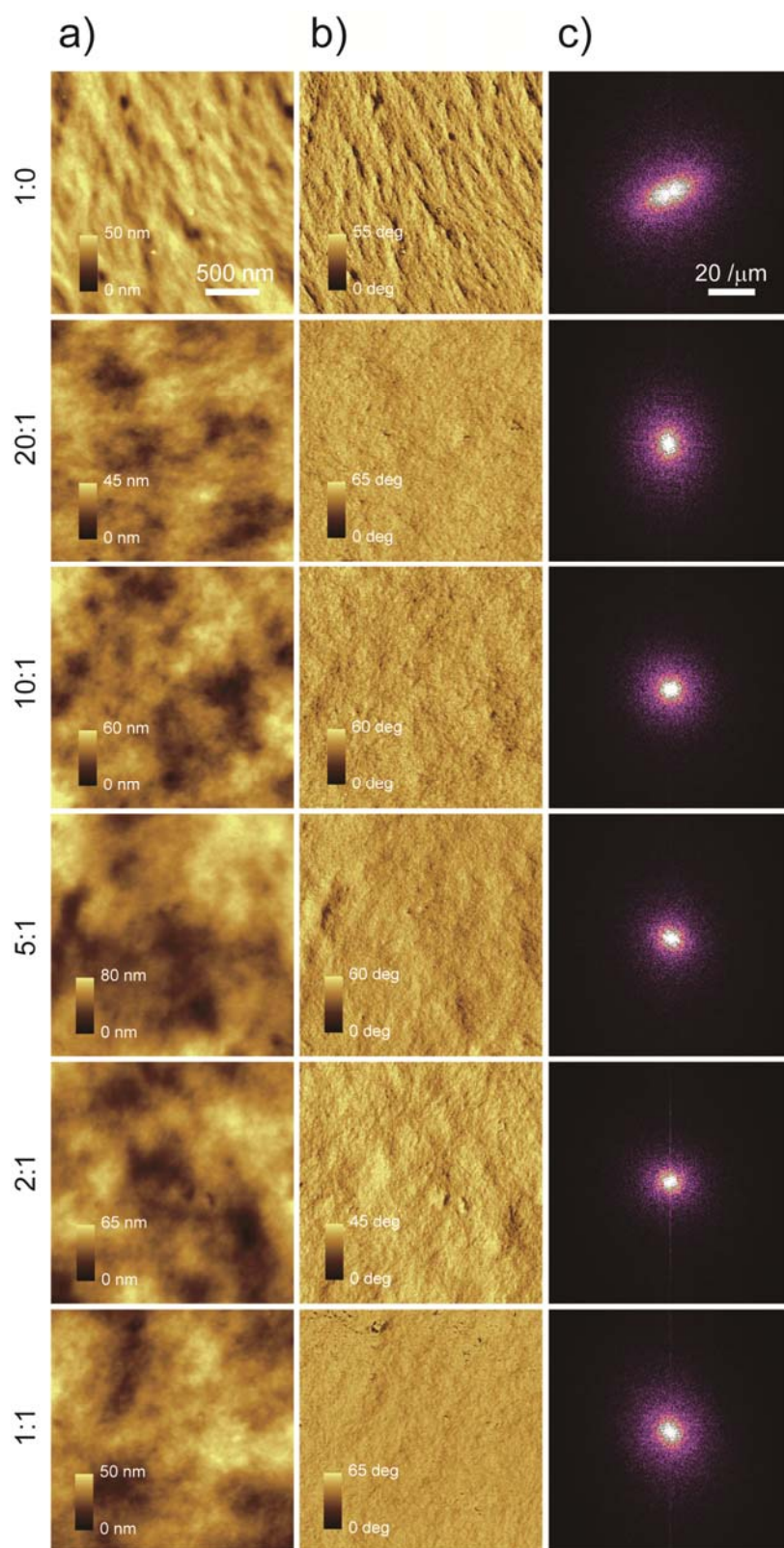


Figure 6.3 AFM height (a) and corresponding phase (b) images of FBT-Th₄(1,4) thin films drop-cast from mixed solvents with different CHCl₃:TCB ratio. c) Corresponding Fast Fourier Transform (FFT) images. All images in a,b) and c) have the same scale bar (500 nm and 20 μm^{-1}).

The topographies of thin films deposited with various CHCl_3 :TCB ratios are characterized by AFM in tapping mode. Figure 6.3 shows the morphology of the polymer thin films after annealing, where the left column are height images and the middle one are phase images. A thin film cast from pure CHCl_3 (1:0) exhibits a clear growth of well-defined microstructures with condensed nanofiber features. Although a small amount of TCB (20:1) has solely minor effect on polymer aggregation in solution (Figure 6.1b), the topography of thin films differs remarkably. The well-defined nanofiber structures disappear but nanofibrillar granules with a lower degree of molecular ordering are formed. It is evident from Figure 6.1b that a further increase in TCB content in mixed solvents effectively avoids the aggregated state in solution, but it must be emphasized that the microstructure of thin films remains almost unchanged. Even at a ratio of CHCl_3 :TCB 1:1, a FBT- $\text{Th}_4(1,4)$ thin film represents an identical morphology to that drop-cast from CHCl_3 :TCB 20:1. The corresponding Fast Fourier Transform (FFT) images in Figure 6.3c indicate that nanofiber structures of thin film from pure CHCl_3 preserve a preferential alignment in comparison with binary mixed solvents. Therefore, it is demonstrated that the addition of TCB into CHCl_3 solution has a crucial effect on the molecular self-assembly of FBT- $\text{Th}_4(1,4)$ in thin films.

Table 6.1 Molecular packing parameters of FBT- $\text{Th}_4(1,4)$ thin films determined by GIWAXS.

CHCl_3 :TCB	molecular orientation	π -stacking distance (nm)	interlayer distance (nm)
1:0	mainly edge-on	0.36	2.45
80:1	face-on	0.36	2.47
40:1	face-on	0.36	2.50
20:1	face-on	0.36	2.50
2:1	face-on	0.36	2.45
1:1	face-on	0.36	2.50

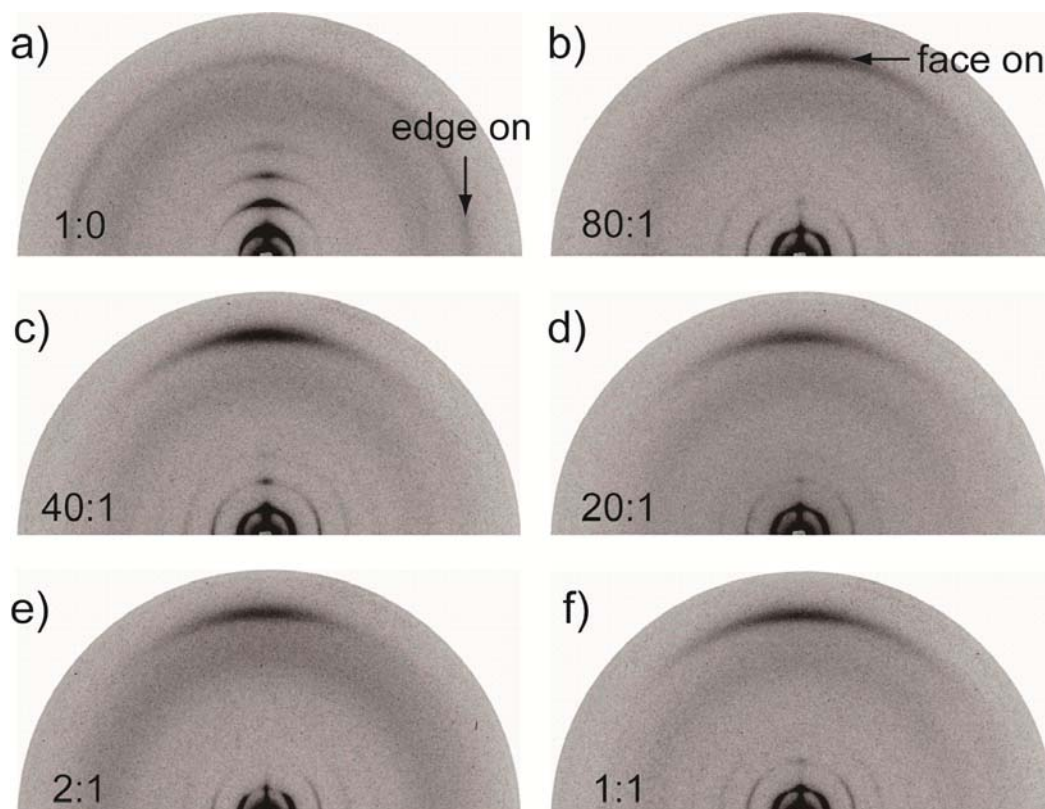


Figure 6.4 GIWAXS patterns of FBT-Th₄(1,4) thin films drop-cast from mixed solvents with different CHCl₃:TCB ratios.

GIWAXS is employed to gain further structural information on the deposited thin films, including cofacial π - π stacking distance, long-range crystalline order and polymer orientation relative to the substrate. It is generally believed that an “edge-on” molecular arrangement leads to a high transistor performance, in which the π - π stacking direction of the molecular backbone is parallel to the substrate facilitating the charge carrier transport in OFETs.^[6] Moreover, a small π - π stacking distance can effectively reduce the energy barrier for interchain hopping of charge carriers facilitating their transport.^[14] For the thin film deposited from pure CHCl₃ (1:0), a π - π spacing peak as a ring arc at $q = 1.75 \text{ \AA}^{-1}$ corresponds to a π -stacking distance of 0.36 nm which is obvious in Figure 6.4 a, indicating that polymer chains are oriented in a hybrid fashion of face-on and edge-on. It has to be noted that the reflection intensity in the direction of in-plane stacking is stronger than out-of-plane stacking implying a majority of edge-on molecular arrangement for 1:0 thin film.

Furthermore, the first order peak at $q_z = 0 \text{ \AA}^{-1}$ and $q_{xy} = 0.26 \text{ \AA}^{-1}$ corresponds to an interlayer distance of 2.45 nm (Figure 6.4 a). On the contrary, the application of the mixed solvent remarkably affects the FBT-Th₄(1,4) self-assembly and leads to the different surface orientation. This is evident from the position of the π -stacking reflection on the meridional plane.^[15] With CHCl₃:TCB 80:1, the π -stacking reflection is located at $q_z = 1.7 \text{ \AA}^{-1}$ and $q_{xy} = 0 \text{ \AA}^{-1}$ suggesting a face-on orientation in spite of the identical π -stacking distance to the thin film from pure CHCl₃ (Figure 6.4 b). On the other hand, a similar interlayer distance with the value of 2.47 nm is obtained (Figure 6.4 b). Interestingly, in the cases of mixed solvents, the FBT-Th₄(1,4) orientation seems independent on the TCB content. When the CHCl₃:TCB ratio varies from 80:1 to 1:1, a face-on arrangement is observed, and both π -stacking distance and interlayer distance remain almost unchanged, as summarized in Table 6.1. It is worth noting that during the film deposition most of chloroform is firstly evaporated due to its much lower boiling point than TCB, even in the case of high CHCl₃:TCB ratio. In other words, at the end of the film formation, a highly concentrated solution appears on the substrate, where the main solvent is probably TCB that dominates the polymer aggregation. As revealed in Figure 1, TCB is able to effectively release the aggregation of FBT-Th₄(1,4) in solution. Therefore, it is reasonable that the addition of TCB causes the same polymer self-assembly and packing in thin films almost independent of the TCB content.

The charge carrier transport of FBT-Th₄(1,4) thin films is investigated by fabricating top-contact bottom-gate OFET devices. Source and drain electrodes with 80 nm in thickness are deposited on the surface of polymer thin films by Au evaporation in vacuum with a shadow mask. The electrical characterizations of the transistors are performed under a nitrogen atmosphere. In this chapter, the field-effect mobility in the saturation regime is characterized. Figure 6.5 shows the transfer and output characteristics of the transistor from pure CHCl₃ (1:0) indicating a classical linear/saturation behavior. It is evident from the transfer curves (Figure 6.5a) that there is basically no negligible hysteresis effect demonstrating that an almost ideal semiconductor/dielectric interface is established due to the application of the surface

modification by HMDS SAMs.^[16] The saturation mobility is extracted from the transfer curves with an average value of $1.57 \pm 0.57 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, and the maximum value reaches $2.15 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Such mobility values are slightly higher than the report,^[9] which can be attributed to the longer-range molecular ordering (nanofibers) and stronger π - π stacking interaction with a preferential edge-on arrangement (Figure 6.4a). On the other hand, the on/off ratio is significantly enhanced to 10^4 - 10^5 , and the threshold voltage is -8 V. Compared with the literature,^[9] both OFET parameters are significantly improved, which can be ascribed to the higher degree of molecular ordering with an edge-on orientation (Figure 6.4 a).

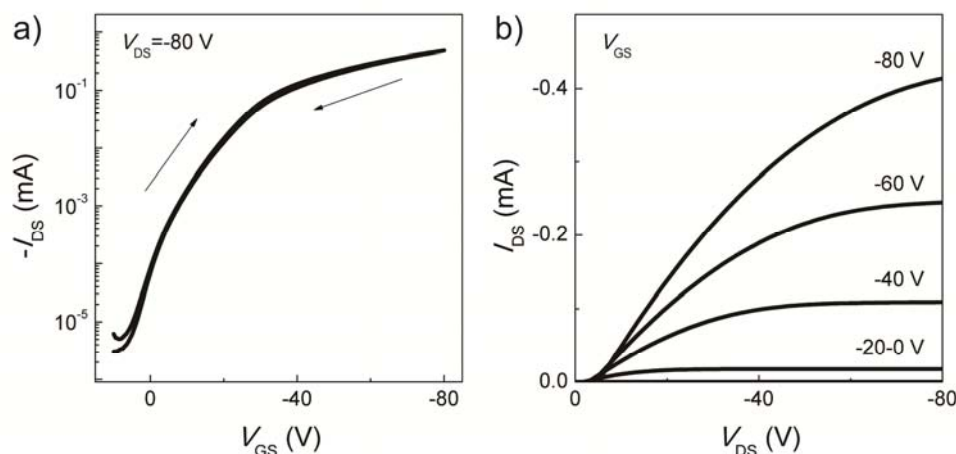


Figure 6.5 Transfer (a) and output (b) characteristics of FBT-Th₄(1,4) thin film transistor deposited from pure CHCl₃ (1:0). In transfer plots, a drain voltage (V_{DS}) of -80 V is applied; in output plots, the drain currents (I_{DS}) reach saturation along V_{DS} at different gate voltages (V_{GS}).

The TCB content has a noticeable impact on the charge carrier transport. Figure 6.6a shows the evolution of transfer characteristics of FBT-Th₄(1,4) thin films with various CHCl₃:TCB ratio. The transfer plots in all cases reflect typical linear/saturation behavior but shift with TCB content in the direction of the applied gate voltage (V_{GS}) indicating a dramatic degradation in charge carrier transport. Representative output plots are present in Figure 6.6 e-f. At $V_{GS} = V_{DS} = -80 \text{ V}$, the value of drain current is dramatically reduced by two orders of magnitude from

4.77×10^{-4} A with 0 vol.% TCB to 4.98×10^{-6} A with 50 vol.% TCB. The corresponding hole mobility as a function of TCB content is shown in Figure 6.6b. With a small amount of TCB (20:1), 20-fold decrease in hole mobility is obtained with the average value of $8.46 \times 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ compared with pure CHCl_3 (1:0). This low mobility based on relatively disordered morphology and face-on arrangement provides more evidence that (i) well-defined microstructures with long-range molecular ordering efficiently reduce the structural defects such as grain boundaries for charge carriers; (ii) the edge-on molecular orientation facilitates the charge carrier transport in OFET devices, in which the direction of π - π stacking interaction is parallel to the conduction channel formed between source and drain electrodes. Starting from 9.1 vol.% (10:1) to 33.3 vol.% (2:1), the hole mobility seems independent of the TCB content, which is in a good agreement with the morphology in Figure 6.3 and polymer arrangement shown in Figure 6.4 and Table 6.1. However, the thin film deposited from CHCl_3 :TCB 1:1 shows a further decrease in transistor performance by one order of magnitude, which may result from the residual TCB solvent still in the film. The threshold voltage (V_T) is also dependent on the TCB content, as shown in Figure 6.6c. A small amount of TCB (20:1) results in the decrease in V_T from -8 to -13 V. Subsequently, the value of V_T is stable ranging from -13 to -14 V until CHCl_3 :TCB is 5:1. The addition of 33.3 vol.% TCB (2:1) slightly reduces V_T to -17 V, but 50 vol.% TCB (1:1) leads to $V_T = -28$ V. As a result, it is demonstrated that the face-on polymer orientation induced by lower aggregation plays a detrimental role in charge carrier transport in OFETs.

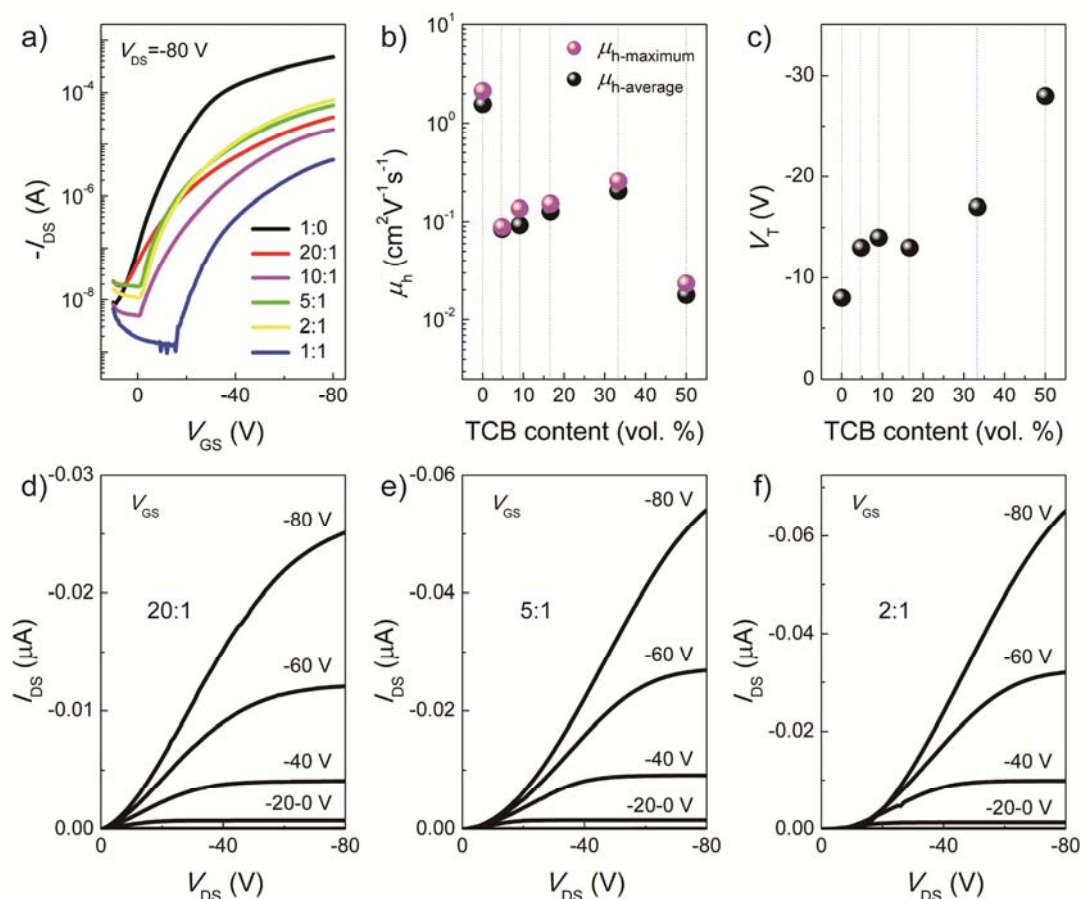


Figure 6.6 a) The evolution of transfer characteristics of FBT-Th₄(1,4) thin films with different CHCl_3 :TCB ratio. $V_{DS} = -80$ V. b) Hole mobility and c) threshold voltage as a function of TCB content in mixed solvents. Over 30 devices are measured. d-e) Representative output characteristics of FBT-Th₄(1,4) thin films with different CHCl_3 :TCB ratios.

6.4 Conclusion

In this chapter, the strong interchain aggregation of FBT-Th₄(1,4) in chloroform solution is confirmed and is in good agreement with chapter 5. In comparison to the literature^[9-10] where warm solution is used to avoid pre-aggregation in solution, this study reveals that the solvent tuning appears to be effective to precisely control the self-assembly of such aggregates. The addition of a high boiling-point solvent, TCB,

effectively releases the FBT-Th₄(1,4) aggregation in solution, as shown in Figure 6.7. More importantly, it is found that the application of TCB critically affects both microstructure and molecular orientation in polymer thin films. The morphology transition from well-defined nanofibers to nanofibrillar granules is observed, even with a small amount of TCB. Furthermore, a face-on arrangement is formed from a preferential edge-on orientation. It was reported that the transition of the polymer orientation could be achieved by modification of the chemical structure^[5] and molecular weight/regioregularity.^[6] Moreover, solvent tuning could only realize the modulation of film microstructure.^[11] However, this chapter enables the control of surface arrangement for a defined polymer by only simply adding another solvent. In the case of pure CHCl₃ as solvent, FBT-Th₄(1,4) thin film exhibits a largely face-on orientation due to the strong pre-aggregation in solution (Figure 6.7). The resultant transistor shows the best device performance with the field-effect mobility of 2.15 cm² V⁻¹ s⁻¹ revealing that the molecular orientation in an edge-on fashion is favorable for the charge carrier transport.^[17]

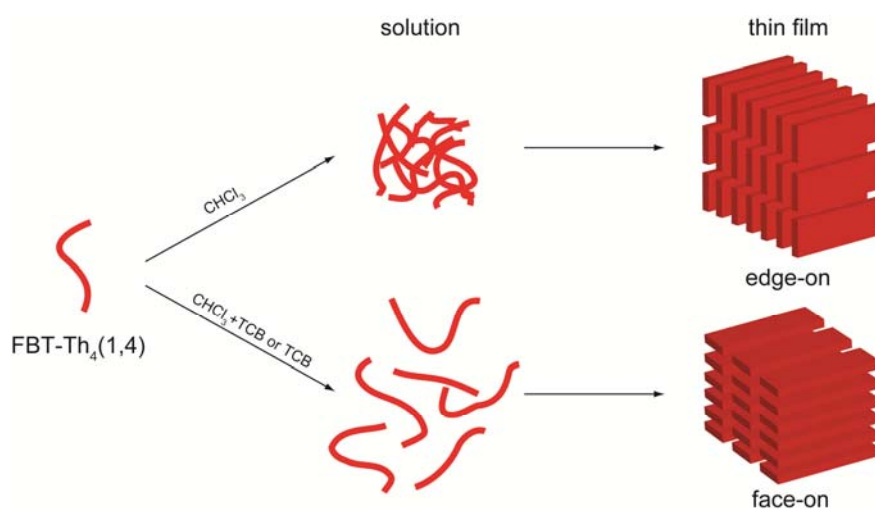


Figure 6.7 Schematic illustration of the control of polymer surface arrangement by solvent tuning.

The solvent tuning method proposed in this chapter employs a low boiling-point CHCl₃ and a high boiling-point TCB as solvents. During the formation of polymer

thin films, it is assumed that most of CHCl_3 is evaporated and then a concentrated solution with TCB as main solvent is formed on the surface of substrate. TCB leads to lower aggregation in solution and subsequently a face-on arrangement of thin films. This is the possible reason why the molecular arrangement is independent of the TCB content in the cases of the binary solvent mixture (Figure 6.7). It was reported that poor solvents such as methanol and water could be also used to induce aggregation, but it has to be emphasized that they usually resulted in inhomogeneous thin films and had detrimental influences on device performance.^[5] This chapter proposes a combination of good solvents with different boiling points to control polymer packing, which is a promising tool to improve charge carrier transport for organic semiconductors.^[1, 18]

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Chapter 7

Alignment of Organic Semiconductor Microstripes by Two-Phase Dip-Coating

7.1 Introduction

In chapter 1, prominent solution-processing approaches are described in detail. In particular, dip-coating is of vital importance due to its precise control over microstructures of organic semiconductors. It is proven that dip-coating is capable of the fabrication of thin films for both conjugated polymers^[1] and small molecules^[2-4]. Furthermore, in chapter 1.4.2, dip-coating was also utilized to investigate the intrinsic role of interfacial microstructure in OFETs. However, it has to be noted that solution processing requires good solubility for the processed conjugated semiconductors to deposit a homogenous thin film. As a benchmark organic semiconductor, pentacene exhibited an extremely high hole mobility of $35 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at room temperature in a single-crystal transistor. However, it is almost impossible to fabricate homogeneous pentacene thin films by solution processing because of its low solubility in common solvents.^[5] Therefore, solution deposition of less-soluble conjugated compounds is still a large challenge limiting the applicability of such systems.

The growth kinetics of conjugated molecules are strongly dependent on many parameters including solvent, concentration, temperature and surfactant.^[6] Surfactants can change the cohesive energy and determine the competition of crystal facet growth

of organic molecules leading to a variety of nanostructures such as micro/nanocrystals and core-shell rods.^[6-8] In this chapter, a novel solution-processing approach, termed as two-phase dip-coating, is proposed to assemble organic semiconductors (especially for the compound with poor solubility) into highly oriented ultrathin microstripes with the assistance of a surfactant.

7.2 Two-Phase Dip-Coating

Two-phase dip-coating employs two immiscible liquids which are a semiconductor solution in an organic solvent and an aqueous surfactant solution. In brief, a droplet of an organic semiconductor solution is firstly dropped onto the surfactant aqueous solution, and dip-coating is then performed resulting in the alignment of ultrathin microstripes. The detailed procedures of two-phase dip-coating are described in chapter 9.2.2. It is found that experimental parameters of two-phase dip-coating including the dip-coating speed, aging time and surfactant concentration play dominant roles in the microstructure of resultant thin films. In this chapter, four different conjugated molecules including both n- and p-type semiconductors are processed by this new method to verify its generality.

7.3 n-Type Organic Semiconductors

5,5'''-Bis(perfluorophenylcarbonyl)-2,2':5',-2'':5'',2'''-quaterthiophene (DFCO-4T, Figure 7.1a) is a high-performance electron-transporting semiconductor, and the corresponding thin film deposited by vacuum sublimation exhibits a field-effect mobility of over $0.51 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[9-10] However, this n-type semiconductor has a poor solubility in common solvents, limiting its processing in solution. The saturated concentration of DFCO-4T in chloroform is only 0.25 mg/mL, and the processing by dip-coating from a DFCO-4T saturated solution leads to a random growth of only very few small crystals on the substrate, as shown in Figure 7.1b. This morphology is found to be independent of the casting conditions. Furthermore, spin-coating causes a

similar result with an average crystal size of around 10 μm . This small dimension does not allow us to fabricate well operating FET devices. Interestingly, two-phase dip-coating approach can by-pass the solubility issue and fabricate well-defined microstructures. 40 μL of saturated DFCO-4T solution is dropped on top of an aqueous surfactant solution (cetyltrimethylammonium bromide (CTAB) as surfactant at a concentration of 0.01 mg/mL). After the chloroform solution has aged for several minutes, ultrathin microstrips can be oriented on a substrate by dip-coating, with the area on the cm^2 scale (Figure 7.1c).

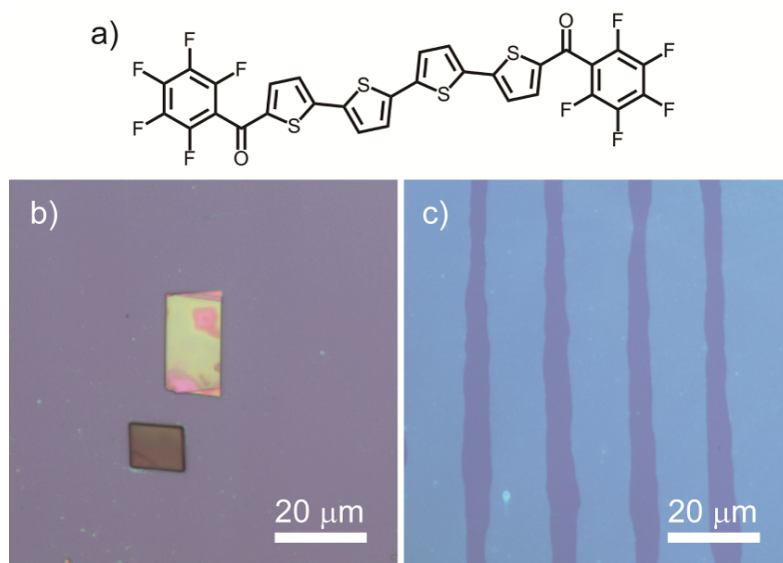


Figure 7.1 a) Chemical structure of DFCO-4T. Optical images of DFCO-4T microstructures fabricated by b) traditional dip-coating and c) two-phase dip-coating.

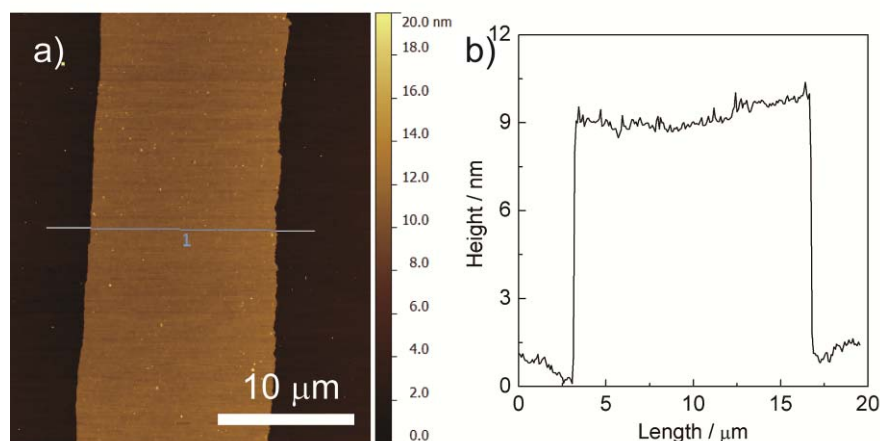


Figure 7.2 a) AFM height image of one single aligned stripe from two-phase dip-coating (line indicates the height plot). b) Height plot for a).

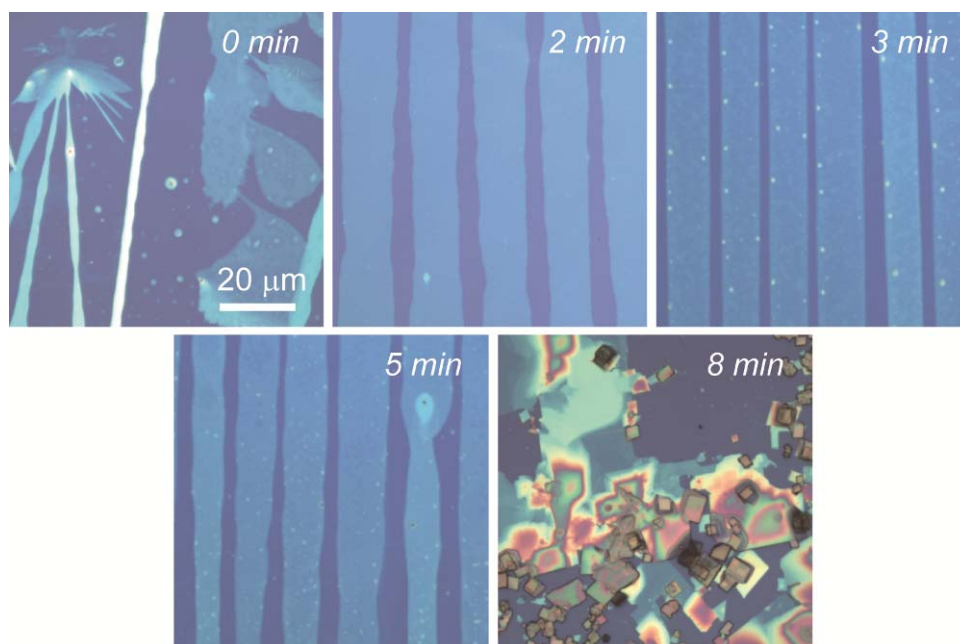


Figure 7.3 Optical images of dip-coated layers of DFCO-4T from the two-phase system at different aging times. All images have the same scale bar. The CTAB concentration is 0.01 mg/mL, and the pulling speed is 10 $\mu\text{m/s}$.

The growth axis of the stripes lies along the pulling direction of dip-coating, and their morphology is characterized by AFM in tapping mode, as shown in Figure 7.2. The stripe width is around 15 μm corresponding to the optical image in Figure 7.1c. The height section of AFM image exhibits the film thickness of around 8 nm (Figure 7.2c). It is worth noting that this pronounced alignment of the organic semiconductor is obtained from ~ 40 μL chloroform and ~ 10 μg DFCO-4T suggesting that two-phase dip-coating is more environmental friendly and lower cost in comparison with traditional solution deposition. In order to align organic semiconductors by two-phase dip-coating, the floating chloroform droplet needs to be aged on the surface of the CTAB aqueous solution for 2–5 min before pulling the substrate. It is found that this aging time critically affects the microstructure of deposited thin films, as shown in Figure 7.3. The immediate dip-coating process after drop-casting of the DFCO-4T solution leads to the growth of only several irregular structures on the substrate (aging=0 min). With the aging time of 2 min, the aligned ultrathin microstripes are formed with high quality. When the semiconductor solution is aged for 5 min, the

morphology of microstrips remains in good alignment, but a few structural defects appear. A too long aging time (for example 8 min) has a significantly negative influence on the self-assembly of conjugated molecules resulting in the growth of an irregular film.

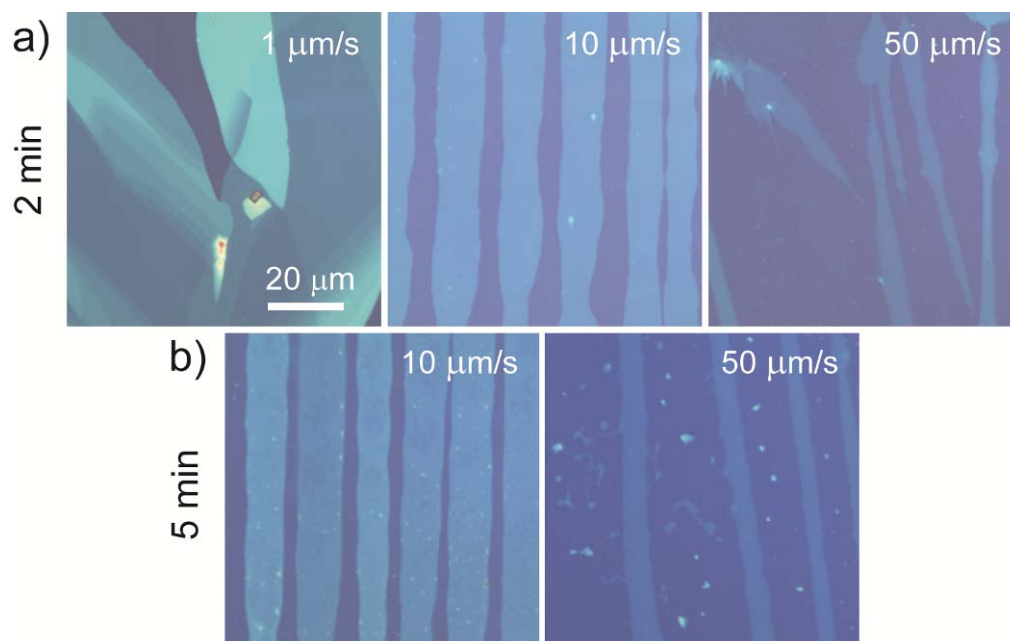


Figure 7.4 Optical images of dip-coated layers of DFCO-4T from the two-phase system at different pulling speeds. All images have the same scale bar. The CTAB concentration is 0.01 mg/mL, and the aging time is 2 and 5 min for a) and b), respectively.

For traditional dip-coating, the pulling speed mainly determines the film thickness or the amount of material deposited on the substrate.^[1] Besides, this parameter is responsible for the formation of the aligned microstrips in the case of two-phase dip-coating. At an aging time of 2 min, more DFCO-4T molecules are deposited on the substrate when decreasing the pulling speed. A low speed such as 1 $\mu\text{m/s}$ causes the formation of multilayers and few small crystals, as shown in Figure 7.4a. On the contrary, a higher pulling speed (50 $\mu\text{m/s}$) results in the deposition of less molecules as well as few random and irregular stripes with smaller size. The optimum speed is 10 $\mu\text{m/s}$, at which uniform microstrips are fabricated in excellent alignment.

The influence of dip-coating speed is also investigated for the aging time of 5 min indicating that a too high speed such as 50 $\mu\text{m/s}$ inhibits the growth of aligned microstripes (Figure 7.4b).

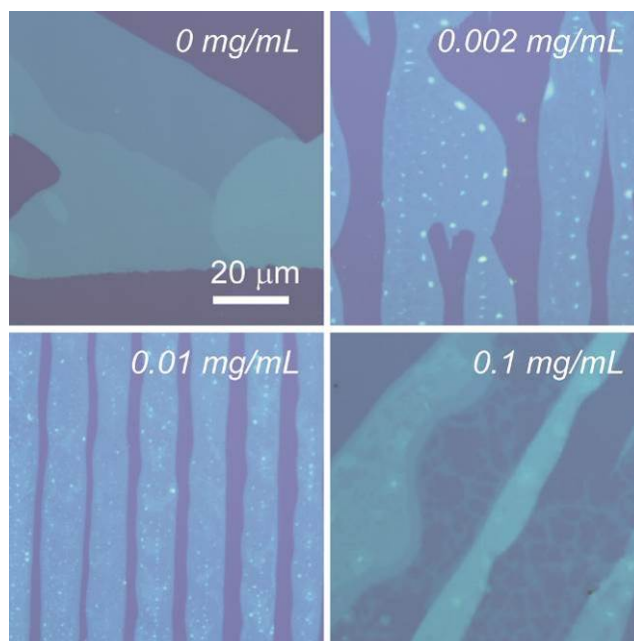


Figure 7.5 Optical images of dip-coated layers of DFCO-4T from the two-phase system at different CTAB concentrations. All images have the same scale bar. The pulling speed is 10 $\mu\text{m/s}$, and the aging time is 2 min.

The surfactant concentration also plays a significant role in the morphology of deposited stripes. Without CTAB (0 mg/mL), DFCO-4T multilayers are observed, as shown in Figure 7.5. The addition of CTAB obviously reduces the dimension of deposited layers and induces the formation of microstripes. At the concentration of 0.002 mg/mL, the alignment of microstripes appears in spite of their irregular shape. An optimum concentration of 0.01 mg/mL CTAB has been identified for the highest degree of alignment of the ultrathin stripes. A higher CTAB concentration, such as 0.1 mg/mL, largely reduces the orientation and leads to inhomogeneous thin layers. On the other hand, an excess amount of surfactant could lead to a strong hysteresis and decrease in charge carrier mobility of the resulting film.^[11]

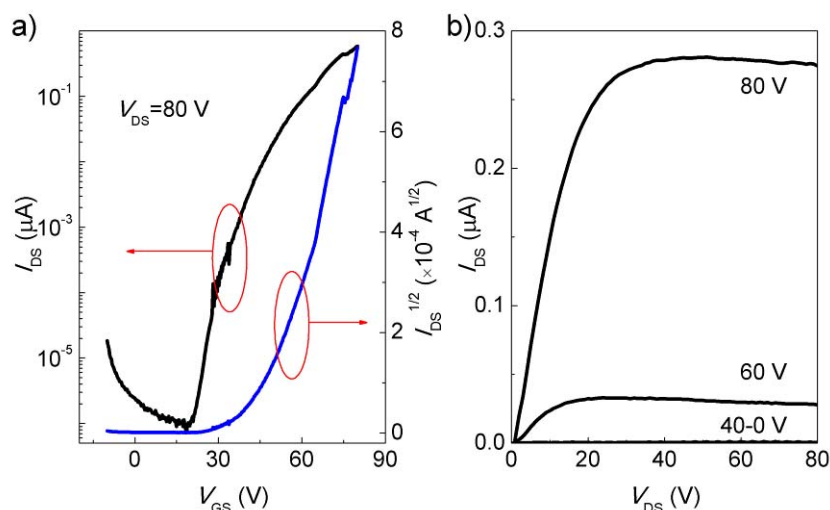


Figure 7.6 The transfer a) and output b) curves of DFCO-4T OFET devices based on aligned stripes. The annealing temperature is 130 °C.

To explore the electrical characteristics, the ultrathin aligned microstrips are deposited under optimum conditions which are: aging time of 2 min, pulling speed of 10 $\mu m/s$, and CTAB concentration of 0.01 mg/mL. A top-contact bottom-gate (TCBG) configuration is employed by evaporating 80-nm-thick Au source and drain electrodes. The electrodes are deposited perpendicular to the axis of microstrips so that the measurements are performed along the orientation direction. It has to be noted that the fabrication of semiconducting layer is performed in air, and water is used to prepare surfactant solution. Both oxygen and moisture are known to have detrimental effects on the charge carrier transport of organic semiconductors.^[12-15] In particular the presence of moisture in the active layer or at the interface with the gate dielectric (especially at the SiO_2 dielectric layer) are important factors responsible for the degradation of the electric performance including decrease in field-effect mobility, current output, threshold-voltage instabilities, and hysteresis effect.^[13-14, 16] The effects of moisture on the charge carrier transport are mainly ascribed to local polarization effects resulting from the large dipole moment of water molecules.^[16] Therefore, the microstrips fabricated by two-phase dip-coating are annealed before and after electrode deposition at temperatures ranging from 100 to 200 °C, which might remove part of the moisture from the interface and bulk enhancing the field-effect

performance. A Keithley 4200-SCS is used for all electrical measurements in a glovebox under nitrogen atmosphere. The transfer and output characteristics of the resultant transistor are shown in Figure 7.6, and a typical linear/saturation behavior is observed. It is evident that this aligned microstripe based device reveals a high transistor performance with the saturation mobility of $0.04 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and on/off ratio of 10^6 . Due to the trapping sites at the SiO_2 interface and contact resistance of the electrodes,^[17-18] the threshold voltage (V_T) is relatively high with the value of $\sim 40 \text{ V}$, but it is still better than literature.^[9-10] The bulk-like transistor performance of the DFCO-4T aligned microstripes demonstrates that the first few monolayers adjacent to the dielectric dominate the charge carrier transport.^[19]

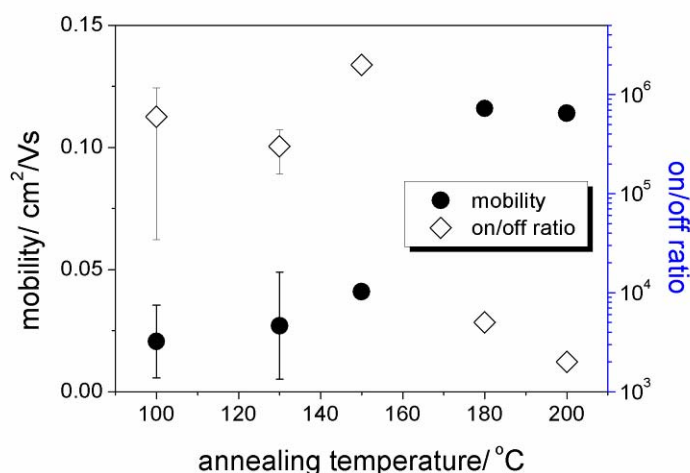


Figure 7.7 Relation between annealing temperature and electron mobility as well as on/off ratio of aligned DFCO-4T microstripes fabricated by two-phase dip-coating.

In addition, the transistor performance is highly dependent on the annealing temperature, as shown in Figure 7.7. As the annealing temperature increases from 100 to 150 °C, the electron mobility is doubled from 0.02 to $0.04 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, while at 180 °C the value jumps to $0.12 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. Above this temperature, the mobility remains almost unchanged. Herein, the maximum temperature used is 200 °C because of the sublimation temperature of DFCO-4T.^[10] On the other hand, at high annealing temperatures (180-200 °C) the on/off ratio of the transistors decreases from around 10^6 to 10^3 - 10^4 due to the increase in off-current.

Table 7.1 Comparison of the experimental details and transistor performance between two-phase dip-coating and Ref. 7.

	Results in Ref. 7		Our results
Deposition methods	Vacuum thermal deposition	Drop-casting	Two-phase dip-coating
Substrate deposition temperature	80 °C	120 °C	Room temperature
Surface modification	HMDS-treated	HMDS-treated	Bare
Film thickness	50 nm	Order of μm	8 nm
Amount of required material	>10 mg	several mg	10 μg
Electron mobility	$0.45\text{--}0.51\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$	$0.21\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$	$0.12\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$

Table 7.1 summarizes the experimental parameters and transistor performance of two-phase dip-coating and literature. In literature, both vacuum thermal deposition and drop-casting were utilized for film deposition.^[10] The substrate temperature was 80–120 °C during film deposition in both cases facilitating the formation of high crystalline films. In order to reduce the trapping sites at the dielectric/semiconductor interface, the dielectric was functionalized by HMDS SAMs. Additionally, thick semiconducting films with the thickness ranging from 50 nm to order of micrometer were fabricated for OFET devices. However, 8-nm-thick microstripes can be assembled onto the nonfunctionalized dielectric in excellent alignment by two-phase dip-coating at room temperature, and the resultant transistors exhibit an identical charge carrier transport to literature. More importantly, for the deposition of semiconducting layer on a cm^2 scale, two-phase dip-coating requires only 10 μg of conjugated molecules, three orders of magnitude lower than literature.

The compact and electron deficient cores of naphthalene diimides (NDIs) and their derivatives make them potential candidates as n-type semiconductors in organic electronics.^[20–23] Extensive investigations demonstrated that the introduction of electron-withdrawing chloro and bromo groups into conjugated cores of NDIs efficiently lowered the lowest unoccupied molecular orbital (LUMO) energy levels generating their air-stability.^[24–27] Recently, an air-stable fluorinated NDI (FNDI, Figure 7.8a) has been reported with an electron mobility of $0.02\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$.^[28]

Although this FNDI has a good solubility in common solvents, the continuous thin films cannot be processed from solutions, because its strong aggregation due to π - π stacking interaction leads to the formation of numerous individual nanocrystals. Therefore, this n-type semiconductor is chosen as the second model compound for two-phase dip-coating.

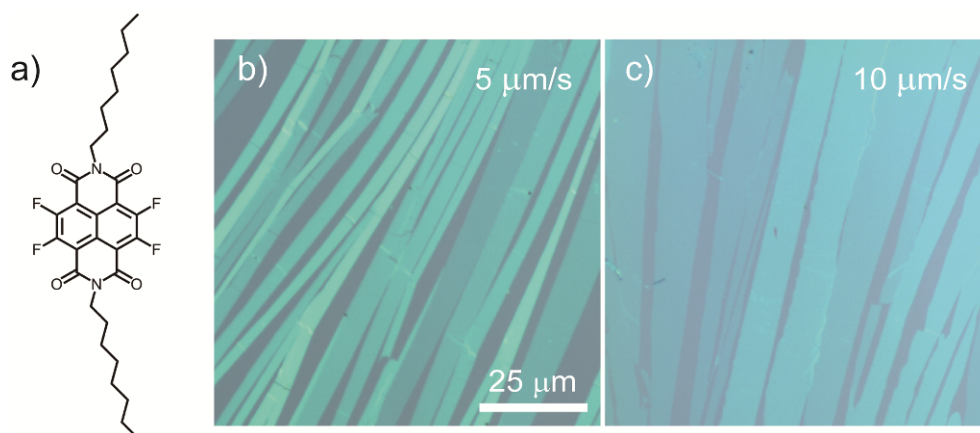


Figure 7.8 a) Chemical structure of the tetrafluoro-substituted NDI used in this section. b-c) Optical images of FNDI microstripes deposited by two-phase dip-coating with different pulling speeds. All images have the same scale bar. FNDI concentration is 1 mg/mL in chloroform, aging time is 2 min and CTAB concentration is 0.01 mg/mL in water.

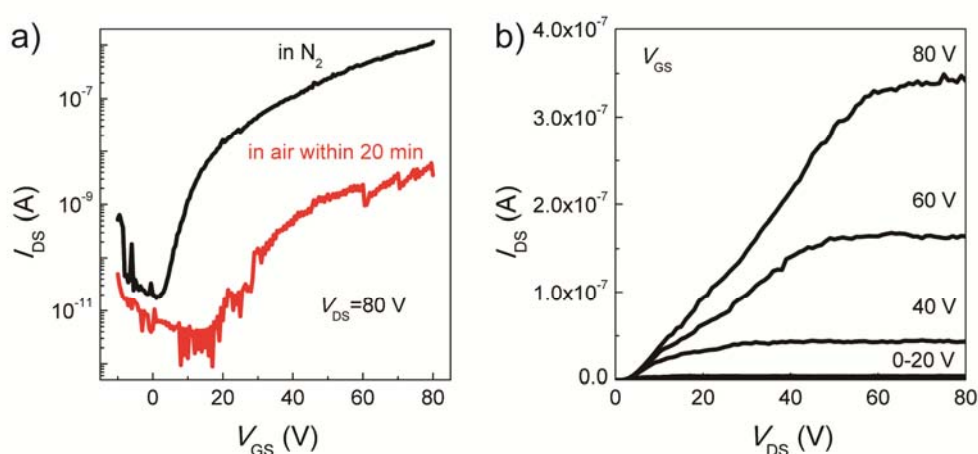


Figure 7.9 a) Transfer and b) output characteristics of FNDI microstripes deposited by two-phase dip-coating. The pulling speed is 5 $\mu\text{m/s}$. The red curve in a) indicates the transfer characteristic measured after exposed in air within 20 min.

A FNDI solution in chloroform at a concentration of 1 mg/mL is prepared for two-phase dip-coating, and a CTAB aqueous solution at a concentration of 0.01 mg/mL is used as base liquid. Similar to DFCO-4T, ~40 μL FNDI solution is firstly dropped on the surface of base liquid and then aged for 2 min. Subsequently, dip-coating is performed with the deposition of ultrathin microstripes in good alignment on the substrate, as shown in Figure 7.8b-c. Two different pulling speeds are employed (5 and 10 $\mu\text{m/s}$), and aligned microstripes appear in both cases. On the basis of FNDI microstripes, OFET device is fabricated with the top-contact bottom-gate device architecture. A typical field-effect behavior is confirmed by the transfer and output characteristics, as shown in Figure 7.9. The electron mobility is extracted from the transfer plots with the value of $3.72 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Moreover, both threshold voltage and on/off ratio are evaluated with the values of 20 V and 10^5 . To explore the air-stability of FNDI microstripes, the transistor is exposed into the air. However, the electron transport is significantly reduced within a short time. Table 7.2 summarizes the transistor performance of FNDI microstripes in different atmospheres. Within 20 min in air, both mobility and on/off ratio are remarkably decreased by two orders of magnitude, and the threshold voltage is increased to 25 V. These results are contradictory with literature^[28] where this FNDI is stable in air. However, the reported transistor was fabricated by vacuum sublimation, and the dielectric was fully covered by the organic semiconductor. In comparison, two-phase dip-coating fabricates partially covered thin films, and oxygen and moisture in air have more chance to contact the semiconductor/dielectric interface and to trap the charge carriers.^[12-15] This is the possible reason for the decrease in transistor performance in air.

Table 7.2 Transistor performance of FNDI microstripes in different atmospheres.

	μ_e ($\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$)	V_T (V)	$I_{\text{on}}/I_{\text{off}}$
In N_2	3.72×10^{-3}	20	10^5
In air	1.39×10^{-5}	25	10^3

μ_e : electron mobility; V_T : threshold voltage; $I_{\text{on}}/I_{\text{off}}$: on/off ratio.

7.4 p-Type Organic Semiconductors

The generality of two-phase dip-coating is further verified by processing p-type organic semiconductors. Dithieno[2,3-d;2',3'-d']benzo[1,2-b;4,5-b']dithiophene (DTBDT) is a high-mobility hole-transporting small molecule. Its highly crystalline thin film fabricated by dip-coating exhibited a remarkable transistor performance with the mobility of $1.7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[29] Furthermore, its single crystal OFET device could reach the mobility as high as $3.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[30] In this section, DTBDT with alkyl chains (DTBDT-C6, Figure 7.10a) is processed by two-phase dip-coating as the first p-type semiconductor.

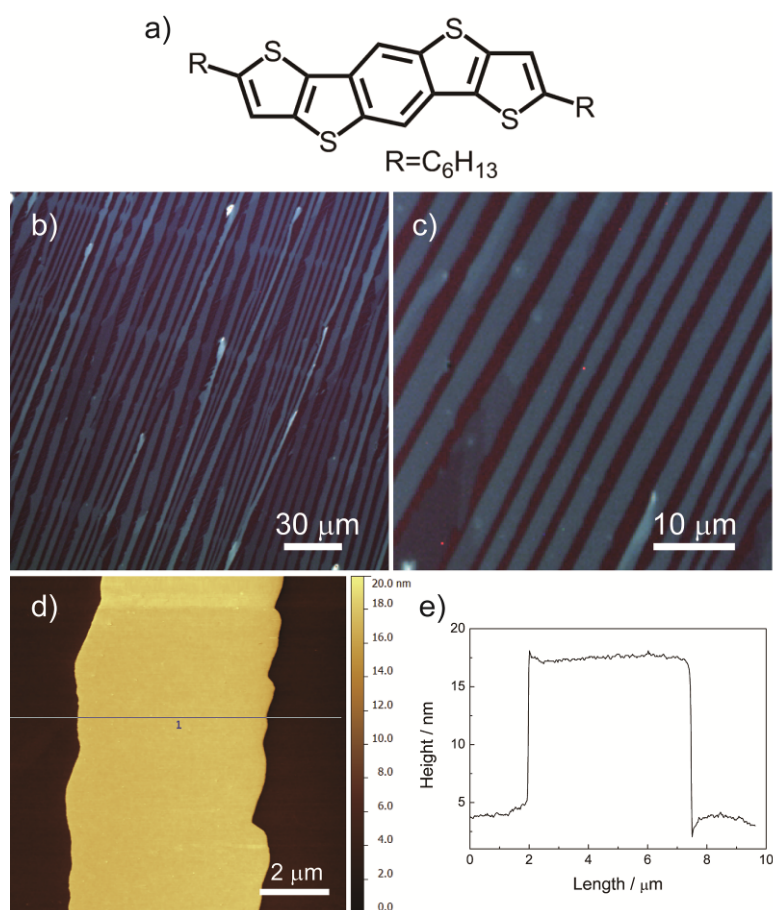


Figure 7.10 a) Chemical structure of DTBDT-C6. b-c) Optical images of DTBDT-C6 aligned microstrips by two-phase dip-coating. d) Height AFM image of one single DTBDT-C6 aligned stripe by two-phase dip-coating (line indicates the height plot). e) Height plot for d). DTBDT-C6 concentration is 1 mg/mL in chloroform, aging time is 2 min and CTAB concentration is 0.01 mg/mL in water.

The exactly same experimental parameters as section 7.3 are used, which are the organic semiconductor solution in chloroform at a concentration of 1 mg/mL, the aging time of 2 min and the CTAB aqueous solution at a concentration of 0.01 mg/mL. It has to be noted that a relatively high pulling speed (100 $\mu\text{m/s}$) is employed for the fabrication of aligned microstripes, because low speeds such as 50 and 10 $\mu\text{m/s}$ lead to the formation of connected branched microstripes or even continuous thin films (Figure 7.11). The morphology of DTBDT-C6 aligned microstripes at 100 $\mu\text{m/s}$ in large area is shown in Figure 7.10b-c. The width of a single stripe is around 5 μm , and the length is up to 1-2 cm. The AFM height image in Figure 7.10d depicts the smooth surface of DTBDT-C6 stripe. A thickness of ~ 12 nm is determined from the height plot of the AFM image corresponding to 6 single molecular layers.^[3-4, 29]

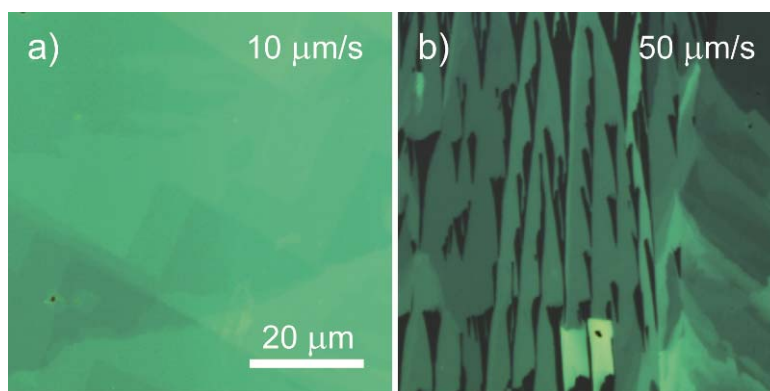


Figure 7.11 Optical images of DTBDT-C6 thin films by two-phase dip-coating at pulling speeds of a) 10 and b) 50 $\mu\text{m/s}$. All images have the same scalebar.

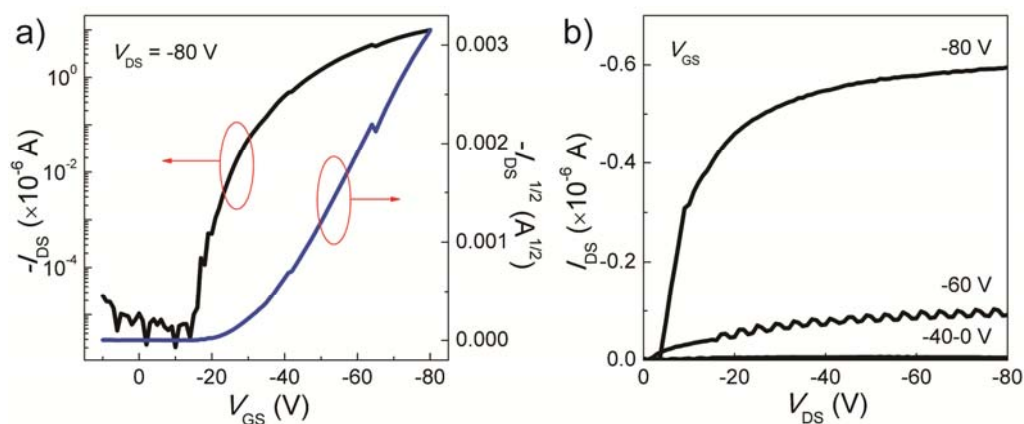


Figure 7.12 The transfer a) and output b) curves of DTBDT-C6 OFET devices based on aligned stripes. The annealing temperature is 115 $^{\circ}\text{C}$.

The charge carrier transport of DTBDT-C6 aligned microstripes is investigated by fabricating top-contact bottom-gate OFET devices. Before electrical measurement an annealing procedure at 115 °C is also carried out. The transfer and output plots in Figures 7.12 indicate a typical linear/saturation behavior, and a saturation mobility of $0.16 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ is extracted with the on/off ratio of 10^6 . Very recently Li et al has reported DTBDT-C6 ultrathin microstripes with around 10 μm in width and with a mobility of $0.1\text{--}0.2 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$.^[4] This mobility value is similar to our results ($0.16 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$), but the width in this chapter is 5 μm , only half as much as the value in literature. This comparison indicates that narrower stripes do not lead to an enhanced charge transport and the potential effect of confinement within this size range can be neglected. Compared with branched microstripes by dip-coating,^[3-4] the aligned stripes by two-phase dip-coating allow the source/drain electrodes to pattern in their perpendicular direction. In this way, the effect of grain boundaries on the charge carrier transport can be minimized, and a better transistor performance can be obtained.

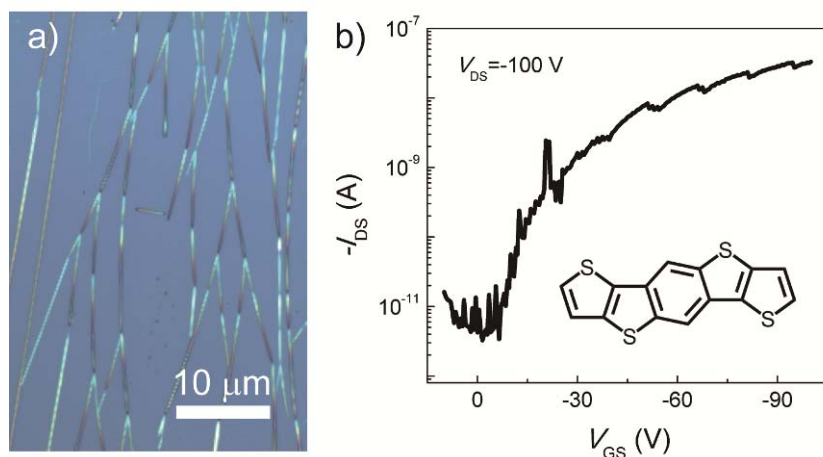


Figure 7.13 a) Optical image of DTBDT-C0 microstripes by two-phase dip-coating. b) The transfer characteristic of resultant transistor. The inset in b) is the chemical structure of DTBDT-C0.

The long alkyl chain of DTBDT-C6 is beneficial for its good solubility. In section 7.3, it is proven that two-phase dip-coating appears to be effective to align semiconductors with poor solubility. Herein, the alkyl chain of DTBDT is

intentionally removed to decrease the solubility, and the corresponding compound is called DTBDT-C0, which is processed by two-phase dip-coating as the second p-type semiconductor. The microstructure of deposited DTBDT-C0 is different from DTBDT-C6, as shown in Figure 7.13a. First of all, the width of stripes is smaller than DTBDT-C6, with the value of only $\sim 1\ \mu\text{m}$. Furthermore, branched microstripes are assembled instead of parallel ones. However, the optimization of experimental parameters is believed to enable the fabrication of parallel microstripes in good alignment. These branched microstripes can also provide efficient pathways for charge carriers to create conducting channel (Figure 7.13b). The top-contact bottom-gate transistor shows a hole mobility of $6.73 \times 10^{-3}\ \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and on/off ratio of 10^4 .

7.5 Proposed Mechanism for Two-Phase Dip-Coating

Molecular self-assembly from solution results from a complex combination of molecule-molecule, molecule-solvent and molecule-substrate interactions.^[31] To obtain a well-defined microstructure, a subtle balance between these interactions has to be achieved. A strong molecule-molecule (i) can generate small aggregates with high degree of molecular ordering, but the aggregation behavior leads to poor solubility, which makes solution processing difficult. Furthermore, a dominant molecule-substrate interaction (iii) will kinetically trap molecules on the substrate surface hindering the intermolecular interactions. In addition, a strong molecule-solvent interaction (ii) is able to effectively shield molecule-molecule interactions resulting in amorphous microstructure during dewetting. However, during two-phase dip-coating proposed in this chapter, a phase-separated system is utilized with the assistance of a surfactant aqueous solution (Figure 7.14). At the interface of the aqueous solution with the semiconductor solution, a certain amount of conjugated molecules are recrystallized to form crystal nuclei. At the same time, some of surfactant in aqueous solution diffuses into the organic semiconductor solution, which is believed to interact with conjugated molecules and change their cohesive energy

(interaction iv).^[6]

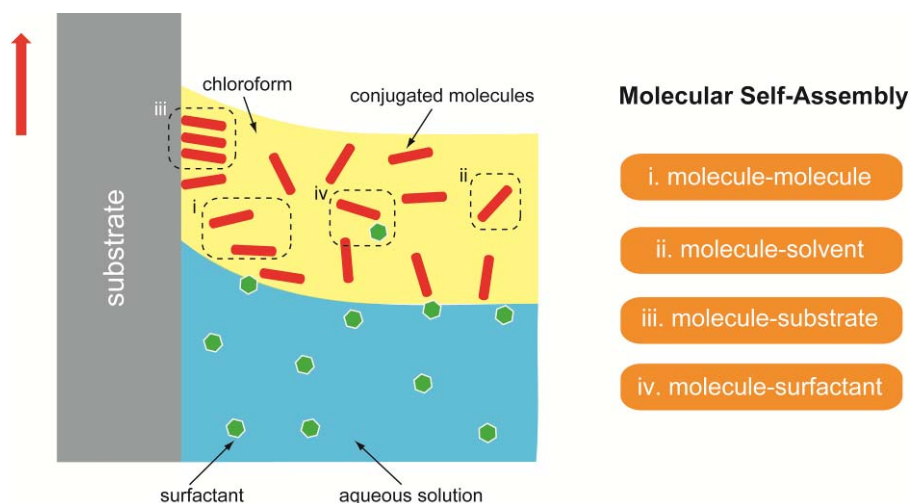


Figure 7.14 Schematic illustration for the proposed mechanism of self-assembly of organic semiconductor microstrips by two-phase dip-coating.

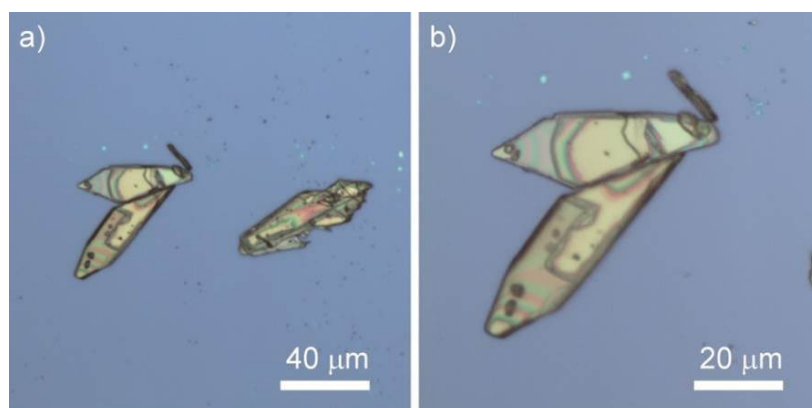


Figure 7.15 The optical images of DFCO-4T crystals by directly dip-coating from chloroform solution with 0.1 mg/mL CTAB. The pulling speed of the substrate is 10 $\mu\text{m/s}$.

To verify the effect of the surfactant, dip-coating is directly performed from DFCO-4T solution in chloroform with CTAB. Different from the rectangular crystals shown in Figure 7.1b (without CTAB), the addition of CTAB results in the formation of diamond-shaped crystals (Figure 7.15). Therefore, two-phase dip-coating combines the conventional dip-coating technique (the driven force for the alignment), the aging procedure (fine control of crystal nuclei size) and the surfactant (modulation of crystal

facet growth) to fabricate aligned thin films. This proposed solution method induces another influencing factor, molecule-surfactant interaction, to tune the self-assembly of organic semiconductors, which could open up a new direction in the field of solution processing.

7.6 Conclusion

To process the organic semiconductors with poor solubility from solution, a new approach, two-phase dip-coating, is developed in this chapter based on the application of a surfactant as an assisting agent and a phase-separated binary liquid mixture. This proposed method appears to be effective to align organic semiconductors into monolayer-scale microstripes, in which the aging time, dip-coating speed, and surfactant concentration play an essential role on the microstructure of deposited thin films. More importantly, it is demonstrated that two-phase dip-coating is a more general method to align organic semiconductors. Firstly, in this chapter, four different types of conjugated molecules including both n- and p-type systems are successfully oriented into ultrathin microstripes by two-phase dip-coating. In spite of the thickness of only ~10 nm (~4 monolayers), the deposited microstripes exhibit a bulk-like transistor performance providing further evidence that only the first few semiconducting monolayers near the dielectric interface are mainly responsible for the charge carrier transport.^[19] Secondly, two-phase dip-coating sufficiently expands the range of application of solution processing, because a good solubility is no more a prerequisite for solution processing any more. Another advantage of two-phase dip-coating is its extremely low consumption of organic semiconductor and solvent exhibiting great potentials in mass production of low-cost flexible organic electronic devices.

In industry, solution processing possesses a great potential in thin film deposition. For instance, the dip-coating process has been commercially utilized for the deposition of thin films such as sol-gel and antireflection layers since the mid of last

century.^[32] However, in many cases, factors such as good solubility are limiting the further development of dip-coating for practical applications of organic electronics. It is believed that the two-phase dip-coating approach can open a new pathway for alignment of conjugated small crystalline molecules by solution-processing independent of molecular solubility.

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Chapter 8

Conclusion and Outlook

8.1 Conclusion

In the present thesis, the precise control of microstructure and molecular ordering of organic semiconducting mono- to multilayers is realized by various processing techniques, especially solution processing, in order to answer: 1) why the molecular self-assembly affects the OFET performance, especially at the interface between the organic semiconductor and dielectric, that is, the mechanism of charge carrier transport in OFETs (chapter 3 and 4); 2) how to control the molecular self-assembly of organic semiconductors (chapter 5 and 6); 3) how to overcome the limitation of traditional solution processing such as the requirement of good solubility (chapter 7). My answers to these three crucial questions are summarized as follows.

The interface between organic semiconductor and dielectric has a key impact on the charge carrier transport in OFETs, where the conducting channel is created by the application of the gate and drain voltages. To elucidate the intrinsic role of the microstructure of the interfacial semiconducting layer in the charge carrier transport, dielectrics with surface roughness within an extremely narrow range from 0.15 to 0.39 nm (chapter 3) are developed in order to control the microstructure of only interfacial semiconducting layer. In the monolayer case, the self-assembly of organic semiconductors is strongly hindered with increasing dielectric roughness leading to

the formation of small domains and subsequently low transistor performance. This is reasonable because the appearance of small domains results in higher density of structural defects or grain boundaries. On the contrary, organic semiconductor multilayers exhibit a substantially lower sensitivity to the sub-nanometer roughness variation in both microstructure and transistor characteristics, so that the roughness dependence is finally eliminated. Three different semiconductor systems, including semicrystalline and amorphous polymers as well as crystalline small molecule, are employed, and an identical trend is observed in all cases. These results demonstrate that the interfacial microstructure only has a negligible impact on the charge carrier transport in organic multilayer transistors. It is assumed that, in spite of the less organized interfacial layer, the upper ones with larger domains can provide the sufficient pathway for charge carriers.

Strong intermolecular π - π stacking interactions usually exist between conjugated molecules, which can trigger intensive molecular aggregation before and/or during processing. In order to exclude the external influence and verify the conclusion in chapter 3, I utilize vacuum sublimation to deposit a p-type semiconductor, α,ω -DH6T, on dielectrics with sub-nm surface roughness in chapter 4. It is evident that an identical trend to chapter 3 is observed in both microstructure and device performance confirming the negligible impact of interfacial microstructure on transistor performance. Considerable achievements in both experiment and theory have been made on the mechanism charge carrier transport.^[1-3] For instance, it was reported that at a certain deposition rate, the first monolayer sustained only a small fraction of drain current, and the upper layers were responsible for the most current, which was explained by the change in charge carrier distribution due to different film growth modes.^[4] However, the spatial inhomogeneity of the semiconducting film due to the difference between semiconductor/dielectric (interfacial layer) and semiconductor/semiconductor (upper layers) interactions was not considered and further investigated. Chapter 4 gives an additional insight into the further understanding of charge carrier transport. Combined with the conclusion of chapters 3, I believe that the variation in charge carrier distribution originates from the lateral

inhomogeneity of the film microstructure. Additionally, in the aspect of practical applications in plastic electronics, the surface roughness of the flexible substrate can be rationally designed and/or treated within the sub-nm range. The increased roughness reduces the molecular ordering at interface without affecting the performance of the whole device, but it appears to be effective to enhance the cohesion/adhesion between the organic semiconductor and the dielectric leading to the fabrication of OFETs with high stability.

Fine control of molecular self-assembly of mono- to multilayer organic semiconductors can be realized by optimizing experimental parameters such as solvent and pulling speed.^[5] Chapter 5 describes that dip-coating allows the fabrication of polymer monolayer with well-defined microstructure of nanofibers. GIWAXS characterization reveals that this polymer monolayer possesses a high crystallinity, which can be attributed to the polymer aggregation. More importantly, the importance of the interface between the organic semiconductor and the metal electrodes is verified, which has a significant influence on the molecular self-assembly and subsequent transistor performance. The optimization of the semiconductor/electrode interface can result in an extraordinary high mobility with the maximum value over $3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ in polymer monolayer transistor. This is a mobility record for organic monolayer transistors. This work, for the first time, realizes a high-performance polymer monolayer transistor with a mobility exceeding that of amorphous silicon exhibiting great potentials in bottom-up integrated circuits with ultrahigh flexibility.^[6] On the other hand, the molecular self-organization on the surface can be precisely modulated by solution processing. In chapter 6, it is revealed that the polymer aggregation strongly depends on the solvent used resulting in the transition of molecular orientation in thin films from edge- to face-on arrangement. It is implied that the choice of solvents might be another efficient way to control the self-assembly of organic semiconductors and subsequently improve the transistor performance. Beyond these achievements of this thesis, graphene, a two-dimensional sheet of carbon atoms, is also a promising candidate to tune the microstructure and molecular ordering of semiconducting layers. Graphene provides an excellent

template for self-assembly of organic semiconductors due to weak organic molecule-graphene interaction and strong chemical bonding interaction.^[7] Also, graphene is a near-ideal material as electrodes contributing to the fabrication of high-performance OFET devices.

Last but not least, traditional solution processing typically requires good solubility of organic semiconductors, and the use of a large amount of organic solvents is harmful to the environment. In chapter 7, a new method, termed as dip-coating, is proposed to align organic semiconductors into ultrathin films. This method is based on the application of a surfactant as an assistant agent and a phase-separated binary liquid mixture. This two-phase dip-coating can be considered as a general technique to process organic semiconductors in solution. In particular, organic compounds with poor solubility can also be aligned into ultrathin films with well-defined microstructure. Another obvious advantage of this method is that only $\sim 10\ \mu\text{g}$ of organic semiconductor and $\sim 40\ \mu\text{L}$ of organic solvent are required to fabricate aligned microstripes with cm^2 area. The resultant thin films with microstripe structures are usually $\sim 10\ \text{nm}$ or even thinner, corresponding to only a few single molecular layers. However, these ultrathin films exhibit good field-effect behavior in OFETs with the mobility comparable to that of bulk films. It is reasonable to expect that this new method is also applicable to conjugated polymers. In particular, I find that the aggregation of polymers is sensitive to the solvent in chapter 6. Therefore, the presence of the base liquid (surfactant aqueous solution) is supposed to play an important role in the self-organization during the deposition of dip-coated polymer thin films in two phases. Furthermore, similar to chapter 6, the tunable mixed solvents can be utilized to dissolve a conjugated polymer, which is then dropped onto the surface of base liquid. In this way, I believe that interesting microstructure and molecular ordering cannot only be obtained but also be controllable.

8.2 Outlook

The scope of this thesis has been centered on the impact of molecular self-assembly on the charge carrier transport in mono- to multilayer OFETs. The findings achieved in this thesis provide a further understanding on the mechanism of charge carrier transport in OFETs, especially at the interface between the organic semiconductor and the gate dielectric. Moreover, this work contributes to a deeper insight into the relationship between the molecular self-assembly and OFET performance, which is beneficial for the fabrication of high-performance OFET devices. Nevertheless, there are still a lot of challenges that should be addressed before the commercialization of OFETs.

In numerous literatures, high mobility values were only reported, but there was no further electrical characterization in a long time that has a higher practical significance. It is often observed that the device performance is gradually reduced after a few weeks or months. It seems to be reasonable that this is originated from the degradation/decomposition of organic semiconductors. However, it has to be noted that in most cases of laboratory research, OFET devices are fabricated, measured and stored under the protection of inert gases such as nitrogen, so compound decomposition seems less possible. Hereby, one interesting arises: is such degradation effect related to the change in microstructure or molecular ordering after long-term storage? Further work is highly encouraged towards this direction.

The next challenge will be to test and optimize OFETs in ambient conditions in order to bring organic electronics further to reality. It is well known that most organic semiconductors are sensitive to oxygen and moisture that could trap charge carriers within the conducting channel in OFETs.^[8-9] Basically, there are two directions to solve this problem. On the one hand, the semiconducting layer can be encapsulated by using, for example, insulating polymers. This seems to be the easiest way. However, it is worth noting that the influence of the encapsulation procedure on microstructure of the semiconducting layer as well as its contact with dielectric should be paid much

attention. Furthermore, the long-term interaction between encapsulation material and organic semiconductor should be also considered because the encapsulation material is likely to diffuse into the organic semiconductor and then affect its molecular ordering. On the other hand, the rational design of air-stable organic semiconductors is another effective way. For instance, several naphthalene diimide based semiconductors exhibited excellent and stable electron transporting behavior even in air, which could be attributed to a large electron affinity and close π - π stacking.^[10-13] In particular, a 2,6-dichloro-naphthalene diimide could be sublimed in air, and the corresponding transistor worked well in ambient conditions with the electron mobility of $3.5\text{--}8.6\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$.^[14] In other words, the realization of air-stable high-performance OFETs also relies on advanced device engineering and rational design of new semiconductor materials.

As mentioned in section 8.1, graphene is an ideal template for the self-assembly of organic semiconductor. Also, it must be emphasized that transistors based on pristine graphene typically show very high charge carrier mobility ($> 10^5\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$, much higher than that of single silicon transistor) in spite of a very low on/off ratio.^[15-16] Therefore, blending organic semiconductor with graphene possesses obvious advantages: 1) improve the molecular self-assembly of organic semiconductor in the active layer; 2) combine the ultrahigh mobility of graphene. It was reported that in comparison to the pristine conjugated polymers such as P3HT and poly(3,3-didodecylquaterthiophene) (PQT-12), the hybrid transistors incorporating graphene exhibited a significant increase in field-effect mobility up to 20 times, while the on/off ratio maintained comparable to or better than what observed without graphene.^[17] Graphene was also able to enhance the device performance of OFETs based on conjugated small molecules. In the case of N,N'-bis(1H,1H-perfluorobutyl)dicyanoperylene-carboxydiimide (PDIF-CN2), the addition of graphene nanoflakes led to an increase in charge carrier mobility by three orders of magnitude, which was proven by both electrical characteristics and time-of-flight photoconductivity measurements.^[18] In addition, graphene owns ambipolar transport property so that it holds a great potential in fabrication of

ambipolar OFETs. P(NDI2OD-T2) is an electron transporting polymer, but the blending of graphene into polymer with the weight ratio $< 1\text{wt.}\%$ resulted in an enhancement in hole mobility by 45 times.^[19] In brief, it is reasonable to expect that incorporating graphene is a promising strategy to control the molecular self-assembly and subsequently enhance the device performance of OFETs. In combination with the investigations on the molecular self-assembly in mono- to multilayer organic semiconductors presented in this thesis, it is believed that the practical OFETs are close to be realized in electronic industry.

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Chapter 9

Experimental Details

9.1 Sub-Nanometer Dielectrics with Sub-Nanometer Surface Roughness

9.1.1 Preparation

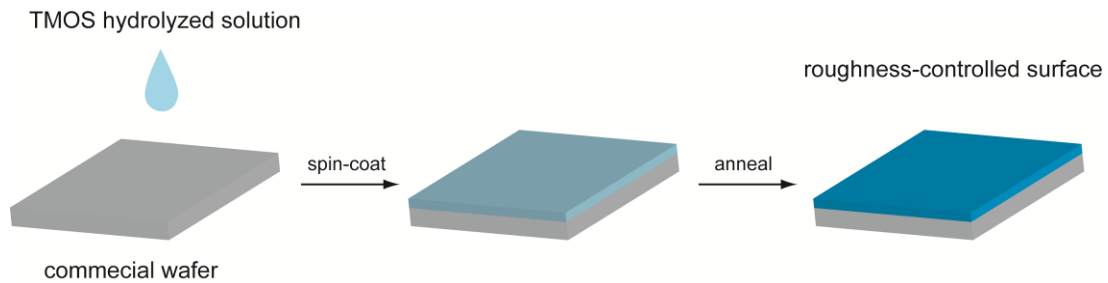


Figure 9.1 Schematic illustration of roughness-controlled surfaces by spin-coating from TMOS hydrolyzed solutions. Heavily doped silicon wafers with 300-nm-thick thermally grown SiO₂ were used as substrates (commercial), and the annealing post-treatment was employed after spin-coating.

Dielectric layers (silica thin film) with roughness of different root-mean-square value (R_{ms}) were prepared using a similar method to that described by Jasieniak et al.^[1] Tetramethyl orthosilicate (TMOS, 2 mL) was mixed with ethanol (2 mL) by stirring for 10 min, subsequently hydrolyzed by gradually adding a solution of H₂O (0.8 mL) and HCl (16 μ L, 2 M) and then heated to 70 °C over 30 min under vigorous stirring.

Afterwards, the heating process was stopped, and the solution was aged for 24 h before use yielding a SILICA solution. The SILICA solution was diluted for 10 times and then spin-coated onto commercial silicon wafers (heavily doped silicon covered with 300-nm-thick thermally grown SiO₂) under the speed of 2000 rpm for 1 min, as shown in Figure 9.1. To remove residual organic impurities, annealing was carried out at 700 °C under nitrogen atmosphere. The resulting spin-coated layer had a R_{ms} value of 0.149 ± 0.006 nm (S1), which was even lower than that of commercial wafers ($R_{\text{ms}} = 0.197 \pm 0.013$ nm).

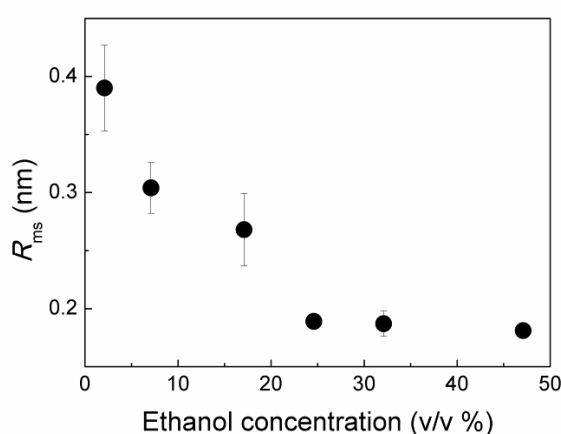


Figure 9.2 The relationship between dielectric surface roughness and ethanol concentration in precursor solution.

Cetyltrimethylammonium bromide (CTAB) was often used as pore-making surfactant for mesoporous silica. Its strong interaction with silica precursors was primarily responsible for the formation and morphology of the final product.^[2] To control the surface roughness of SiO₂, 1 mL of SILICA solution was diluted by 9 mL of H₂O, and then mixed with 10 mL of 2 mg/mL CTAB solution (H₂O). Subsequently, the same spin-coating procedure was performed. For the diluted SILICA solution with CTAB, it was found that the addition of ethanol could precisely control the surface roughness of spin-coated layer. It had to be noted that both TMOS and CTAB contents remained unchanged in all cases. Figure 9.2 showed that the surface roughness of spin-coated SiO₂ was strongly dependent on the ethanol concentration with R_{ms} values ranging from 0.187 ± 0.011 to 0.390 ± 0.037 nm (S2-S5).

9.1.2 Characterizations

Morphologies of prepared silicon oxide layers were firstly characterized by a Dimension Icon FS Atomic Force Microscopy (AFM) in tapping mode. The height AFM images were used to evaluate the surface roughness. The measured surface could be imagined as a two-dimensional function $z(x,y)$. For a given AFM height image, measurement sampled this function at discrete points. Thus a matrix of heights $z_{i,j}$ was obtained, where $i = 0, 1, 2, \dots, N-1$ and $j = 0, 1, 2, \dots, M-1$. It was assumed that the mean value was zero, that was,

$$\sum_{i=0}^{N-1} \sum_{j=0}^{M-1} z_{i,j} = 0 \quad (9.1)$$

Thus the root-mean-square surface roughness (R_{ms}) could be given by

$$R_{ms} = \left[\frac{1}{MN} \sum_{i=0}^{N-1} \sum_{j=0}^{M-1} z_{i,j}^2 \right]^{1/2} \quad (9.2)$$

Kurtosis coefficient (R_{ku}) was the fourth central moment of distribution of heights describing the sharp spikes or cracks. The definition was as follows.

$$R_{ku} = \frac{1}{MN R_{ms}^4} \left(\sum_{i=0}^{N-1} \sum_{j=0}^{M-1} z_{i,j}^4 \right) \quad (9.3)$$

All values of R_{ms} and R_{ku} were analyzed by using a Gwyddion software.

The element components were determined by an energy-dispersive X-ray spectroscopy (EDX, Bruker) for prepared dielectrics. Besides, the corresponding surface properties were also characterized by a contact angle measuring system (DSA10-MK2, Kruss), where 3 μL of H_2O was utilized for the measurement.

9.2 Solution Processing

9.2.1 Dip-Coating

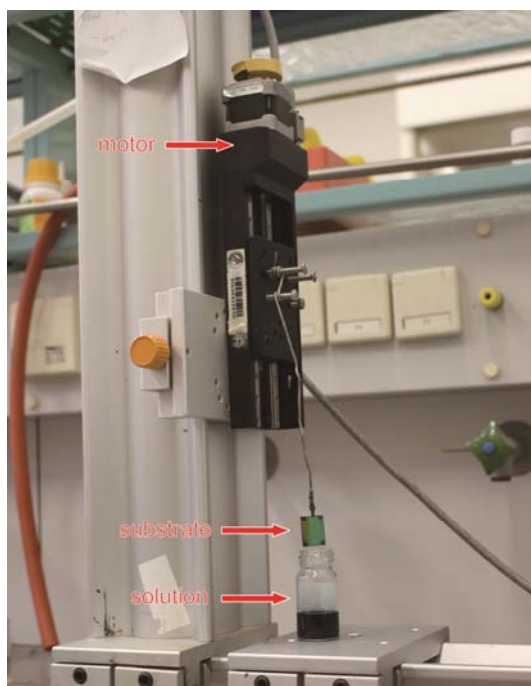


Figure 9.3 Photograph of dip-coating setup.

Dip-coating started from the preparation of organic semiconductor solution in an open glass vial. A high-precision linear motor was used to control the dip-coating speed ranging from 1 $\mu\text{m/s}$ to 2 mm/s , as shown in Figure 9.3. The substrate connected with the motor was firstly immersed into the organic semiconductor solution, and then was withdrawn slowly out of the solution. Due to the solvent evaporation, a thin film of the organic semiconductor was deposited on the surface of the substrate. The whole process was performed in ambient conditions at room temperature ($\sim 23^\circ\text{C}$).

9.2.2 Two-Phase Dip-Coating

A two-phase system was utilized for two-phase dip-coating, as shown in Figure 9.4. The surfactant, cetyltrimethylammonium bromide (CTAB, Alfa), was dissolved in

ultrapure water (Milli-Q). Heavily doped silicon wafers with a thermally grown silicon dioxide layer with the thickness of 300 nm were used as substrates. Before film deposition, substrates were firstly cleaned via ultrasonication in acetone for 10 min, followed by sonication in isopropanol for 10 min. 10 mL CTAB solution was injected into a 20 mL glass bottle as base liquid. Then a droplet ($\sim 40 \mu\text{L}$) of organic semiconductor solution in chloroform was dropped onto the surface of surfactant aqueous solution. Although chloroform was immiscible with water, and its density (1.48 g/mL) was larger than that of water (1 g/mL), the chloroform solution floated on the surface of the aqueous surfactant solution due to the surface tension of water (Figure 9.4 d). After this two-phase system was aged for a few minutes, the dip-coating was processed by using cleaned substrates. Consequently, the aligned ultrathin microstrips were deposited with the area over cm^2 (Figure 9.4 e).

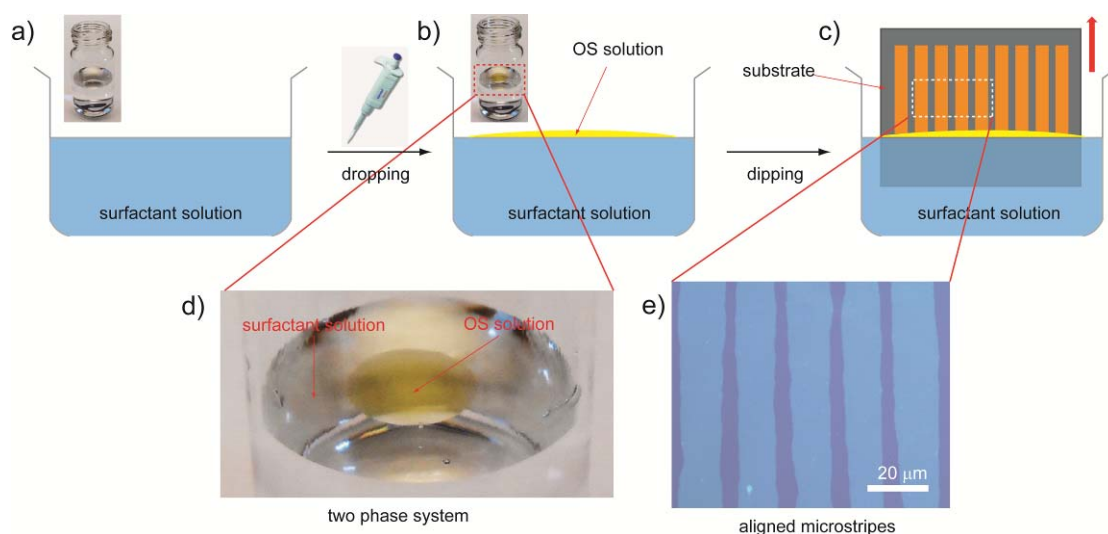


Figure 9.4 a-c) Schematic illustration of two-phase dip-coating technique. A droplet of organic semiconductor (OS) solution was drop-cast onto the surface of surfactant solution, and then a substrate was dipped from this two phase system. The insets in a-b) are the photographs of surfactant and semiconductor/surfactant solutions, respectively. d) The enlarge images of the inset in b). e) The optical image of aligned ultrathin microstrips by two-phase dip-coating.

9.3 Characterizations for Organic Semiconductors

9.3.1 AFM

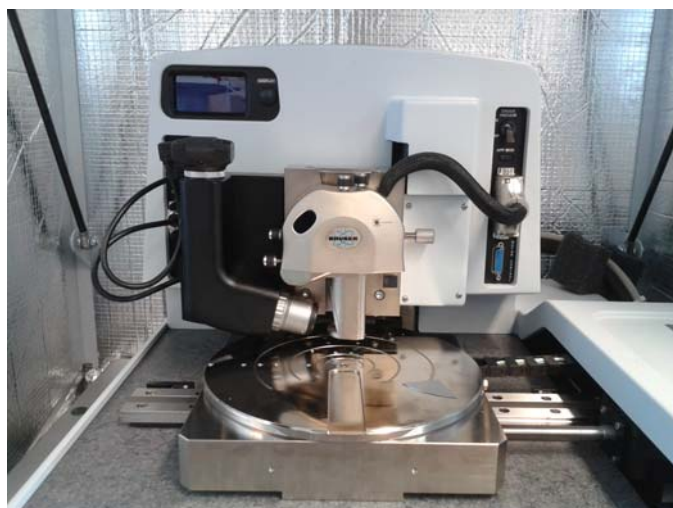


Figure 9.5 Dimension Icon FS AFM setup.

Atomic force microscopy (AFM) was one kind of scanning probe microscopies (SPM) that were designed to explore the local surface properties, such as height, friction, magnetism, with a probe. To acquire an image, a small area of the sample on a micrometer and/or nanometer scale was usually scanned. AFM was operated by measuring the force between a sharp probe and the sample, where the vertical and lateral deflections of the cantilever were measured by an optical lever with the assistance of a position-sensitive photo-detector. There were basically two AFM imaging modes. In a contact mode, the distance between tip and sample was only a few angstroms so that a very strong repulsive force appeared between the tip and sample atoms, which was attributed to the overlap of the electronic orbitals at atomic distance. In contrast, a non-contact mode applied a larger tip-sample distance, and the cantilever was oscillated instead, where van der Waals forces dominated. In comparison, the tapping mode took the advantages of the contact and non-contact modes, and provided higher resolution. On the one hand, it eliminated frictional forces when contacting the surface. On the other hand, it prevented the tip from being

trapped by adhesive meniscus forces from the contaminant layer. In this thesis, all AFM measurements for organic semiconductors were carried out by a Dimension Icon FS setup in tapping mode (Figure 9.5), and the corresponding height images were mainly utilized to investigate the morphological information. Generally, the scanning size was $10 \times 10 \mu\text{m}^2$ or smaller.

9.3.2 TEM and SAED

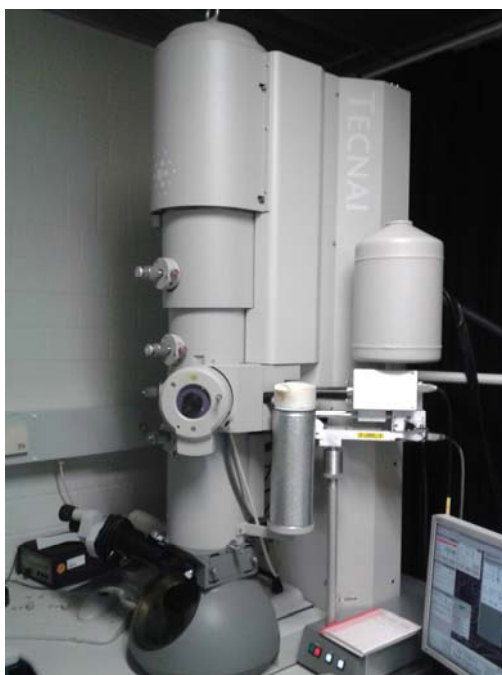


Figure 9.6 FEI Tecnai F20 TEM setup.

Transmission electron microscopy (TEM) was able to provide detailed morphological information of extremely small objects or areas of objects by passing a beam of electrons through a very thin sample. TEM used electrons as “light source” and its basic principles were similar to that of the light microscopy. An electron beam was generated from the “electron gun” by emitting from a cathode and then accelerating through an anode. Afterward, the electrons passed through an aperture into the vacuum tube, where electromagnetic lenses were used to direct the electron beam through the centre of the tube to a very thin sample. Depending on how they were affected by the sample, electrons continued down the tube with a certain energy

and reached an image plane such as a fluorescent screen. Eventually, an image was recorded by a CCD camera.

During TEM measurement, it was possible to obtain electron diffraction patterns from the sample under observation. Diffraction patterns were able to provide structural details related to the sample's orientation, polytype, phase and defect morphology, which were an excellent complement to x-ray diffraction data. In such measurement, one could choose any part of the sample to get the diffraction pattern, which was called selected area electron diffraction (SAED). Bragg's Law was a very useful physical picture of the diffraction process because the diffracting planes appeared to behave as mirrors for the incident electron beam. The corresponding equation was as follows.

$$n\lambda = 2d \sin \theta \quad (9.4)$$

which described the reflection of a plane wave (wavelength λ) incident at an angle θ to atomic planes of spacing d .

In chapter 3, the morphology of crystalline ultrathin films were determined by a FEI Tecnai F20 TEM at 200 kV under liquid nitrogen cryoconditions, and SAED was recorded by using a Philips CM 12 electron microscopy.

9.3.3 GIWAXS

Grazing incidence wide angle X-ray scattering (GIWAXS) was a scattering technique for the investigation of film morphology and the nanostructure of thin films, especially for organic semiconductors.^[3] Compared with specular diffraction that described the periodicity out of the substrate plane (Figure 9.7 A), GIWAXS applied a grazing incident angle, α , that is below the critical angle of the substrate (Figure 9.7 B,C), and the diffracting lattice planes were perpendicular to the sample plane when the scattering vector pointed along the sample plane.^[4] An area or plate detector setup allowed for rapid data collection over a large range of scattering angles (Figure 9.7 C).^[4]

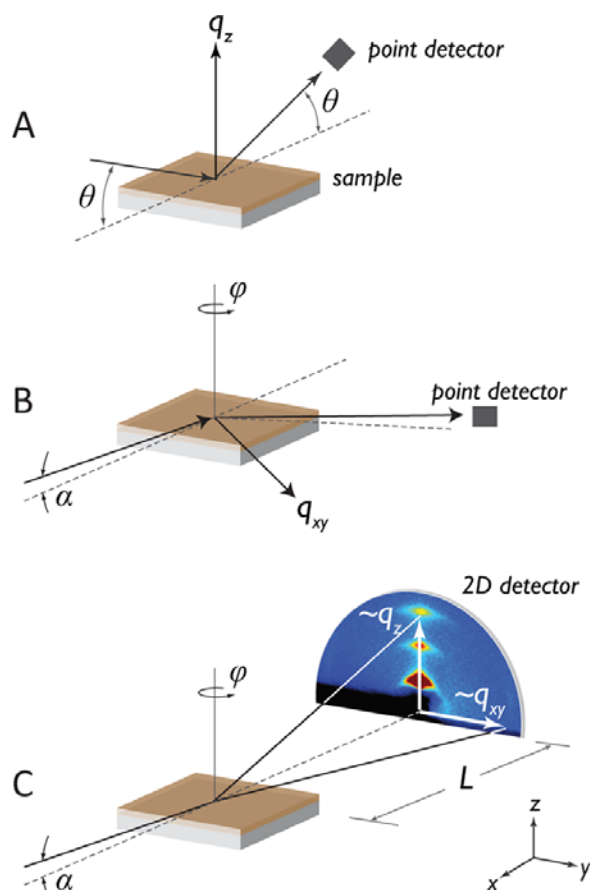


Figure 9.7 Wide-angle X-ray scattering geometries on thin films. (A) Specular diffraction. (B) Grazing incidence wide-angle X-ray diffraction (GIXD) with a point detector. α was the incidence angle and θ was an in-plane, azimuthal, rotation. (C) Grazing incidence X-ray scattering (GIXS) with a 2D image plate.^[4]

In this thesis, GIWAXS experiments were performed by means of a solid anode X-ray tube (Siemens Kristalloflex X-ray source, copper anode X-ray tube operated at 35 kV and 40 mA). Osmic confocal MaxFlux optics, X-ray beam with pinhole collimation, and a MAR345 image plate detector. The beam size was 0.5×0.5 mm, and samples were irradiated just below the critical angle for total reflection with respect to the incoming X-ray beam ($\sim 0.18^\circ$).

9.3.4 Others

In chapters 5 and 6, UV-vis-NIR absorption spectra were measured on a

PerkinElmer Lambda 9 spectrophotometer at room temperature. In chapter 7, the morphology of organic semiconductor microstripes was characterized by a Zeiss Axiophoto optical microscopy (OM) equipped with a Hitachi KP-D50 color digital CCD camera. The number-average molecular weights and polydispersity index of conjugated polymers were determined by a gel permeation chromatography (GPC) equipped with a refractive index detector running in 1,2,4-trichlorobenzene at 135 °C using a PLgel MIXED-B column calibrated against polystyrene standards.

9.4 OFET Fabrication

9.4.1 Cleaning Substrates

The heavily doped silicon wafers with a 300 nm-thick thermal oxide layer were used as substrates, which were cleaned by 10 min ultrasonication in acetone and subsequent 10 min ultrasonication in isopropyl alcohol.

9.4.2 Electrode Deposition

For the deposition of Au source and drain electrodes, the shadow masks were fixed onto the cleaned substrates with or without semiconducting layers, and then put into the vacuum evaporation system. Subsequently, the shutter was closed and the whole system was vacuumed. A quartz crystal microbalance was employed to in situ monitor the thickness of Au electrodes. In chapters 3, 4, 6 and 7, the thickness of Au electrodes were 60-80 nm. It was worth pointing out that the substrates with pre-patterned Au electrodes (50 nm in thickness) were used in chapter 5, which were purchased from BASF and Philips.

In chapter 5, graphene was also used as electrode material. To fabricate graphene electrodes, a thin film of exfoliated graphene (EG)^[5] was firstly prepared on the silicon wafer by my colleague, Sheng Yang, with a vacuum filtration and dry transfer method.^[6] An EG dispersion at 0.05 mg/mL in DMF was prepared and sonicated for 2

h to reduce the aggregation before use. Subsequently, vacuum-filtering was employed through a poly(tetrafluoroethylene) (PTFE) membrane. In order to transfer EG thin film, the filtered film was mechanically pressed against the silicon wafer. Afterwards, the PTFE membrane could be peeled off because of van der Waals interaction between the substrate and graphene. It had to be noted that the thickness of the transferred EG film was highly dependent on the filtration volume. In order to obtain a 50-nm-thick graphene film, the dispersion solution of ~ 5 mL was filtered. The fabrication procedures of graphene electrodes were shown in Figure 9.8. Briefly, I thermally evaporated an Au layer micropattern with 50 nm in thickness on the surface of the EG film by using a shadow mask, which could act as a protection mask against oxygen plasma etching. The oxygen plasma for 30 s removed the unprotected EG resulting in the same pattern with Au layer. After that, the evaporated Au layer was removed by an Au-etchant (Sigma) leaving the patterned graphene electrodes. Finally, the substrate with graphene electrodes was rinsed with Milli-Q water for three times.^[6]

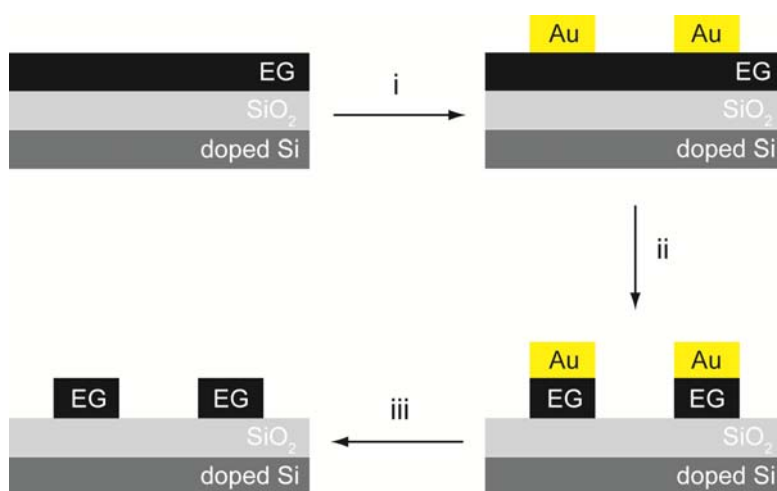


Figure 9.8 Schematic illustration for the fabrication of graphene electrodes. i) Au electrodes with 50 nm in thickness was evaporated on top of EG by using a shadow mask; ii) Oxygen plasma for 30 s was employed to remove EG area without the protection of Au electrodes; iii) Au electrodes were etched.

9.4.3 Surface Modification by SAMs

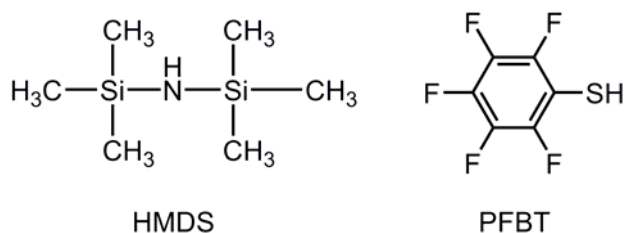


Figure 9.8 Chemical structures of HMDS and PFBT.

After activation by using oxygen plasma, the dielectric layer of cleaned substrate was functionalized with HMDS SAMs from the vapor phase. HMDS in electronic grade was purchased from Alfa (Figure 9.8). 100 μL of HMDS was added into a small glass vial that was located in the center of an airtight container. The container was sealed and placed in an oven at 140 $^{\circ}\text{C}$ for 6 h so that it was filled with HMDS vapor. Subsequently, HMDS molecules were chemically bonded onto the surface of SiO_2 , and a SAM layer was formed.

In order to modify Au electrodes by using SAMs, the pre-patterned substrates ($1 \times 1 \text{ cm}^2$) were immersed into 5 mL of PFBT (Aldrich, Figure 9.8) solution in ethanol at a concentration of 10 mM. After 6 h, PFBT molecules were chemically bonded onto the surface of Au electrodes, and a SAM layer was formed. Then the substrates were rinsed with ethanol and dried in a nitrogen flow.

9.5 Transistor Probe Station

Figure 9.9 showed the photograph of the transistor probe station for OFET measurements in this thesis, in which a microscope was mounted for the observation of source/drain electrodes and organic semiconductor thin films, and three probes were connected to source, drain and gate electrodes, respectively. The whole setup was situated in a glovebox under a nitrogen atmosphere to avoid oxygen and moisture that typically degrade the transistor performance. A semiconductor characterization

system, Keithley SCS 4200, was connected to three probes for all electrical measurements. It contains a software allowing the sweep of I_{DS} as a function of V_{GS} or V_{DS} .

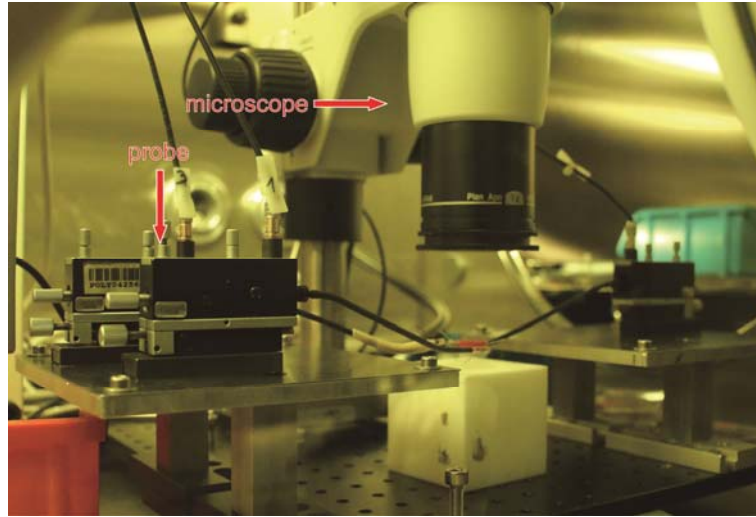


Figure 9.9 Photograph of the transistor probe station.

9.6 OFET Parameter Extraction

The current-voltage characteristics of OFETs can be described by the following equations^[7]:

In the linear regime, $V_{GS} - V_T \gg V_{DS}$,

$$I_{DS} = \frac{W}{L} \mu_{lin} C_i \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad (9.5)$$

In the saturation regime, $V_{DS} > V_{GS} - V_T$,

$$I_{DS} = \frac{W}{2L} \mu_{sat} C_i (V_{GS} - V_T)^2 \quad (9.6)$$

where C_i is the gate dielectric capacitance per unit area, μ is the charge carrier mobility in the semiconductor, L is the channel length of the transistor and W is the channel width. In the linear regime, $V_{GS} \gg V_{DS}$, equation 9.1 can be simplified^[8] to

$$I_{DS} = \frac{W}{L} \mu_{lin} C_i (V_{GS} - V_T) V_{DS} \quad (9.7)$$

In equation 9.3, V_{DS} is constant, and I_{DS} is proportional to V_{GS} , therefore, the mobility in the linear regime (μ_{lin}) can be extracted through the first derivative with respect to the V_{GS} , as follows.

$$\mu_{lin} = \frac{L}{WC_i V_{DS}} \frac{\partial I_{DS}}{\partial V_{GS}} \quad (9.8)$$

In comparison, the mobility in the saturation regime (μ_{sat}) is extracted by equation 9.2 that can be rewritten as:

$$\sqrt{I_{DS}} = \sqrt{\frac{W}{2L} C_i \mu_{sat} (V_{GS} - V_T)} \quad (9.9)$$

Equation 9.5 exhibits that plotting the square root of the saturation I_{DS} against V_{GS} would lead to a straight line. As a result, the value of μ_{sat} can be obtained from the slope of the line, and can be given by

$$\mu_{sat} = \frac{2L}{WC_i} \left(\frac{\partial \sqrt{I_{DS}}}{\partial V_{GS}} \right)^2 \quad (9.10)$$

Therefore, expressions for the charge carrier mobility in the linear and saturation regimes can be derived by equations 9.8 and 9.10. As mentioned in chapter 1.2.2, the density of charge carriers in saturation regime is not uniform, so it is believed that the mobility along the conducting channel is not constant, but the extracted value from equation 9.10 represents a mean value.^[9] Nevertheless, the saturation regime is the range typically used and reported in literature for determination of the charge carrier mobility in organic transistors.

9.7 Materials

In chapter 3, PCPDTBT was provided by Dr. Felix Henkel and synthesized by using a general polymerization procedure according to a modified literature procedure.^[10] The molecular weight (M_n) and polydispersity index (PDI) by

GPC are 40 K g/mol and 5 separately. PTAA was purchased from Sigma-Aldrich Corporation with $M_n = 7000-10000$. PDI₈-CN₂ (ActivInkTM N1200) was purchased from Polyera Corporation.

In chapter 3 and 6, FBT-Th₄(1,4), was synthesized and provided by Dr. Cunbin An with $M_n = 23.2$ K g/mol and $M_w/M_n = 1.9$.^[11] In chapter 5, the same polymer was synthesized and provided by Prof. He Yan with $M_n = 42.3$ K g/mol and $M_w/M_n = 1.71$.^[12]

In chapter 4, α,ω -DH6T was purchased from Sigma-Aldrich Corporation.

In chapter 7, DFCO-4T (ActivInkTM N0400) was purchased from Polyera Corporation. FNDI was synthesized and provided by Dr. Zhongyi Yuan. DTBDT with and without alkyl chains were synthesized and provided by Dr. Cunbin An and Prof. Martin Baumgarten.^[13]

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Publication List

1. **Mengmeng Li**, Tomasz Marszalek, Yiran Zheng, Ingo Lieberwirth, Klaus Müllen, Wojciech Pisula. Modulation of Domain Size in Polycrystalline *n*-Type Dicyanoperylene Mono- and Bilayer Transistors. *ACS Nano*, 2016, DOI: 10.1021/acsnano.5b07742.
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