Electronic Supplementary Material (ESI) for Lab on a Chip.

Continuous high throughput nanofluidic separation through tangential-flow vertical nanoslit arrays

Supporting Information

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Fabrication of vertical nanoslit arrays

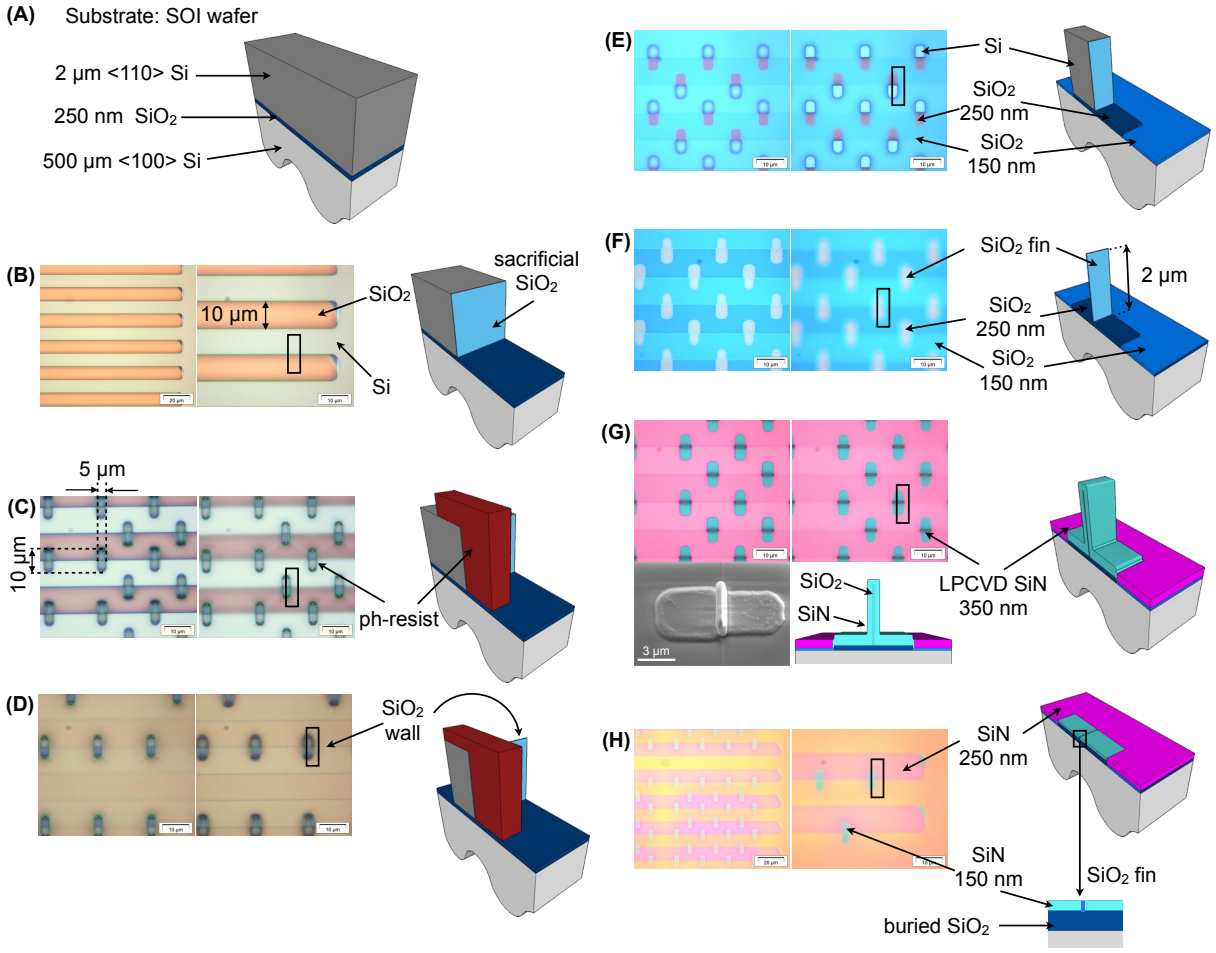

Figure 1: Vertical nanoslits fabrication (A) SOI wafer sketch: 2 μm thick $<110>$ device layer; 250 nm thick buried oxide layer; 500 μm thick handle $<100>$ Si wafer. (B) Si device layer patterned with 10 μm wide trenches etched trough the depth of the device layer. Sacrificial SiO_2 layer grown by thermal oxidation is on the side walls. (C) Patterning of the etched surface by standard photolithography. (D) DRIE etching of Si device layer. (E) Wet etching in buffered hydrofluoric acid (BHF) of not protected sacrificial oxide and partial etching of the buried oxide. Removal of resist by O_2 plasma etching. (F) Etching the residual Si and generation of 2 μm height SiO_2 fins. (G) LPCVD SiN deposition. The fins are encased in the thin layer. (H) Planarization with chemical mechanical polishing CMP of the SiN surface.

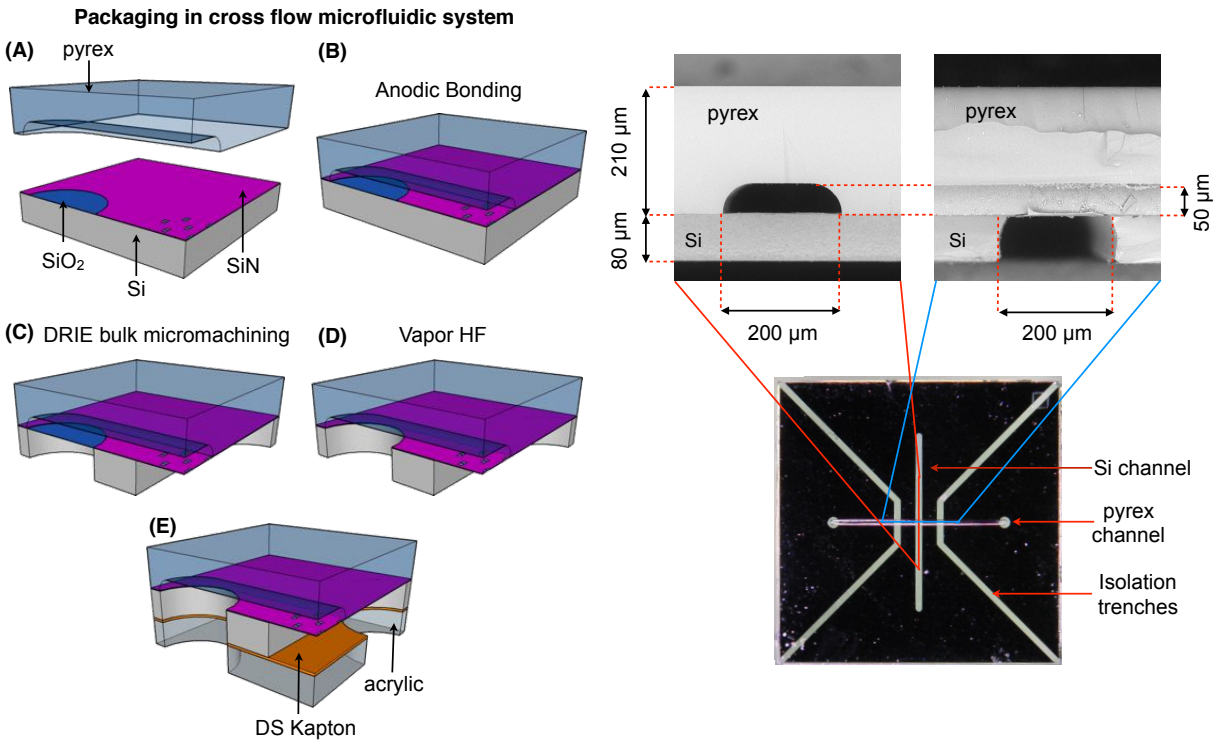

Figure 2: Packaging schematic. Chip top optical view and SEM views of chip cross section along Si and pyrex channel.

The fabrication process start with the patterning of the 2 μm thick $<110>$ device layer of a SOI wafer with 10 μm wide trenches (Figure 1(A)). A LPCVD 50 nm thick SiN layer is used as hard mask for the wet etching in KOH 30 wt% at 40 $^{\circ}C$. Due the high etch rate selectivity between different Si crystal planes of KOH, the etching of Si $<110>$ proceed orthogonally to the surface exposing the (111) plane leading to the formation of vertical smooth side walls.[1] A two step alignment scheme is employed to align the trenches with the crystal orientation more accurately than would be possible by the placement of the wafer flats alone. More specifically, a fan shaped pattern consisting of 3 mm long and 10 μm wide trenches, which fun out at 0.05 degree angles to one another and span from -2 degree to 2 degree, is etched using KOH 30 wt% at 40 $^{\circ}C$ in the device layer to the right and to the left of the wafer. The most narrow lines with minimum undercut representing the real (111) plane, are used as alignment markers for the next patterning step.[2]

Next, the wafer is oxidized in 1000 $^{\circ}C$ dry O_2 and a sacrificial oxide is grown on the vertical walls of the trenches. The oxidation time is changed in accord with the desired sacrificial oxide thickness (Figure 1(B)). The SiN layer, that avoids the top surface of the device to be oxidized, is subsequently removed by wet etching in hot orthophosphoric acid (H_3PO_4) at 160 $^{\circ}C$ for 40 min. Although the selectivity of the etching between SiN and SiO_2 is high, in this step $\sim$5 nm of SiO_2 are etched.[3] The structure needs to be further patterned to determine length, number and position of the nanoslits. Rectangular resist features 5 μm wide and 10 μm long are patterned on top of the trenches edges in order to protect the sacrificial oxide in the following etching steps (Figure 1(C)). The two optical images obtained focusing on the Si surface (left) and on top of the resist (right) help reconstructing the three-dimensionality of the structures shown in the sketch. The Si device layer is etched using silicon anisotropic dry etching (DRIE) leading to the exposure of the buried silicon oxide layer and of the sacrificial oxide, where no protected by the resist pattern (Figure 1(D)). Around 1 μm

of mask underetching occurs in the DRIE etching. Due to exposition of the surface to the previous oxidation and etching steps, the trenches pattern is transferred to the surface of the oxide layer. Next the sacrificial SiO_2 and 100 nm of buried oxide are etched in buffered hydrofluoric acid (BHF) and subsequently the resist is etched using dry O_2 plasma etching (Figure 1(E)). The residual Si is etched using DRIE thus generating vertical SiO_2 fins with a height of 2 μm sitting on top of islands of thicker buried oxide (Figure 1(F)).

The SiO_2 fins are embedded in a 350 nm conformal layer of LPCVD silicon-rich silicon nitride (Figure 1(G)). In both optical and SEM images are clearly visible the resulting structures 2 μm tall, 3 μm long, and 700 nm wide. The geometry of the buried oxide layer is perfectly transferred on the SiN layer, due to the high conformity of the LPCVD process. In the optical images, the areas surrounding the vertical fins are turquoise and not pink because of the larger thickness of the buried oxide in these areas ($\sim$100 nm thicker). The surface is then planarized and the SiN layer thinned using chemical mechanical polishing (CMP) (Figure 1(H)). The SiO_2 fins are thus exposed and nanoslits, which width equals the fins thickness, are obtained by selectively etching the sacrificial oxide using hydrofluoric acid (HF) vapor. The planarization produces a membrane which thickness is smaller than the initial thickness of the SiN layer, and with a smaller thickness around the fins, emphasized in the sketch with different colors of the layer.

In order to package the membrane devices in a microfluidic cross flow system the processed SOI wafer is bonded to a Pyrex wafer in which 6 mm long channels, 50 μm in depth and 200 μm wide, are previously formed using wet etching in HF (49%) as shown in Figure 2. The bonded wafer is then ground down to 80 μm in the Si side, and down to 210 μm in the Pyrex side. The Pyrex side was also polished in order to obtain a light transparent surface. Next, the Si bottom half of the wafer is patterned with 6 mm long channels by bulk micromachining with DRIE etching. This step leads to the release of the membranes located at the crossing between channels in the Pyrex top half and the channels in the Si bottom half. Bottom buried oxide layer, used as stop layer for the DRIE, and sacrificial oxide fins are etched by exposing the Si bottom half of the diced chips to HF vapor, opening in this way the nanoslits Figure 2(D). The Si bottom half of the chips is finally sealed using a 2 mm thick acrylic layer. Double sided kapton tape is used to keep together acrylic and silicon chip (Figure 2(E)). The acrylic is used as injector chip, the micro channels and holes are made in the acrylic by laser cutting and engraving. Si chip, and acrylic are easily aligned. The good adhesion to the double sided kapton tape avoid the formation of fluid leakages between channels and isolation trenches, allowing the continuous use of the chips for weeks.

SEM images analysis

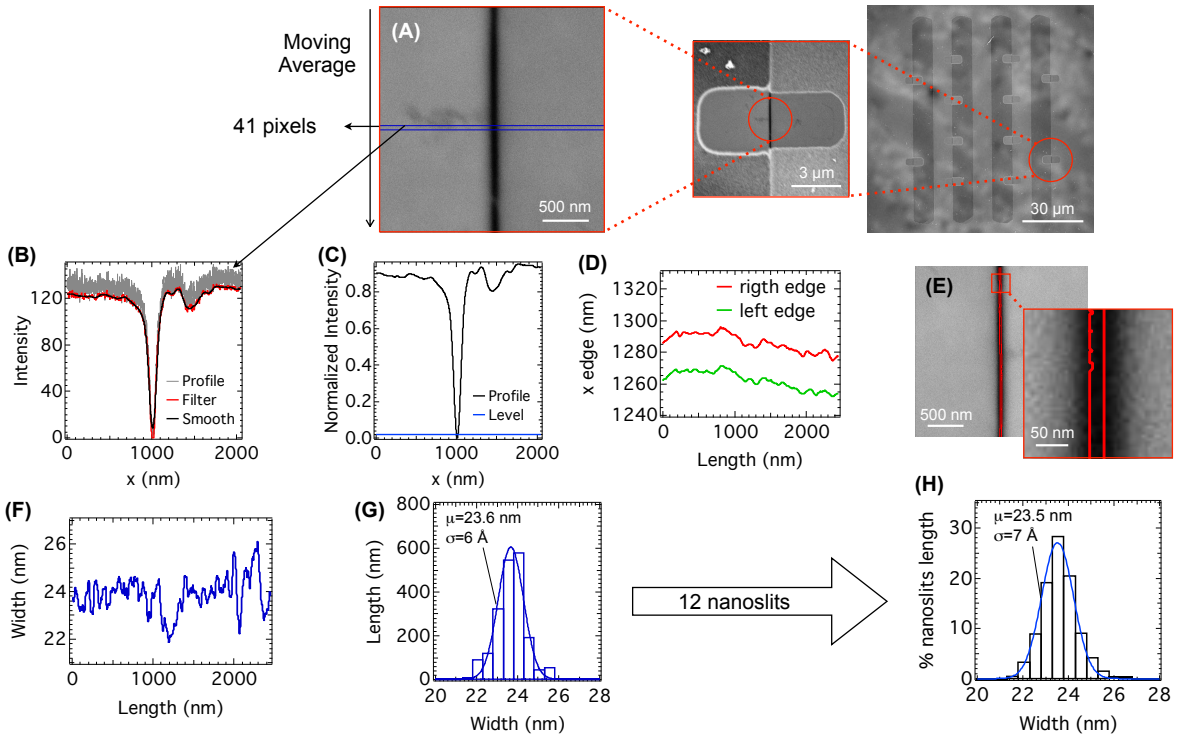

Figure 3: Nanoslit edges detection using Igor Pro 6. (A) SEM image of nanoslit: the line profile of the image is constructed by averaging 41 pixels orthogonally to the nanoslits direction. (B) The images are treated with a gaussian filter to reduce the noise (gray to red profile). The the line profile is smoothed using a Savitzky-Golay algorithm (red to black). (C) The position of the edges is given by the position at which the line profile crosses with the level. (D) The nanoslit edges (left and right) plotted in this graph are detected by using the moving average over 41 pixels. (E) The nanoslit width is here plotted as function of the position. (F) Histogram of the width distribution over the length of a single slit. (H) Histogram of the width distribution over the length of 12 nanoslits over the membrane. The Gaussian distribution, plotted in blue, was calculated starting from the values of mean width μ, and standard deviation σ calculated from the entire data set of widths collected by analyzing the 12 single slit images.

Conductance Mesurements

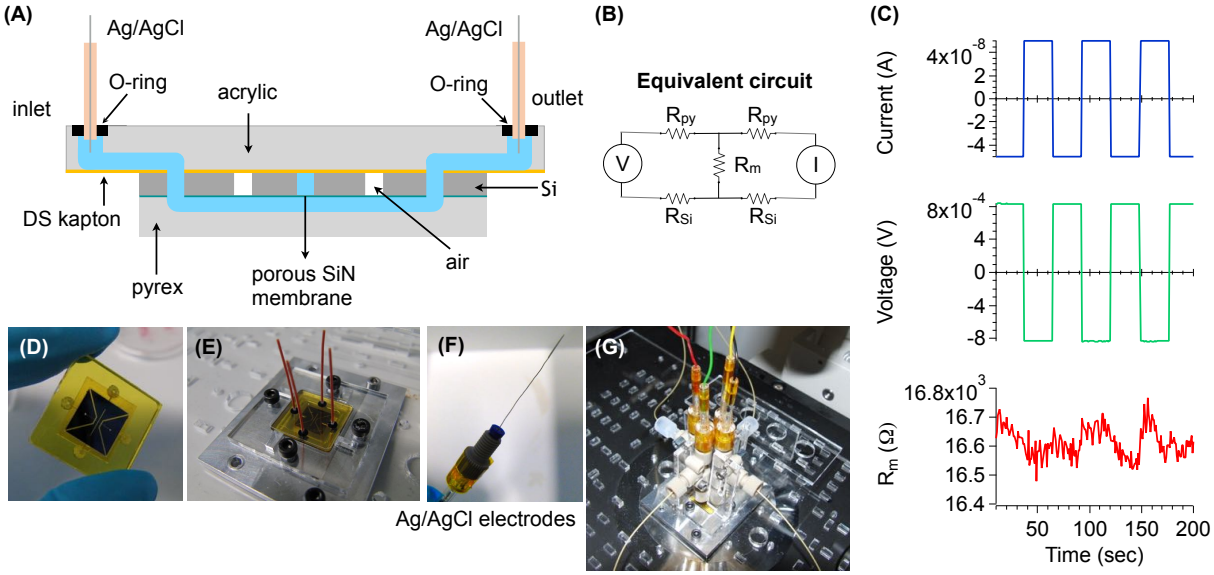

Figure 4: (A) Schematic of the cross section along the pyrex channel of the microfluidic devices used to measure the conductance. (B) Equivalent electrical circuit of the fluidic devices. (C) A current is applied across the membrane trough the electrodes at the inlets of the crossing channels. The voltage drop corresponding to the membrane resistance was measured through the electrodes connected at the outlets. The high impedance of the Keathley 2636 SourceMeter makes possible to measure the high resistance of the membrane at low KCl concentrations. To avoid effects due to the drift in potential at the Ag/AgCl electrodes, positive and a negative currents were applied with a period of 10 s and the drift was subtracted from the signal.

Separation of charged dyes

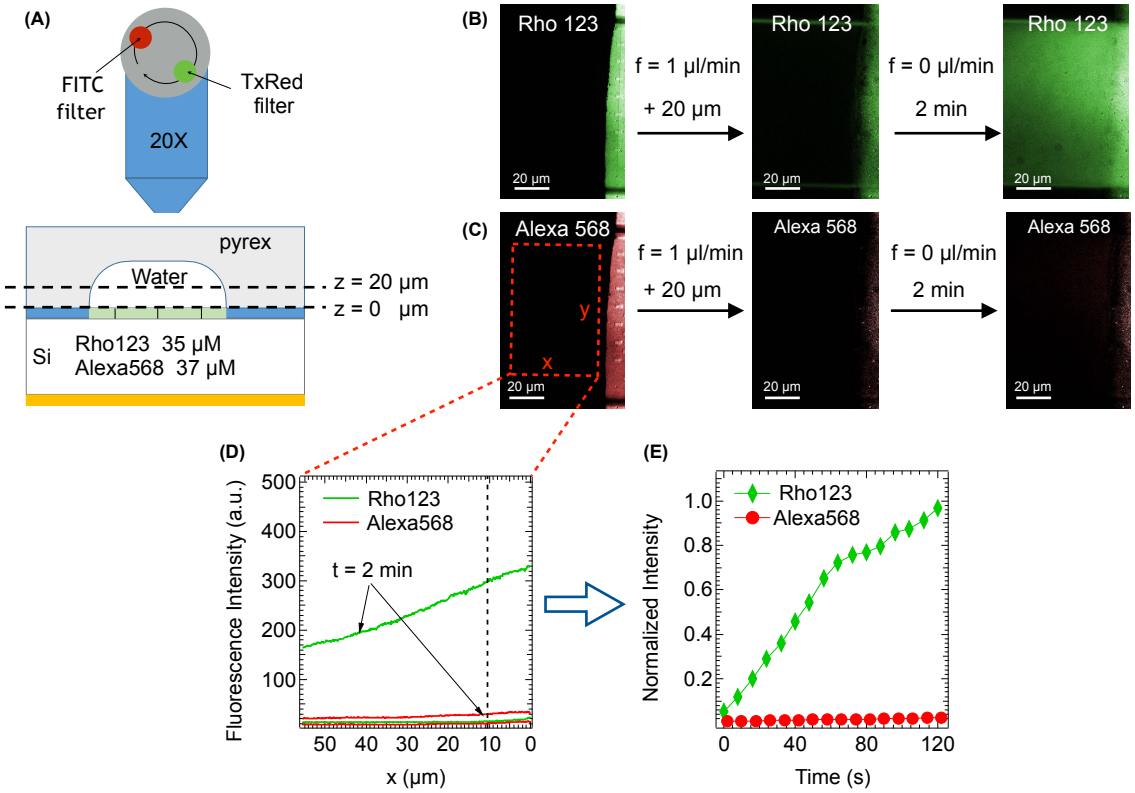

Figure 5: Static separation of charged dyes. (A) Passage of fluorescent dyes through the SiN membrane was monitored with a fluorescence confocal microscope. The dye mixture flows in the silicon channel, while pure water flows on the pyrex channel. During the filtration experiments the flow is stopped and the dyes permeating the membrane diffuse away from the membrane. (B) Fluorescent images of passage of rhodamine 123 through a negatively charged SiN membrane at low ionic strength. Using structured illumination (Andor DSD) we were able to image optical sections. (Left) Image of optical section at the membrane plane z = 0. The flow rate was set to 1 μl/min. (Center) Initial frame: optical section well within the channel (z = 20 μm) to avoid any possible bias by molecules sticking to the channel walls. The flow was stopped immediately after. (Right) Image acquired after 2 min. (C) Fluorescent images of passage of Alexa 568 at low ionic strength. The initial frame (Centre) and the final frame (Left) are almost identical. The negatively charged dye is rejected by the negative membrane very efficiently. (D) Fluorescence intensity as a function of the distance from the membrane on initial and final frames. The fluorescence intensity of Alexa568 is almost unchanged after 2 min, and is very low to respect the Rho123. (E) Kinetics of the passage of Alexa 568 and rhodamine 123 in a low ionic strength solution. The intensity was measured 10 μm away from the membrane edge (see dashed line in (D)). The signal was normalized by the intensity recorded while flowing in the pyrex channel a 10 times diluted dye mix solution. This normalized signal gives unambiguous information about the relative fluxes of the two dyes through the membrane.

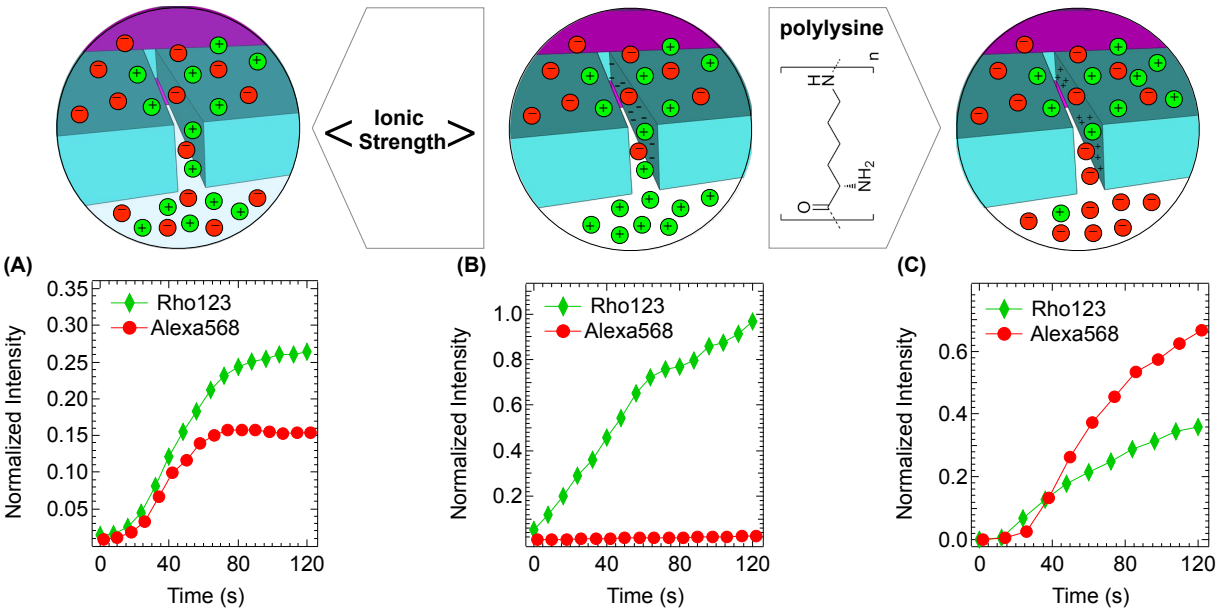

Figure 6: Comparison of permeation kinetics of rhodamine 123 and Alexa 568 in three different experimental conditions. (A) Permeation kinetics through negatively charged nanoslits at high ionic strength (0.5 M KCl). (B) Permeation kinetics through negatively charged nanoslits at low ionic strength. (C) Permeation kinetics through polylisine surface modified nanoslits at low ionic strength.

References

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[2] Pan Mao, Ultra-High-Aspect-Ratio Nanofluidic Channels for High-Throughput Biological Applications. Ph.D. thesis, Massachusetts Institute of Technology, 2009.

[3] Williams, K. R.; Gupta, K.; Wasilik, M. *Journal of Microelectromechanical Systems* **2003**, *12*, 761–778.