Optimizing BUSSARD, the new 16-phase inverter system of ASDEX Upgrade

Markus Teschke[a], Nils Arden, Horst Eixenberger, Michael Rott, Michael Schandrul, Wolfgang Suttrop and the ASDEX Upgrade Team

Max Planck Institute for Plasma Physics, Boltzmannstr. 2, D-85748 Garching, Germany

BUSSARD is a new inverter system at the nuclear fusion experiment ASDEX Upgrade for mitigation of so called "edge localized modes" (ELM) [1,2] and execution of other, physics related experiments. The concept and first results have been presented in detail [3]. Four-phase operation was routinely done during shot campaign 2015/16 and much experience in operation was gained. Now, the completion of BUSSARD is finished and many improvements have been adopted. 16-phase operation with up to 16x 1.3 kA coil current of arbitrary waveform controlled by 16 independent real-time controllers at 500 Hz bandwidth, 5 kHz switching frequency and about 1 MW/10 Mvar total real/reactive power was commissioned within the last campaign. In this publication it is discussed the power stage, PSpice simulations and the fully revised predictive controller with special focus on a (first time published?) numerical method to reduce systematic errors in current measurement. This ends up in an effect comparable to loop latency reduction.

Keywords: multilevel inverter / converter (MLC); pulse width modulation (PWM); predictive controller; averaging correction; loop latency; neutral point clamped topology (NPC); magnetic perturbation in-vessel coils (MPC / IVC)

1 Introduction

Small non-axisymmetric perturbations of the magnetic confinement field are found to be beneficial in the ASDEX Upgrade (AUG) nuclear fusion experiment in Garching/Germany, and to this end AUG is being equipped with two different sets of magnetic perturbation saddle coils – planned or already integrated into the vacuum vessel, the so called "A-coils" and "B-coils". Currently, 16 B-coils are integrated [4,5]. To operate these coils at full bandwidth (DC...3 kHz / 500 Hz A/B-coils) and full current (1.3 kA peak), "BUSSARD" – a 16-phases IGBT-based inverter was developed, installed and successfully commissioned at the end of the 2016 campaign (first AUG shot #33696).

2 Some Remarks on Power Stage

The concept of BUSSARD was chosen in a way that operation of the low-bandwidth B-coils is possible (up to 500 Hz) as well as the high-bandwidth operation of the future planned A-coils (up to 3 kHz). It was also found out that a good reactive power exchange between the inverters is advantageous for most physical applications, like e.g. rotating fields for ELM mitigation. Both requirements led to the somewhat unusual power stage topology in Fig. 1.

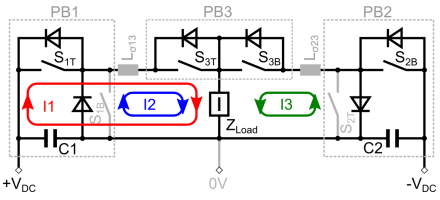

Fig. 1: "NPC-like" power stage (half bridge). Elements which differ from the original NPC topology are grey coloured.

It is comparable to the well-known neutral point clamped topology (NPC) but equipped with additional switches S_{1B} and S_{2T} and fed by two individual DC voltages V_{DC+} and V_{DC-}. This offers the opportunity to operate at DC and very low frequency, which is impossible or very hard to realize with standard NPC topology (because C1 and C2 voltages have to be balanced, actively). To keep development costs low, commercially available power blocks (PB) were used, equipped with high-current IGBT half-bridges (top switch S_T, bottom switch S_B) and the corresponding driver circuits. In case of NPC-like full-bridge operation (replace 0V-junction of Z_{Load} by another NPC-like half-bridge output) the additional switches S_{1B} and S_{2T} enable additional redundant switching states which can be used for frequency doubling. There exist 2^4=16 switching states (instead of 3^2=9 for standard NPC) for five output voltage levels ($-2\cdot V_{DC}$, $-V_{DC}$, 0V, $+V_{DC}$, $+2\cdot V_{DC}$) and the total switching frequency can be quadrupled compared to the single PB switching frequency. It has to be noted that only switching losses can be balanced. The NPC-like topology does not offer any advantage if conducting losses are close to the limit. A challenge in realization are the inter-PB stray inductances $L_{\sigma 13}$ and $L_{\sigma 23}$. For example, commutation between I1 ($V_{Load}=+V_{DC}$) and I2 (V_{Load}=0V) switching state is unproblematic because current of $L_{\sigma 13}$ does not change during switching event. In contrast to this, switching between I1 ($V_{Load}=+V_{DC}$) and I3 (V_{Load}=0V) causes high voltage spikes due to a rapid current change in $L_{\sigma 13}$ and $L_{\sigma 23}$ during switching event. Snubber circuits have to be added which are related to additional losses, of course [3].

3 Some Remarks on PSpice Simulations

We performed detailed simulations about each component of BUSSARD since beginning of this project. The calculation time is acceptable as long as the single inverters can be assumed to be decoupled from each other. This is fulfilled if energy stored in DC capacities is much bigger than energy stored in the load circuits (= B-coils and output filters), see Fig. 2:

[a]*email: teschke@ipp.mpg.de, phone: +49 (0) 89 3299 1296*

$$E_{DC} >> E_{Load} \quad \text{or} \quad \tfrac{1}{2}\cdot V_{DC}^2 \cdot C >> \tfrac{1}{2}\cdot I_{Coil}^2 \cdot L_{Load}$$

For BUSSARD, the maximum DC voltage is 340 V, the maximum B-coil current 1.3 kA, the total load inductance roughly 16x 50µH, the total DC link capacity 16x 3.5mF. This results in

$$E_{DC}=3.2\ \text{kJ} >> E_{Load}=0.7\text{kJ}$$

The situation seems to be relaxed in that only small DC voltage excursions are to be expected for full load current swing. For reduced voltage operation, which is interesting for powering the coils at low-ripple DC or very low-frequency, the situation becomes much more complicated. At half DC voltage, the energy distribution is changed to

$$E_{DC0.5}=0.8\ \text{kJ} \approx E_{Load}=0.7\text{kJ}$$

due to quadratic relation of E_{DC} on the voltage.

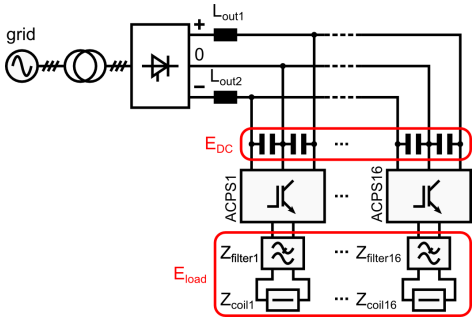

Fig. 2: Stored energy distribution of BUSSARD

For reduced DC-link voltage, inverters can not be assumed to be electrically decoupled from each other anymore. The dynamic is limited by the acceptable derivative of current given by the output coils of the common thyristor rectifier $L_{out1,2}$. This has to be taken into account by the inverter controllers, otherwise rapid breakdown of DC link voltage is possible during quick steps in load current and/or oscillations on the DC link can be generated. This behaviour can be quite complex and adequate simulation is difficult to realize, because the whole system has to be modeled. To take these difficult boundary conditions into account, an extreme approach was chosen: Keep it as simple as possible, at the expense of accurate description of unnecessary detail, as long as the essential system effects under study are retained.

A small detail of the complex global BUSSARD model is presented in Fig. 3. The thyristor model has almost nothing to do with a real thyristor but its commutation behaviour is comparable. It is voltage controlled via gate junction "G" (instead of being current controlled in reality) and its resistivity depends exponentially on the current between anode "A" and cathode "K" (instead of gate current amplification in reality). The "ignition" of the thyristor is only possible for gate voltage "G" >1 Volt. The resistivity is modified by the voltage controlled voltage source E1 which depends on the actual current measured by the current controlled voltage source H1. Between +0.3A and -0.6A, the A-K-resistivity is exponentially modified between 10^{-3} and 10^{6} Ω. The delay element LAPLACE1 is needed to fulfill causality of the loop spanned by H1, E1 and the ideal elements in between. It can also be used to take into account the commutation time of real thyristors. The numerical behaviour of this model is continuous in time and between input (current) and output (resistivity). Convergence is very good (even better then SPICE implementations of switches and diodes) and thus calculation time acceptable even in case of a big number of involved thyristors like here for the 2x6-pulses thyristor bridges.

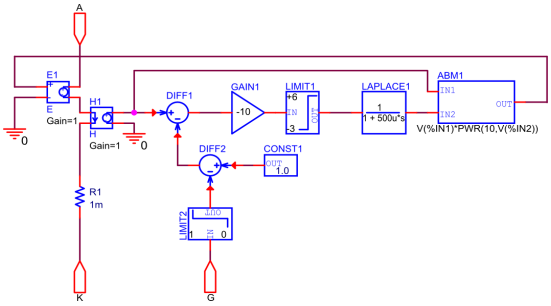

Fig. 3: PSpice model of a thyristor

4 Predictive Controller

As an outcome of the simulations, the existing controller was fully revised to achieve the following main goals:

- The controller should be stable even in case of unrealistic waveform request. Therefore, also the special behaviour of DC feeding (see chapter above) should be taken into account [6].
- Current overshoot has to be small in any case due to strict over-current turn-off limits (IxB forces). Typical operation is done close to that limit! Nevertheless, full-bandwidth operation has to be possible.
- The system should be open for implementing additional models like e.g. magnetic calculations of the coil field and forces or a model of the mechanical support structure.

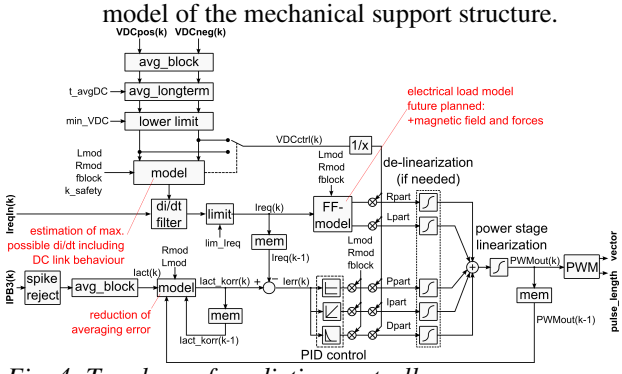

Fig. 4: Topology of predictive controller

The block diagram of the new controller topology is shown in Fig. 4. A feed-forward (FF) model operates the load with the requested waveform as the only variable input. The model considers load inductance L_{mod}, resistance R_{mod} and switching frequency f_{sw}. The output is a voltage which becomes scaled by the actual DC-link voltage. Non-linearities of load can be taken into account by separate de-linearization of inductive and resistive voltage output. For quick response, the de-linearization is performed by use of pre-calculated tables which are setup during preparation phase before each plasma pulse.

The model generates a realistic output only for realistic input, of course. For an inductive load, the requested current derivative has to be small enough for the actual DC link voltage, otherwise the model output results in a duty cycle for PWM generator higher than 100% and/or possibly a risk of full breakdown of the DC-link voltage. To warrant a realistic input, another model estimates the achievable change of current by given DC link voltage and known load parameters. It also chooses the relevant DC link (there are two!) which has to power the load current during next switching cycle. A real-time di/dt filter modifies the requested waveform in case of too high current derivative.

Because even a good load-model can never be a perfect one, a PID controller is implemented in addition. In contrast to an analogue PID controller, its input Ierr(k) is not the actual control error (= actual request minus actual measurement). It is the remaining error after a single switching period, instead (= request one switching period ago minus actual measurement). For a good model, this value is typically much smaller which means that for any given control error the PID gains can be reduced to achieve higher stability.

For a stable controller, a good load current measurement with low noise amplitude is needed. Therefore, all samples of a switching period (up to 30 at f_{sw}=5 kHz switching frequency) are averaged. In addition, a "spike rejection" filter removes the two samples with highest and lowest value. This is done to suppress electromagnetic interference on current measurement during switching events of power stage.

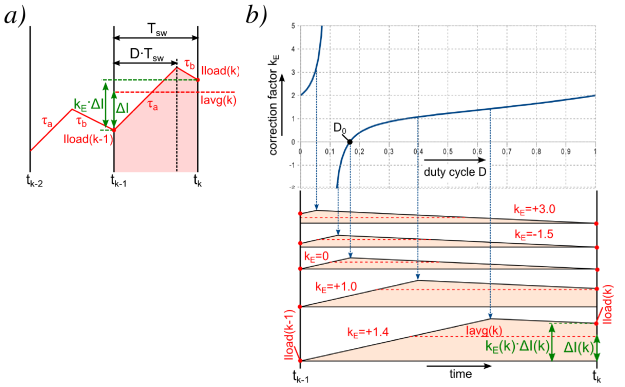

Fig. 5: (a) Load current characteristics, (b) Correction factor k_E for a slew rate relation of k_c = 0.2

For highest controlling performance and stability, small delay of control loop is essential [7]. This delay here sums up by the individual delays of *(i)* limited bandwidth of current probe (< 0.5µs), *(ii)* the analogue anti-aliasing filter at ADC input (< 10µs), *(iii)* the above mentioned digital (boxcar) averaging (T_{sw}/2=100µs @ f_{sw}=5kHz), *(iv)* the average controller's operation system response time (< 20µs) and *(v)* the control algorithm itself (< 5µs). So, the digital averaging is identified as highest contribution. To improve this situation, another model to estimate the (systematic) averaging error of current measurement was implemented.

In Fig. 5a the strategy for this model is demonstrated. It is shown the variation of load current in time for two switching periods T_{sw}. For each switching period there exists a time interval for current ramp up with slew rate τ_a and an interval for current decay with slew rate τ_b. After a switching period of length T_{sw}, the averaged load current $I_{avg}(k)$ is known instead of the real load current $I_{load}(k)$. If we define

$$\Delta I(k) = I_{avg}(k) - I_{load}(k\text{-}1)$$

we can try to estimate a correction factor k_E with

$$I_{load}(k) = I_{load}(k\text{-}1) + k_E \cdot \Delta I(k)$$

by use of additional, real-time available information. This is equivalent to a reduction of averaging delay, because averaging process is comparable to low pass filtering (which is related to a phase shift). The additional real-time available information is the duty cycle D of pulse width modulated (PWM) load current and the slew rates for current rise τ_a and current fall τ_b. The slew rates depend on actual current and voltage levels and the calculation should be refreshed each switching cycle. Even though the individual slew rates include the well known L_{load}/R_{load} relation, the ratio k_c of both does not. It can be shown that

$$k_c = \frac{\tau_b}{\tau_a} = \frac{I_{act}}{I_0 - I_{act}}$$

whereby I_{act} is the actual current level (which can be the last current estimation or the last reference current value) and I_0 is the ohmic current limit with $I_0 = U_{DC}/R_{mod}$. By the help of k_c it can be shown that

$$k_E = \frac{D - k_c \cdot (1-D)}{D \cdot (1 - D/2) - k_c/2 \cdot (1-D)}$$

For a slew rate relation of $k_c = 0.2$ the duty cycle dependence of k_E is shown in Fig. 5b. There is a pole at $D < D_0 = k_c/(1+k_c)$, which means k_E can have a very high value (which is related to an increase of noise for $|k_E|>1$). Thus, the correction should not be applied in this case. For the most interesting, highly dynamic case, which means large duty cycle $D > D_0$ the function is smooth and the range limited by a maximal value of $k_{Emax} = 2$. Only in this case, a small loop delay is really relevant for controlling quality (e.g. to minimize overshooting of current after a step in requested waveform) and the correction results in a significant improvement. The range of $k_E \approx 0$ has to be handled carefully, because $k_E = 0$ corresponds to a deactivation of load current measurement – the controller becomes blind for unexpected events. The correction should not be done too long in succession, because this would lead to a growing summation error. There exists an elegant solution for this problem: The controller can count the number of cycles in succession and if this number is too high, an alternative correction can be done. In this case, we try to find a correction factor k_F with

$$I_{load}(k) = I_{avg}(k\text{-}1) + k_F \cdot \Delta I_{avg}(k)$$

and we define

$$\Delta I_{avg}(k) = I_{avg}(k) - I_{avg}(k\text{-}1)$$

With the assumption that the ratio of slew rates k_c did not change significantly (= similar current level) and the

stronger assumption that the duty cycle D did not change since last switching period as well, it can be shown

$$k_F = 2 - \frac{1}{k_E}$$

Obviously, k_F has a root at $k_{E0} = 0.5$ and it has a high growth rate for smaller $k_E < k_{E0}$ – so, the correction should not be done in this region. For $k_F = 0$ the most recent measurement is fully ignored. The original average should be taken instead or k_F should be limited to a minimal value.

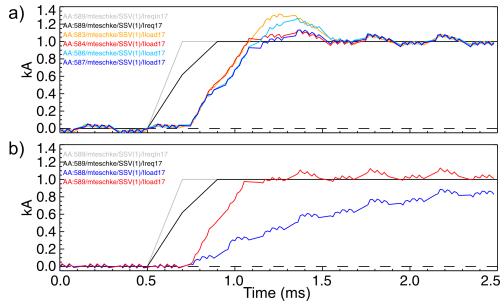

Fig. 6: Comparison of step response from different controllers (load emulator board, V_{DC}=100V, f_{sw}=5kHz): black/grey: original/corrected reference curve, red/orange: predictive controller with/without k_E correction, blue/light blue: PI-controller with/without k_E correction. (a) k_p=0.8, k_I=0.8, (b) k_P=0.2, k_I=0.2

It is interesting, that one get almost the same controlling results by use of this alternative correction method, permanently. In this case there exists no summation error, anymore (see Fig. 7 and text below). It is also important to mention that noise can be increased by a factor of two in worst case for the technically relevant range of k_E,k_F = 0...2 which is much better than a simple weighting process (e.g. taking the last current sample alternatively would increase noise by a factor of 30 in case of 30 samples per switching period T_{sw}). There were also tested other well known methods for model-based real-time prediction of load current trend. They are typically related to offset errors in case of model inaccuracies which have to be compensated by the PID controller. This can worsen controlling results drastically. This problem does not exist for the methods shown here.

Finally, some results are shown in Fig. 6,7. They were achieved with the original BUSSARD hardware but instead of the power blocks, an analogue emulation board was adapted. Systematic analysis is much easier in this way. Full B-coil operation was also performed and the results are comparable. In Fig. 6a the step response of different controllers is compared. For optimal gain factors of proportional part k_P and integral part k_I, there is almost no difference between the model-based predictive controller and a pure PI-controller. But for both controllers, there is a huge difference in case of corrected averaging value as controller input or the non-corrected one. The overshooting is much higher for the non-corrected case. To increase controller stability it can be advantageous to reduce the controller gain factors, as shown in Fig. 6b. In this case, the model-based predictive controller is in clear advantage to a pure PI-controller, of course.

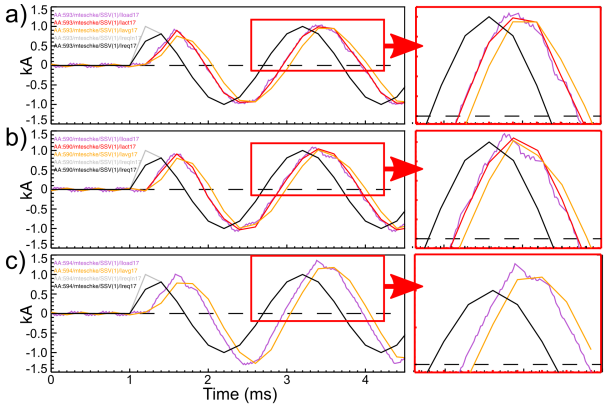

Fig. 7: Comparison of different correction methods (predictive controller, k_P=1.0, k_I=1.0, V_{DC}=100V, f_{ref}=500Hz, f_{sw}=5kHz, emulated load). (a) k_E-, (b) k_F-, (c) no correction activated. grey/black: original/corrected reference violet: measured current red/orange: corrected/original boxcar average.

In Fig. 7 the correction with (a) k_E (and k_F each 10th cycle to limit summation error) and (b) k_F exclusively is compared. As a reference, the same controlling was done without any correction in (c). The original average is always shown to compare (orange). The reduction of overshooting effect is significant – the corrected average (red) is almost superimposable to the original current measurement (violet). k_E-correction is slightly better during periods of high derivative in current, which is related to high variation of duty cycle D. This example demonstrates operation very close to the theoretical maximum of dynamic with given voltage and load (L_{load}=20µH, R_{load}=11 mΩ, peak controller output up to approx. 100%).

5 Acknowledgments

BUSSARD is an in-house development, designed and assembled by (alphabetic order): N. Arden, H. Eixenberger, M. Gorniok, M. Heckmeier, P. Höpfl, C. Jacob, C.P. Käsemann, K. Klädtke, E. Neubauer, S. Prey, M. Rott, M. Schandrul, S. Schneider, T. Schwarz, W. Suttrop, M. Teschke, R. Zultner. A special thank to the whole AUG team for continuous support in every sense.

This work has been carried out within the framework of the EUROfusion Consortium and has received funding from the Euratom research and training programme 2014-2018 under grant agreement No 633053. The views and opinions expressed herein do not necessarily reflect those of the European Commission.

6 References

[1] W. Suttrop et al., Phys. Rev. Lett. **106** (2011) 225004

[2] W. Suttrop et al., Plasma Phys. Contr. Fus. **53** (2011), 124014

[3] M.Teschke, et al., Fusion Eng. Des. (2015) 171–176

[4] T. Vierle at al., Fus. Eng. Des. **84** (2009) 1928

[5] M. Rott et al., Fus. Eng. Des. **84** (2009), pp. 1653-1657

[6] N. Arden et. al., Fus. Eng. Des. (2017), same conference

[7] W. Suttrop et al., Fus. Eng. Des. **84** (2009) 209