

MARCONI FUSION: The new High Performance Computing facility for European nuclear fusion modelling

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Abstract— The new European HPC facility for Fusion is in operation since July 2016. It replaces, for European fusion researchers, the Helios supercomputer installed in Japan in the context of the Broader Approach agreement. The supercomputer is hosted at CINECA and it is a fraction of the MARCONI system. Thanks to a customized technical project done by ENEA, in a joint development agreement with CINECA, the European community of fusion modelling can exploit the latest available CPU technologies, following the CINECA HPC roadmap towards 50 PFlops planned for 2019. The MARCONI Fusion fraction is being delivered in two phases: the first one, 1 PFlops of CPU multi-core architecture based on the Intel Broadwell processors, is already in operation since July 2016, and the second one, 5 PFlops of the same architecture based on the INTEL Skylake processors, will be deployed in July 2017. Furthermore the project includes 1 PFlops of the third generation of Intel Xeon Phi many-core architecture (Knights Landing generation).

Within this framework, ENEA/CINECA provides, in addition, the operation support of the Gateway infrastructure of EUROfusion Work-Package Code Development. A new Gateway HPC system is in operation at CINECA since Jan. 2017 thanks to the data migration and software porting activities carried out by ENEA/CINECA team together with the Core Programming Team of the Infrastructure and Support Activity work package from EUROfusion. The new Gateway infrastructure is tightly coupled with the MARCONI Fusion fraction, sharing the same 100 Gbps low-latency network based on the Intel OmniPath technology.

The paper describes the technical details and the performances of MARCONI, one of the largest HPC OmniPath based infrastructure.

Index Terms — HPC: High Performance Computing

I. INTRODUCTION

The European Fusion Research roadmap [1] provides a long-term perspective to enable electricity production by mean of nuclear fusion well before 2050. ITER is the key facility in the roadmap and it is already on-going placing the EU in a leading position.

Theory and the modelling effort in plasma and materials relevant for nuclear fusion is a crucial key in the roadmap as capability to validate experimental physics results produced by ITER and to enable the design of the next fusion power plant DEMO.

Considerable progress has been made with detailed modelling and the simulation of plasma evolution in tokamak configurations, control, stability and its impact on materials is now at high level of exploitation in the fusion specialists community, developing integrated models able to simulate the whole scenario of a tokamak experiment.

Special provisions for High Performance Computing (HPC) are being recommended in the fusion roadmap as essential

facilities to support basic research and the modelling effort for the various objectives.

The European Fusion community has used dedicated HPC facilities since 2009, with HPC-FF [2]: a multiprocessor Intel[®] Xeon Nehalem EP[™] cluster of 100 TFlops of peak power and Infiniband QDR low latency network, in operation until 2013 at Jülich Supercomputing Centre, followed by Helios: a supercomputer with a performance of 2 PFlops consisting in a Intel Xeon Sandy-bridge EP[™] partition of 1.6 PFlops and in a many-in-core Intel Xeon Phi (KNC generation) partition of 0.4 PFlops with the same low latency network, in operation until the end of 2016 at IFERC-CSC in Rokkasho, Japan [3]. Both HPC facilities have been exploited by means specific allocation time project calls relevant in plasma and materials modelling and nuclear fusion technology simulations.

Furthermore the High Level Support Team (HLST), the developers team based in IPP Garching, has provided to optimize codes in order to improve the speedup on the new CPU technologies and low latency network as well, including also the new Many Integrated Core (MIC) architectures Intel Xeon Phi[™].

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Following the increasing need in the issues related to plasma physic simulations (turbulence, MHD, edge physics and integrated modelling) together with an important number of computing projects addressing technology issues, a growing number of fusion modelling developers are optimizing with success their own codes making able for scaling up to a large number of cores. Therefore the EU fusion community are extending its technical computational capabilities by establishing a new HPC facility for Fusion Applications under EUROfusion. The facility, named MARCONI-FUSION is a dedicated part of a larger HPC Tier-0 system hosted at CINECA [4] (Bologna) under an EUROfusion Project Implementing Agreement (PIA) with ENEA/CINECA. It consists in two parts: a conventional processor part (based on Intel Xeon processors) and a many-cores processor part (based on Intel Xeon Phi processors).

Thanks to CINECA Tier-0 Development Roadmap of the HPC infrastructure for the period 2016–2020, the EU fusion community could deploy HPC resources based on the newest technology generation of processors.

Furthermore as consequence of the Gateway shutdown at IPP Garching, additional resources are allocated to the new Gateway closely connected to Marconi-Fusion hosting the IM (Integrated Modelling) tool developed by EUROfusion. For this purpose, a cluster of 24 compute nodes, has been configured in a flexible environment allowing graphical interactive remote sessions and batch jobs submissions as well. Thanks to a common hardware/software infrastructure, the Gateway users can exploit the HPC computing resources of Marconi.

The paper describe hardware/software configuration of the CINECA Marconi HPC facility, the Fusion partition and the new Gateway as well. It includes performance benchmarks, issues in the new high performance interconnectivity network for configurations with a large number of compute nodes and performance indexes during the first phase of operations.

II. MARCONI

The CINECA is currently one of the Large Scale Facilities in Europe and it is a PRACE [5] Tier-0 hosting site. Aimed at supporting scientific research in HPC, CINECA approved a development roadmap in two provisioning phases, from 2016 to 2020. The first provisioning phase in 2016-2017 is being provided a computing peak of 18 PFlops as Tier-0, named MARCONI. The complete MARCONI deployment is being expected on Jul.2017 and it is based on the following three steps:

- *A1*: 2 PFlops Intel Xeon conventional “Broadwell (BDW)” based, in full production on Jul. 2016
- *A2*: 11 PFlops Intel Xeon Phi “Knights Landing (KNL)” based, in full production on Jan.2017
- *A3*: 5+ PFlops Intel Xeon “Skylake (SKL)” based, it is being expected on Jul. 2017.

In total MARCONI is 18 PFlops peak performance, 17 PB raw of high performance storage and 3 MW of power consumption.

MARCONI A1

MARCONI *A1* is the first part of the new Tier-0 system, co-designed by CINECA and based on the LENOVO NeXtScale platform. It takes advantage of the new Intel[®] Omni-Path Architecture (OPA), which provides the high performance interconnectivity (100 Gb/s) required to efficiently scale the system’s thousands of servers. A high-performance Lenovo GSS storage subsystem, that integrates the IBM Spectrum Scale[™] (GPFS) file system, is connected to the Intel Omni-Path Fabric and provides data storage capacity. This system is air-cooled.

A dedicated fraction of MARCONI *A1*, (named MARCONI-FUSION) is reserved for the EUROfusion HPC activities, next replaced by 5 PFlops of MARCONI *A3* shall be in production until Dec.2018, end of EUROfusion HPC Phase 1 commitment. The Table 1 shows the main characteristics of the MARCONI *A1* and the dedicated fraction of MARCONI-FUSION as well.

	MARCONI A1	MARCONI-FUSION
Model:	Lenovo NextScale	
Architecture:	Intel OmniPath Cluster	
Nodes:	1512	806
Processors:	2x18 cores Intel Xeon E5-2697 (BDW) at 2.3 GHz	
Cores:	36 cores/node – Total=54432	Total=29016
RAM:	128 GB/node , 3.5 GB/core	
Racks:	21 + 1 (mgmt.shared)	~11+1 (mgmt. shared)
Peak Performance:	= 2 cpu × 18 cores × 2.3Hz × 16 fpo × 1512nodes=2.003 PFlops	= 2 cpu × 18 cores × 2.3Hz × 16 fpo × 806nodes=1.068 PFlops
Disk Space:	17 PB (raw)	5 PB (raw)
Power:	700 kW	350 kW

Tab.1: MARCONI A1/FUSION main characteristics

The compute node of MARCONI *A1* is based on server LENOVO NeXtScale nx360M5. It’s a ½U two-socket server supporting Intel Xeon V4 up to 22 cores per processor, DDR4 memory at up 2400 MHz and DIMM capacities up to 64 GB. The NeXtScale architecture provides a dense compute nodes assembly thanks to the n1200 chassis that can host up to 12 nx360M5 nodes in a 6U enclosure.

The MARCONI *A1* compute node configuration is the following:

- 2 x CPU Intel Xeon E5-2697 v4 / 18 core at 2.3 GHz
- 8 x 16GB DIMM of RAM DDR4 2400MHz .
- 1x120 GB SATA MLC S3500 Enterprise Value SSD
- 1 x link OPA (Omni-Path) 100Gb/s, 2 link 1GbE

The 1512 compute nodes nx360M5 are packaged in 126 nx1200 chassis assembled in 21 racks 42U.

The Front-End system of MARCONI *A1*, in sharing with the FUSION fraction, is composed of 8 login nodes LENOVO x3550M5 1U (rack-mount). The Management System is composed of: *i*) the Management server of MARCONI *A1*, in sharing with the FUSION fraction, is composed of 6 mgmt. servers LENOVO x3550M5 1U

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(rackmount) configured as above except for cpu having a INTEL Xeon E5-2600 v3 (Haswell); *ii*) the Management network is composed of 48 LENOVO RackSwitches mod. G8052: 48 ports 1 GbE, 4x uplink 10 GbE. The layout is 2 RackSwitch for each rack. The RackSwitch G8052 are linked to 2 LENOVO RackSwitch mod G8296 main switch: layer 3, 86 port 10 GbE and 10 ports 40 GbE.

The low-latency interconnection network is based on the new Intel Omni-Path fabric based on the product line Intel OPA 100 series running at 100 Gbps, the same than Infiniband Enhanced Data Rate (EDR), MARCONI is based on Tapered Fat-Tree (TFT) [6] network topology with a level “core” switches on the top of the level “edge” switch and an oversubscription of 2:1. The levels switch of MARCONI is composed of:

- 5 x OPA core switches Sawtooth Forest, Director Class 100 Series, 768 ports, 20U. The maximum configuration is : 5 core x 768 port x 2 tapering = 7680 nodes
- 42 x OPA edge switches Eldorado Forest, Edge Class 100 Series, 48 ports, 1U.

The TFT makes possible to interconnect an island of 32 nodes on a single edge switch. It is growing up to 216 x OPA edge switches to scale in MARCONI A2/A3. The fig.1 shows the TFT topology of the MARCONI OPA infrastructure.

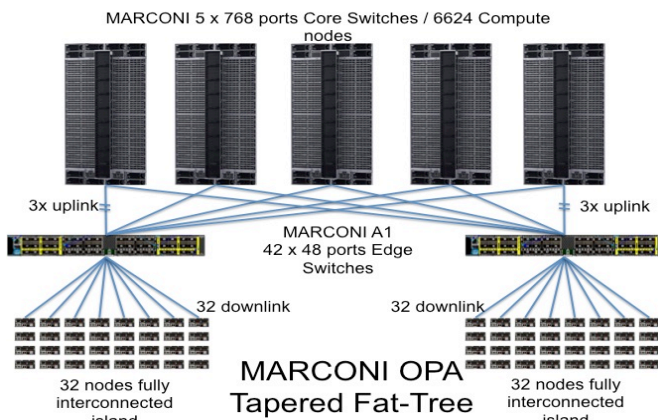


Fig.1: MARCONI Omni-Path infrastructure

The High Performance Storage (HPS) of MARCONI is based on LENOVO GPFS STORAGE SYSTEMs (GSS). It offers high performance on a scalable building-block approach. Performance and capacity increase adding server and disk enclosure. The current configuration of MARCONI HPS is composed of: 6 LENOVO GSS mod.26 each equipped with:

- 2 x 3650 M4 servers
- 6 disk enclosures
- 8 TB x 348 disk drives SATA

The current total capacity is about 17 PB raw and about 12 PB usable as filesystem.

AI PERFORMANCE TESTS

A set of performance tests were carried out in the Q2-2016 by CINECA SCAI team and LENOVO.

The main performance test of MARCONI AI was the *High Performance Linpack* (HPL) [7] benchmark that solve a dense system of linear equations. The HPL benchmark of MARCONI AI is ranked at 47th of TOP500 list of Jun 2016.

HPL	#MPI/# Thread	N/NB	Perf range
Single Node	1 / 36	104832 / 192 (90GB)	1.29 – 1.30 TFlops
Full System	1 / 36 for node	4320000 / 192 (90 GB)	1.6 – 1.72389 PFlops

Tab.2 The HPL test of MARCONI AI. Main parameters

The HPL benchmark on MARCONI AI is reported in the table 2. The HPL test was carried out disabling the *turbo* bios parameter in order to avoid the throttling.

The Intel[®] MPI Benchmarks (IMB) [8] perform a set of MPI performance measurements for point-to-point and global communication operations for a range of message sizes.

The generated benchmark data fully characterizes performance of a cluster system including: network latency, and throughput as well as efficiency of the MPI implementation used. The tests of MARCONI AI have been carried out in order to evaluate the performance of the Intel OPA network in the Tapered Fat-tree topology. Therefore two tests benchmark have been performed: *i*) at L0 level switch: for two compute nodes belonging the same edge switch; *ii*) at L1 level switch: for two compute nodes belonging to two different edge switch .

The IMB test *SendRecv*, is depicted in fig.1 to show the performance results of the bandwidth of MARCONI AI Intel OPA. The fig.2 plots the IMB *SendRecv* test for two switch levels: L0 (close nodes) and L1 (far nodes).

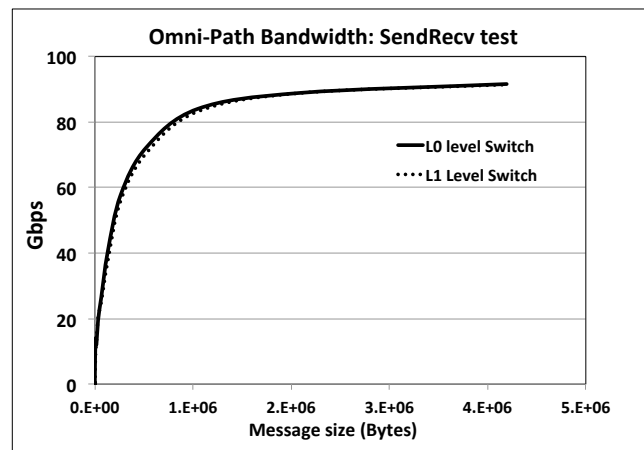


Fig.2: The IMB test. OPA bandwidth for two switch levels

The IOR [9] is designed to measure parallel file system I/O performance at both the POSIX and MPI-IO level. "IOR" stands "InterleavedOrRandom," which has very little to do with how the program works currently. This parallel program performs writes and reads to/from files under several sets of conditions and reports the resulting throughput rates. Using

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MPI-IO level the IOR benchmark measures the aggregate parallel I/O better than of single process I/O benchmarks. The aggregate performance of the High Performance Storage of MARCONI measured with IOR benchmark is reported in table 3.

IOR configuration	read max [MB/S]	write max.[MB/S]
124 compute node of 2 different racks	101477.89	97303.87
72 compute node of the same racks	101663.25	97658.31

Tab.3 The IOR benchmark of MARCONI A1

The MARCONI HPS aggregate performance measured are compliant with the technical requirements of 100 GB/s of bandwidth within the tolerance of 2 %.

MARCONI A2

MARCONI A2 is the second part of the new Tier-0 system, co-designed by CINECA and based on the Intel Server Board platform. It uses the same Intel OPA low latency network than A1. The table 4 shows the main characteristics of the MARCONI A2 and the dedicated fraction of MARCONI-FUSION as well.

The Compute Node of MARCONI A2 is based on Intel Server Board S7200AP. It's a 1/2U two-socket server supporting Intel Xeon V4, DDR4 memory at up 2400 MHz and DIMM capacities up to 64 GB, processor core up to 22 cores per processor. The Intel Server Board S7200AP provides to support the Intel Xeon Phi processor families Knights Landing-D/F. Four S7200AP compute nodes are inserted in Intel Server Chassis H2312XXLR2 purpose-built for high-density and lowest total cost of ownership in dense computing applications, such as HPC.

	MARCONI A2	MARCONI-FUSION
Model:	INTEL SERVER BOARD	
Architecture:	Intel OmniPath Cluster	
Nodes:	3600	340
Processors:	Intel Knights Landing (KNL) 1 x Xeon Phi 7250 (KNL) at 1.4 GHz	
Cores:	68 cores/node – Total=244800	Total=27200
RAM:	96 GB/node	
Racks:	50 + 1 (mgmt.shared)	~6+1 (mgmt. shared)
Peak Performance:	= 3 TF x 3600 nodes= 10.8 PFlops	= 3TF x 340 nodes= 1.02 PFlops
Disk Space:	17 PB (raw)	5 PB (raw) of MARCONI A1
Power:	1300 kW	120 kW

Tab.4: MARCONI A2/FUSION main characteristics

The MARCONI A2 compute node configuration is the following:

- 1 x CPU Intel Xeon Phi Knights Landing-D 7250 68 cores at 1.4 GHz (272 cores with Hyper-threading).
- 6 x 16GB DIMM of RAM DDR4 2400MHz
- 1 x 120GB SSD DCS3510 SATA 6Gbs MLC
- PCSD Accessory-Remote Management Module
- 1 x Fabric - Intel OPA HFI 100 Series 1Port PCIe 16x, 2 Link 1GbE.

The 3600 compute nodes SF7200AP are packaged in 900 Intel Server Chassis assembled in 50 racks 42U. A water based free cooling system is installed for lowering the air temperature in the computer hall by means a rear door heat

exchangers on each rack. The low-latency Interconnection Network is the same infrastructure than MARCONI A1 based on Omni-Path.

KNL is a many-in-core processor able to perform massive thread and data parallelism with high memory bandwidth [10]. It is a stand-alone, self-boot processor starting from standard operating system and connect to a network directly via standard interconnects such as: Infiniband, Ethernet or Omni-Path. KNL offers over 3 TFlops of double precision and 6 TFlops of single precision peak floating performance. It introduces a new memory architecture utilizing two types of memory: MCDRAM a high bandwidth memory (400+ GB/s) and the standard DDR4. It is binary compatible with prior Intel processors. KNL introduces the 512-bit Advanced Vector Extensions (Intel AVX-512). These new instruction set are consistent with the previously AVX-256 and AVX2 vector instructions. The AVX-512 instructions will be supported in the future Intel Xeon Skylake processors as well. KNL introduces optional on-package integration of the Omni-Path architecture enabling direct network connection. AVX-512 has been defined with programmability in mind. Most AVX-512 programming occurs in high-level languages, such as C/C++ and Fortran, through vectorizing compilers and pragmas to guide the compilers or via libraries with optimized instruction sequences, which may use intrinsic.

The design has a concept of a *tile*, which is the basic unit for replication. Each tile, consists of two cores, two vector-processing units (VPUs) per core, and 1 MB of L2 cache shared between the two cores. These tiles are physically replicated 38 times on KNL, however at most 36 of them are active; the extra two tiles are present to improve manufacturing chip yield and are disabled..

The tiles are interconnected by a cache-coherent 2D mesh on-die interconnect in order to access data stored in L2 caches of others tiles. The 2D mesh on-die interconnect architecture is based on a ring topology. The mesh supports three modes of clustered operation, which provide different levels of address affinity to improve performance. These are: *i)* All-to-All mode, *ii)* Quadrant mode with Hemisphere variant and *iii)* sub-NUMA clustering (SNC4/2) mode. All the L2 caches are kept coherent in the mesh with a protocol where each tile has a directory (*tag directory*) which together make up the DTD: Distributed Tag Directory which identify on the chip the location of any cache line. If a tile cannot find some data from its own local cache then it must query the DTD to find the data.

For MARCONI A2 quadrant mode is the default. Switching from quadrant mode to an SNC mode may boost performance for some applications, generally using more than one MPI rank on a single KNL.

The KNL high-bandwidth memory MCDRAM is integrated on-package grouped in 8 modules of 2 GB size each. The aggregate bandwidth measured with *Streams* benchmark [11] is over 450 GB/s. The memory can be configured at boot time in one of three modes : *i)* *cache mode* - where MCDRAM is like a L3 cache for DDR4. It is transparent for programming; *ii)* *flat mode* – where MCDRAM treated like a

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standard memory in the same address space as DDR4. It needs to be aware of how to use the memory in the software code; and *iii) hybrid mode* – where a portion of MCDRAM is cache and the remaining is flat. The 392 KNL nodes of MARCONI A2 Fusion partition are: 144 nodes configured in *flat mode* and 248 nodes in *cache mode*. DDR4 offers high capacity memory that is external to the KNL package. There are two DDR4 memory controllers, on opposite sides of the chip, each controlling three channels. The total memory capacity will depend on the capacities of the DIMM used, but the maximum total capacity is 384 GB, assuming 64 GB DIMMs per channel. The aggregate bandwidth measured with *Streams* benchmark for all six channels is ~90 GB/s..

The KNL hardware of Marconi (processors) works in standalone mode which removes limitations of the previous generation of Intel Xeon Phi (coprocessors) both in terms of performance (bottleneck of moving data from a processor to a coprocessor by a PCIe bus) and in terms of ease of programming.

A2 PERFORMANCE TESTS

A set of performance tests were carried out during Q3-2016 by a CINECA SCAI team and LENOVO.

The main performance test of MARCONI A2 was the *High Performance Linpack* (HPL) benchmark that solve a dense system of linear equations.

HPL	#MPI /# Thread	N / NB	Perf range
Single Node	1 / 64	40000 / 336 (12GB)	1.9 TFlops
Full System	1 / 64 for node	6287568 / 226 (83 GB)	6.22 PFlops

Tab.7 The HPL test of MARCONI A2. Main parameters

The HPL benchmark of MARCONI A2 is ranked at 12th of TOP500 list of Nov. 2016. The HPL benchmark on MARCONI A2 is reported in the table 7.

III. OPERATIONS

MARCONI FUSION is provided to EUROfusion by ENEA and CINECA under the Project Implementing Agreement (PIA) with a set of Key Performance Indicators (KPI) aiming at measuring the availability and the usage of the different partitions and the IT infrastructure (long term storage, network) including users support. In particular the availability of the HPC system is provided monitoring the availability of the main services, such as: users access, GPFS filesystems and PBS resources. The monitoring of KPIs is done during monthly operation committee meetings aiming also at tuning the operation parameters of MARCONI-FUSION in order to provide the best service to users. During the first months of operation of Marconi-Fusion frequent problems connected to the interconnection network (OPA) and the parallel file system (GPFS) affected the availability of the supercomputer. The availability and usage performances is getting better, as shown in fig.3, thanks to the efforts of a task-force composed of CINECA, LENOVO, INTEL and IBM.

The base operating system of MARCONI is Centos 7 and the software resources: compilers, scientific libraries, data analysis tools and debuggers are available in a module environments. They are grouped in different profiles and organized by functional category (compilers, libraries, tools, applications..).

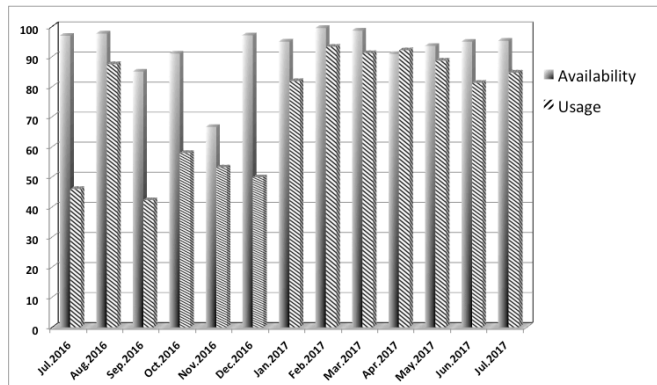


Fig.3: MARCONI A1 Availability/Usage performances

The batch jobs are managed by the PBS batch scheduler that provides the exclusive exploitation of MARCONI FUSION to the EUROfusion projects.

IV. GATEWAY

The Project Committee of MARCONI FUSION commissioned to ENEA/CINECA to provide a new Gateway [12] at CINECA working from 01.01.2017 to 31.12.2018. It integrates the Gateway resources offered by ENEA/CINECA with Hardware/Software resources belonging to MARCONI FUSION and new services. Furthermore a set of virtual nodes, of CINECA cloud infrastructure, are deployed to manage the administrative services like: authorization, authentication, ticketing system, wiki site, etc. The activities of installation and configuration of the resources including users data transfer to the new Gateway at CINECA Data Centre, embedded to MARCONI Tier-0 facility, have been carried out from middle Sep.2016 to Dec.2016 by ad-hoc working group composed of ENEA/CINECA support and CPT. Gateway operations started on Jan.1st 2017 with the access to a restricted group of users whilst the full users access started on Feb.1st 2017.

V. CONCLUSIONS

The new MARCONI-FUSION HPC facility for the European community of nuclear fusion modeling is in operation since Jul. 2016 under ENEA/CINECA handling. It is deploying by means a roadmap allowing to exploit the newest technologies of CPUs.

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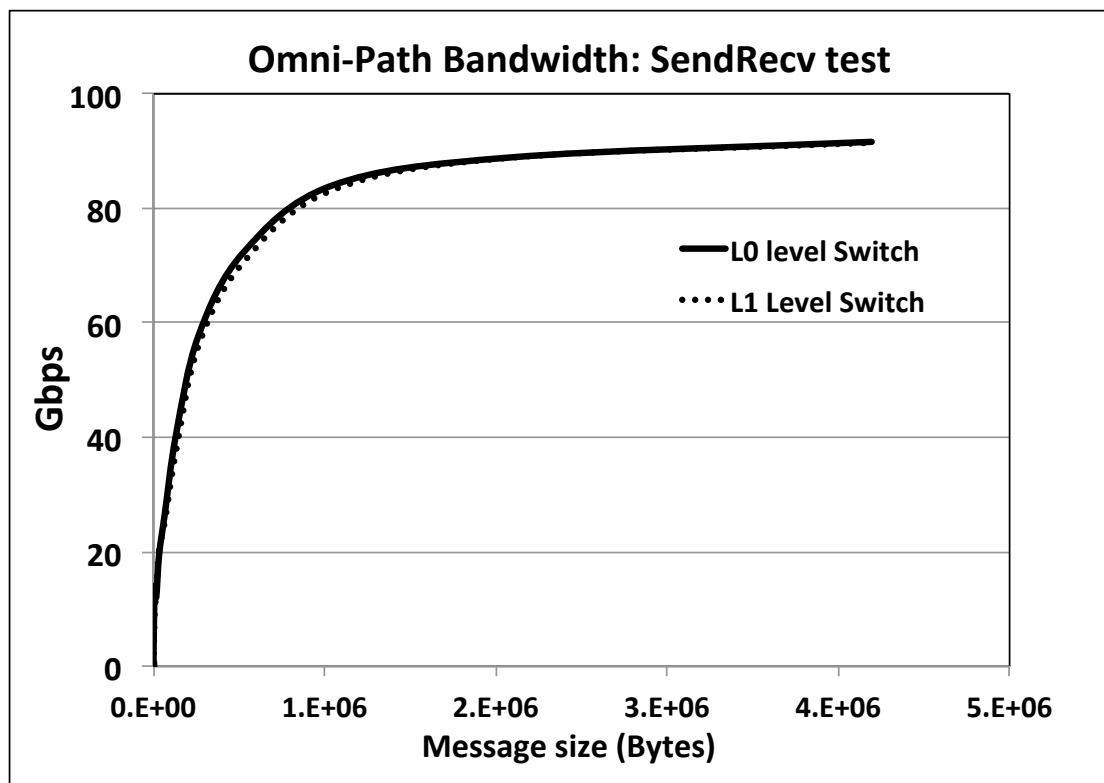


Fig.1