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Designing Multi-Level Resistance States in Graphene Ferroelectric Transistors

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Conventional memory elements code information in the Boolean "0" and "1" form. Devices that exceed bistability in their resistance are useful as memory for future data storage due to their enhanced memory capacity, and are also a necessity for contemporary applications such as neuromorphic computing. Here, with the aid of an experimentally validated device model, design rules are outlined and more than two stable resistance states in a graphene ferroelectric field-effect transistor are experimentally demonstrated. The design methodology can be extrapolated for on-demand introduction of multiple resistance states in ferroelectric transistors for applications both in data storage and neuromorphic computing.

1. Introduction

Resistance switching in 2D-material-based ferroelectric field-effect transistors (Fe-FETs)[1] is achieved by modulation of charge carrier density and thereby conductance of the 2D material by polarization of the ferroelectric gate dielectric.[2–10] The binary states, "0" and "1," are programmed by switching from one polarization state to the another by applying a bias that exceeds the coercive bias, V_C, of the ferroelectric gate.[20–23] Graphene has been the workhorse of the 2D material family. Demonstration of wafer-level upscaling of graphene Fe-FETs,[13–19] on flexible foils,[23–27] and even fully solution-processed graphene Fe-FETs[19] has supported the proposed application of 2D materials for high-speed nonvolatile memories.[11,12]

The conventional Fe-FETs have a Boolean "0" and "1" output.[28–30] The binary system is simple but offers limited data storage capacity as every bit of information (0 and 1) is translated to one of the two possible states. Multi-valued storage devices have been proposed to alleviate the limited storage capacity of the binary devices.[31,32] For instance, in a quaternary memory, the information is coded into one of the four possible states of 0, 1, 2, and 3 that together represent the information of two binary bits and are represented by 00, 01, 10, and 11, respectively. In comparison, for a 16 × 16 bit array, the binary system offers 256 bits, offering 2^{256} possible states, while at the same time, the quaternary system offers 4^{256} (or $(2^{256})^2$) possible states. A quaternary graphene Fe-FET would require four different conductance levels at zero gate bias. Despite the technological promise, multi-bit 2D material Fe-FETs have not been extensively studied.[12,32,33]

Memory devices also play central role in the hardware-based implementation of artificial neural networks (ANNs).[45] The figure of merit in this hardware-based approach is the mapping of the coupling between neurons that are found in biology (also known as synaptic weight) in the device memory state.[46] This synaptic weight is usually regarded as a continuous variable in biology, and therefore it is more biologically realistic to be emulated with analogue memory devices.[47] It is now well-known that core functions of ANNs, such as vector-matrix-multiplication, can be implemented on a crossbar array of analogue memory devices.[47–50] Despite the fact that nowadays research is quite intense in the field of analogue memory devices for synaptic electronics, the representation of synaptic weight with lower precision (i.e., few bit-memory) is still a viable route for the implementation of ANNs.[51,52] This approach represents a trade-off between precision in synaptic weight mapping and data volume during transfer,[49] and even allows for the potential implementation of hardware-based ANNs with devices that lack intrinsic analogue memory phenomena. Among other devices, a few examples of 2D or semiconductor Fe-FETs that exhibit gradual modulation of resistance have been reported in the past.[53–56] However, specific design principles for on-demand introduction of the number of states in Fe-FETs based on the needs of a specific application have not been reported yet.

Here, we design and experimentally demonstrate graphene Fe-FETs with four resistance states (quaternary) and generalize the design to exceed four states in a graphene Fe-FET. The Fe-FETs are realized with graphene grown from chemical vapor deposition (CVD) technique that are gated with a ferroelectric polymer poly(vinylidenefluoride-*co*-trifluoroethylene) (P(VDF-TrFE)). We hypothesize that the methodology developed can be used for any combination of 2D materials with both organic and inorganic ferroelectrics, provided that the correct material

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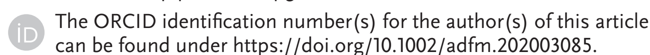

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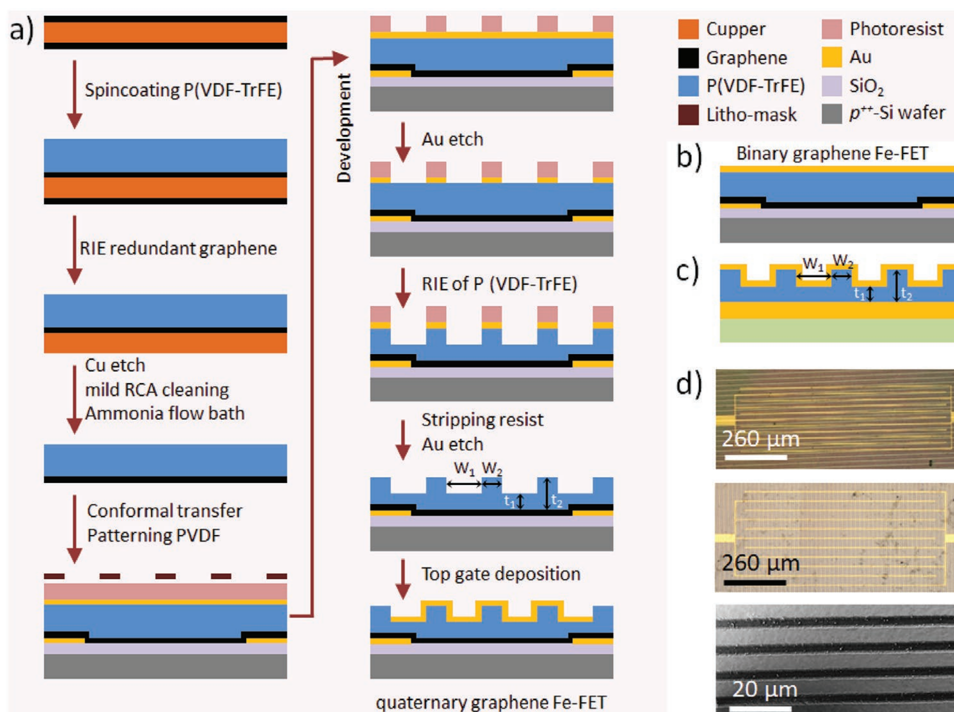

Figure 1. a) Process flowchart of quaternary graphene Fe-FETs. b) Schematic of a conventional binary graphene Fe-FET. c) Cross-sectional schematics of the patterned P(VDF-TrFE) capacitors. d) Optical photograph of the graphene/P(VFD-TrFE) layer that is transferred on to prefabricated interdigitated Au electrodes with (top) pattern parallel and (middle) perpendicular to the graphene channel. Bottom: SEM image of the patterned P(VDF-TrFE) layer.

description is taken into consideration. The methodology allows for developing memory cells with multiple number of states that are predefined through design. The results provide valuable guidelines for realization of multi-level ferroelectric transistors for applications ranging from data storage to neuromorphic computing.

2. Experimental Section

CVD graphene grown on copper (Graphenea) was coated with P(VDF-TrFE) (65–35% mole %) (Solvay). A layer of P(VDF-TrFE), with thickness of 800–1500 nm, was spin-coated onto the graphene-coated copper foil from a 10 wt% methyl ethyl ketone (Sigma-Aldrich) solution. Doping-free transfer of the graphene was done according to previous reports.[58] The graphene layer on the uncoated copper surface was removed by oxygen plasma. After etching Cu in 1 M aqueous bath of $FeCl_3$, the floated graphene/P(VDF-TrFE) layer was thoroughly washed using deionized (DI) water and a continuous flow bath of NH_3:DI-water (1 M) for 30 min. Subsequently, the graphene/P(VDF-TrFE) layer was transferred on to the pre-patterned FET substrate using the conformal transfer technique. The interdigitated Ti/Au (2 nm/150 nm) source-drain electrodes with a fixed channel width of 10 000 µm and a varying channel length of 10–40 µm, Figure 1d were fabricated by conventional photolithography on 6 in. Si wafers with 250 nm hexamethyldisilazane-passivated, thermally grown SiO_2.

The stack was dried at 40 °C for 12 h in a vacuum oven at 1 mbar, and then annealed at 140 °C for 2 h to enhance crystallinity of the P(VDF-TrFE) layer. The fabrication process of Fe-FET was completed by evaporation of a 100 nm gold top gate electrode through a shadow mask.

Patterned P(VDF-TrFE) layers for capacitors and gate structures, Figure 1c, were realized by performing an additional photolithography step. A layer of Au was deposited onto the P(VDF-TrFE) film and patterned. The underlying Au electrode lines were used as a cue for the alignment of the top patterns. It was noted that a slight misalignment of the etching lines with the Au contact lines would not affect the experimental observation. For down-scaled device, proper alignment of the pattern with the electrodes is required. Patterns parallel and perpendicular to the graphene channel, as shown in Figure 1d, were realized. The exposed Au stripes were etched in $KI/I_2/H_2O$ (4:1:4) solution. Subsequently, the exposed P(VDF-TrFE) was etched using reactive ion etching (RIE) with a plasma power of 150 W, at a pressure of 0.08 mbar, and oxygen/Ar flow of 30/10 sccm (etching rate of 330 nm s^{-1}). The etching depth was controlled by RIE etching time. Note that the etching rate was chosen due to the large thickness of the P(VDF-TrFE) layer. For thinner P(VDF-TrFE) films, required in application, the etching rate should be substantially lower to allow for good control of the etching depth. After the etching process, the redundant photoresist and Au cover layer were stripped and etched, and the substrates were thoroughly rinsed in DI water. The photoresist was removed after the RIE process because the resist remover solvent dissolves P(VDF-TrFE) layer. Patterned graphene Fe-FETs and capacitors were finalized by evaporation of a top Au electrode (150 nm). The flow chart of the fabrication process is given in Figure 1a. Trenches are patterned parallel to

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the interdigitated electrodes (Figure 1d). All electrical measurements were performed in high vacuum (10^{-6} mbar) using a Keithley 4200 semiconductor characterization system. The Fe-FET measurements were performed by application of a small bias of +50 mV to the drain, and the drain current was monitored while changing the gate bias. The retention measurements of the programmed states in Fe-FETs were performed at zero gate bias while a bias of +50 mV was applied to the drain.

2.1. Multi-Bit Graphene Memory through Design

An analytical model was previously developed that coupled voltage-dependent charge displacement of the ferroelectric gate layer with the charge transport across the graphene channel.[57] To extend the formalism to multi-bit graphene Fe-FET, the geometrical topography was incorporated in the charge displacement description of the ferroelectric gate layer. The displacement, D, of a ferroelectric gate layer with a constant thickness, t, is the sum of the linear dielectric response and the ferroelectric polarization and is given by

$$D = \varepsilon_0 \varepsilon_P E + P(V,t) \quad (1)$$

where $E(=V/t)$ and $P(V)$ are the electric field and ferroelectric polarization, respectively. Voltage-dependent polarization of the ferroelectrics can be described phenomenologically using

$$P^+(V,t) = \varepsilon_0 \varepsilon_P \frac{V}{t} + \frac{P_2}{2} f(V,t) \quad (2)$$

with

$$f(V,t) = \left(\tanh\left(\frac{V+V_c}{t.\delta} \right) + \tanh\left(\frac{V-V_c}{t.\delta} \right) \right) \quad (3)$$

and

$$\delta = 2\frac{V_c}{t}\left[\ln\left(\frac{1+P_r/P_S}{1-P_r/P_S} \right) \right]^{-1} \quad (4)$$

where V_c, P_s, and P_r are the coercive bias, saturation polarization, and remanent polarization of the ferroelectric layer, respectively. The $P^+(V)$ functional denotes the lower branch of the polarization loop, going from negative bias and polarization towards the positive values. The negative branch, $P^-(V)$, is calculated using $P^-(V) = -P^+(-V)$.[35,36] Equation (2) describes the D–V loop of an unpatterned P(VDF-TrFE) ferroelectric capacitor with a good accuracy, as shown in **Figure 2**a.[39–44] The best fit is obtained using the following parameter values: $\varepsilon_P = 15$, $P_r = 75.09$ mC m^{-2}, $P_S = 75.1$ mC m^{-2}, and $E_C = (V_c/t) = 60$ MV m^{-1}, which are the typical, experimentally reposted values for P(VDF-TrFE).

Writing the $P(V)$ functional in terms of voltage allows for generalizing the formalism for the patterned P(VDF-TrFE) capacitor as follows

$$P^+(V) = \sum\nolimits_{i=1,2} \left(W_i \times P(V_i, t_i) \right) \quad (5)$$

where W_i and t_i are areal fraction and thickness (nm) of the respective fraction of the patterned P(VDF-TrFE) film, as schematically shown in Figure 1c. Capacitors with various fractional areas were tested. Representative experimental D–V loop of a capacitor with $W_1 = 0.25$ and $W_2 = 0.75$ is shown in Figure 2b. Using Equation (5) and the parameters resulting from the fit to Figure 2a, combined with the geometrical parameters of (W_1, t_1) = (0.25, 400 (nm)) and (W_2, t_2) = (0.75, 800 (nm)), a good description of the D–V loop was obtained for the patterned P(VDF-TrFE) capacitor as shown in Figure 2b.

The polarization of the ferroelectric gate layer changes the effective gate bias experienced by the graphene layer

$$V_{\text{eff}} = V_G - V_D + \frac{P^{\pm}(V_G)}{C_P} \quad (6)$$

where V_G and V_D represent gate and Dirac voltage, respectively, $\frac{P^{\pm}(V_G)}{C_P}$ is the polarization-induced voltage, and C_P is the geometrical areal capacitance of the P(VDF-TrFE) gate layer in F m^{-2}. Assuming that the remanent and saturated polarization of the ferroelectric gate in Fe-FET remains the same as those in the capacitor, and 100% coupling of the ferroelectric polarization

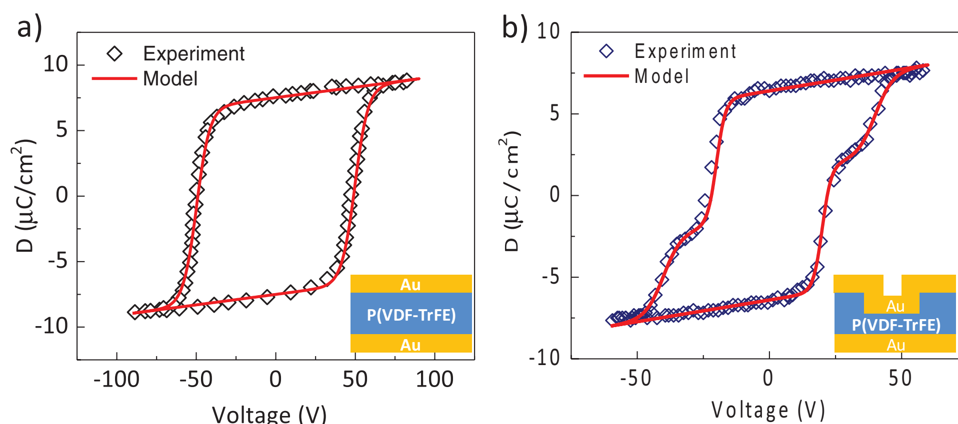

Figure 2. D–V loop of ferroelectric capacitors (insets) with a) a uniform and b) patterned P(VDF-TrFE) films. The solid red lines show the fits produced by the phenomenological model.

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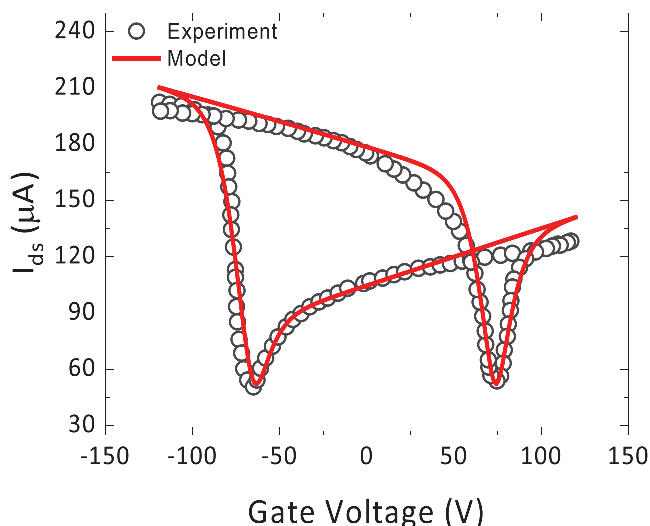

Figure 3. Transfer characteristics of a graphene Fe-FET with unpatterned plane P(VDF-TrFE) gate layer. The solid line shows the fit obtained using the analytical device model.

with channel conductance, hence ignoring depolarization,[37] the gate bias-dependent carrier density can be written as

$$n(V_G) = \frac{C_P}{e}\left(V_{\text{eff}} + \frac{b^2}{2e}C_P - b\left(\frac{V_{\text{eff}}C_P}{e} + \frac{b^2}{4e^2}C_P^2\right)^{\frac{1}{2}}\right) \tag{7}$$

where $b = \frac{\hbar v_f \sqrt{\pi}}{2e}$ appears due to taking into account the quantum capacitance of the graphene layer, $(2e^2\sqrt{n(V_G)})/(\hbar v_f\sqrt{\pi})$ with ħ and v_f are reduced Plank's constant and Fermi velocity of the carriers, respectively. The source-drain current, I_{ds}, in the graphene Fe-FET is then given by

$$I_{ds}(V_G) = V_{ds} \times \left(R_c + N_{sq}\left(\mu e\sqrt{n_0^2 + n(V_G)^2}\right)^{-1}\right)^{-1} \tag{8}$$

where R_c, N_{sq}, and μ are contact resistance of the metal–graphene junction, number of squares of the gated area, and charge carrier mobility of the graphene layer, respectively.

The model was experimentally validated by fitting the transfer curves for the graphene Fe-FETs with a plane, unpatterned P(VDF-TrFE) gate layer. The parameters obtained from the fits of the *D–V* loops of the P(VDF-TrFE) capacitor, Figure 2a, were used as the input parameters for the gate layer of the Fe-FETs. The model accurately describes the transfer characteristics of the graphene Fe-FET with constant mobility of μ = 800 cm^2 V^{-1} s^{-1}, and V_D = 285 V, as shown in **Figure 3**. The model describes well the Fe-FETs with unpatterned gate, and is therefore experimentally validated.

Based on the model, the operation of the graphene Fe-FET with a plane, unpatterned ferroelectric layer can now be accurately explained. Application of −125 V to the gate sets the P(VDF-TrFE) gate to its full positive polarization state, which is accompanied by accumulation of holes in the graphene channel. The hole current is persistent upon sweeping the gate bias toward zero and then further to positive gate bias. At ≈+75 V, the gate bias reaches $+E_c$, and P(VDF-TrFE) reverses its polarization. The negative polarization state is fully compensated by electron accumulation in the graphene channel, and the electron current prevails as the gate voltage increases further toward +125 V. The electron current persists upon sweeping back the gate bias to zero and down towards negative biases. At nearly ≈−75 V, the gate bias reaches $-E_c$ and the polarization of the P(VDF-TrFE) gate layer switches back to the initial positive polarization state, re-establishing the hole current. The presence of both electron and hole channels in the graphene Fe-FET is due to the ambipolarity of the CVD-graphene layer by removal of the unintentional doping.[58]

Following the experimental validation, the model is used to make predictions for Fe-FETs with patterned gates. To produce transfer curves, the parameters that are obtained for the graphene Fe-FET with un-patterned P(VDF-TrFE) gate are used. The transfer characteristics are calculated for the patterned structure perpendicular to the graphene channel by varying the factional area of W_1 (and W_2) from 0 to 0.50. A representative calculated *D–V* loop is given in Figure 2b for W_1 = 0.25 and W_2 = 0.75. The calculated transfer characteristics of the comprising graphene Fe-FETs with the same patterned P(VDF-TrFE) are shown in **Figure 4**a. The Fe-FET clearly shows four different conductance levels depending on the polarization configuration of the patterned gate layer. Due to the ambipolarity of the graphene layer, the intermediate polarization states are compensated and therefore stable in time, hence no depolarization of the gate layer is expected.[32,34]

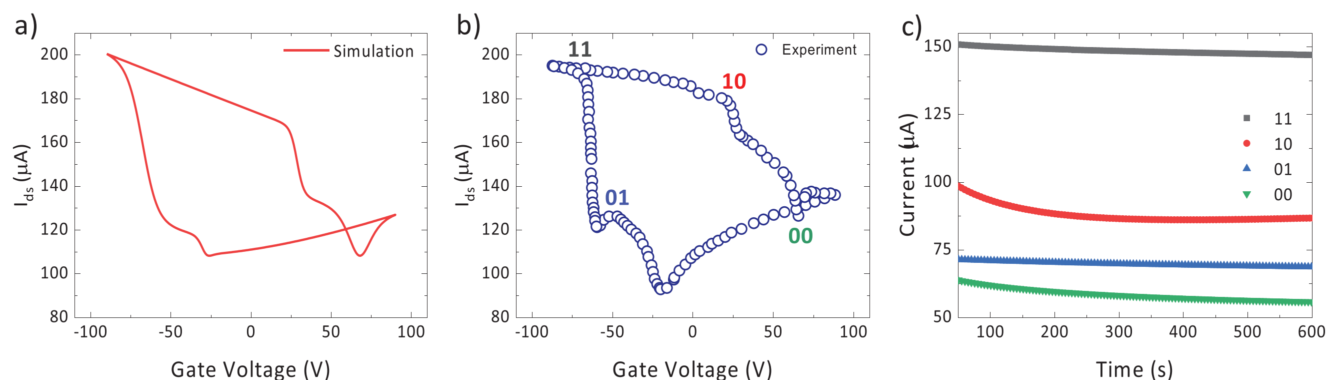

Figure 4. a) Model prediction of the quaternary graphene Fe-FET and b) experimental demonstration of the same device using a patterned P(VDF-TrFE) ferroelectric gate. c) Retention time of different states of the quaternary graphene Fe-FET measured at zero gate bias and a drain bias of +50 mV.

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The experimental transfer characteristics of the graphene Fe-FETs with patterned P(VDF-TrFE) perpendicular to the graphene channel is shown in Figure 4b. The P(VDF-TrFE) layer has the same pattern (W_1 = 0.25 and W_2 = 0.75) with a thickness of t_1 = 600 nm and t_2 = 1200 nm, respectively. Application of negative gate bias of –90 V sets the patterned P(VDF-TrFE) layer in the fully positive polarization state, and hole accumulation is formed in the graphene layer. Upon sweeping the gate bias towards positive biases, the drain current shows a sudden drop at a gate bias of ≈+30 V. The thin part of the P(VDF-TrFE) gate layer is now in negative polarization state. As gate bias approaches nearly +60 V, the thick part of the P(VDF-TrFE) layer is now in positive polarization state, and therefore the P(VDF-TrFE) layer is homogeneously in positive polarization. As a result, a uniform electron accumulation channel is formed in the graphene layer. Upon back sweeping the gate bias, the electron current persists. At a gate bias of ≈–30 V, the hole accumulation channel is partly retrieved. At gate bias –60 V, P(VDF-TrFE) gate layer is again in full negative polarization. The Fe-FET, depending on the programming of the gate layer, shows four different conductance levels that are stable in time as shown in Figure 4c, in the absence of the external gate bias. Therefore, the graphene Fe-FET has a quaternary output.

The Fe-FETs with parallel alignment of the pattern with respect to the graphene channel have shown similar transfer characteristics. A parallel alignment would yield series connection of the channel portions, where the highest resistive portion of the channel would dominate the transfer characteristics. The perpendicular alignment would produce channels that are connected in parallel, and where the currents add up. In the case of graphene, the difference between the high and low resistance states, as shown in Figure 3, is a factor of two, which apparently is not large enough to yield different transfer characteristics. Dissimilarity between the two alignments is expected when more resistive semiconductors than graphene are used.

It should be noted that for a relatively large-area device, where the ferroelectric layer is composed of many domains. Multi-level resistance[61,62] can also be realized by partial polarization of the ferroelectric layer into its intermediate polarization states[59,60] using a pulsing scheme. However, downscaling of the devices as eventually needed for neuromorphic applications can limit multi-value resistance. At device dimensions comparable with ferroelectric domain size, partial polarization of the ferroelectric layer, as to produce multi-levels of resistance, becomes challenging.[63] However, for a patterned ferroelectric gate, the precise control over the polarization, and therefore channel conductance, is straightforward, whereas for partial polarization, precise control of the polarization level can become challenging.

Realization of differentiable intermediate “01” and “10” states depends very much on the geometrical features, that is, the height and width of the pattern in the ferroelectric layer. To investigate the effect of the geometry on the transfer curve of the Fe-FET, both height and width are varied. In Figure 4a, the effect of variation in the height for a fixed W_1/W_2 of 0.25/0.75 is shown. The intermediate regime becomes more apparent as the height difference increases, as highlighted for the enlarged section of the transfer curve, where state “10” emerges. Since almost all ferroelectric thin-films are polycrystalline, they have a distributed coercive voltage. As a result, a

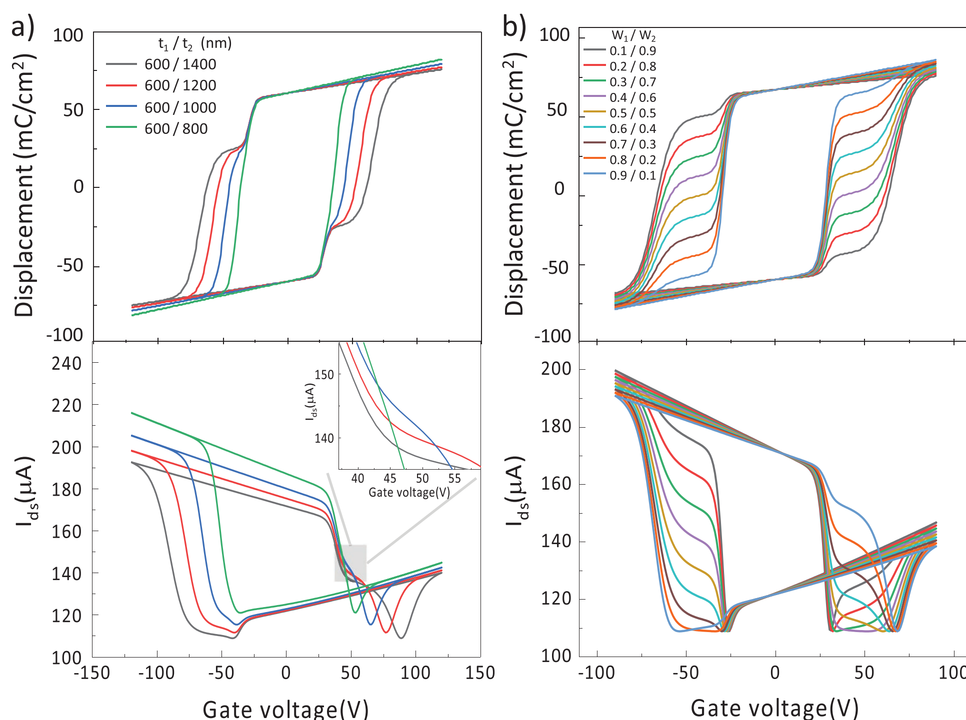

Figure 5. The effect of height and width of the patterns in the ferroelectric gate layer on the transfer characteristics of the graphene Fe-FET. a) The influence of different thickness for W_1/W_2 of 0.25/0.75 and b) the effect of the width for t_1/t_2 of 600/1200 nm.

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single switching voltage is absent and there is always a voltage distribution around V_c. For the Fe-FETs with patterned gate to have differentiable intermediate state, the height difference should be large enough to ensure that the V_{c1} and V_{c2} are well-separated and do not overlap. Therefore, as a design guide, an optimal height difference of 50% is suggested for clearly discernable "01" and "10" intermediate states in the transfer characteristics of the Fe-FET.

The influence of the width of the patterns on the transfer curve is presented in Figure 4b for a fixed height difference of 50%, and variable ratio of W_1/W_2. Changes in W have a distributing effect on the polarization, and consequently the current level of the intermediate "01" and "10" states. The minimum W, an important factor for downscaling of the patterned devices, could be as small as tens of nanometers because it was demonstrated that the ferroelectric domain can be stabilized down to tens of nanometer.[65]

The methodology of patterning the ferroelectric gate defines various switching voltages that allow for creating multiple number of resistance states that can be controlled deterministically. As a demonstration, the designs are provided for capacitors with three and four steps in the thickness of the ferroelectric layer, as presented in Figure 6a–c, respectively. The details of the design, namely the thicknesses and the fractional areal coverage of every thickness, are given in the legends of the Figure 6. Three steps in the ferroelectric film topography lead to six different polarization states, as shown in **Figure 5**a. Implementation of the ferroelectric layer as the gate insulator yields a Fe-FET that clearly shows six different resistance states, as shown in **Figure 6**b. Similarly, four steps in the ferroelectric film topography leads to eight different polarization states, Figure 5b, and consequently eight different resistance states in the Fe-FET, as shown in Figure 6d. It should be noted that the intermediate states are determined by measuring the current at zero gate bias, not at the coercive bias of the intermediate states. Since polarization of the intermediate states is compensated and, therefore, stabilized, the current level of the intermediate states will be, therefore, different and the intermediate states can be easily differentiated from one another.

A brief note should be given about the switching voltages in multi-level resistance states in patterned graphene Fe-FETs. For many applications, including memory and neuromorphic,

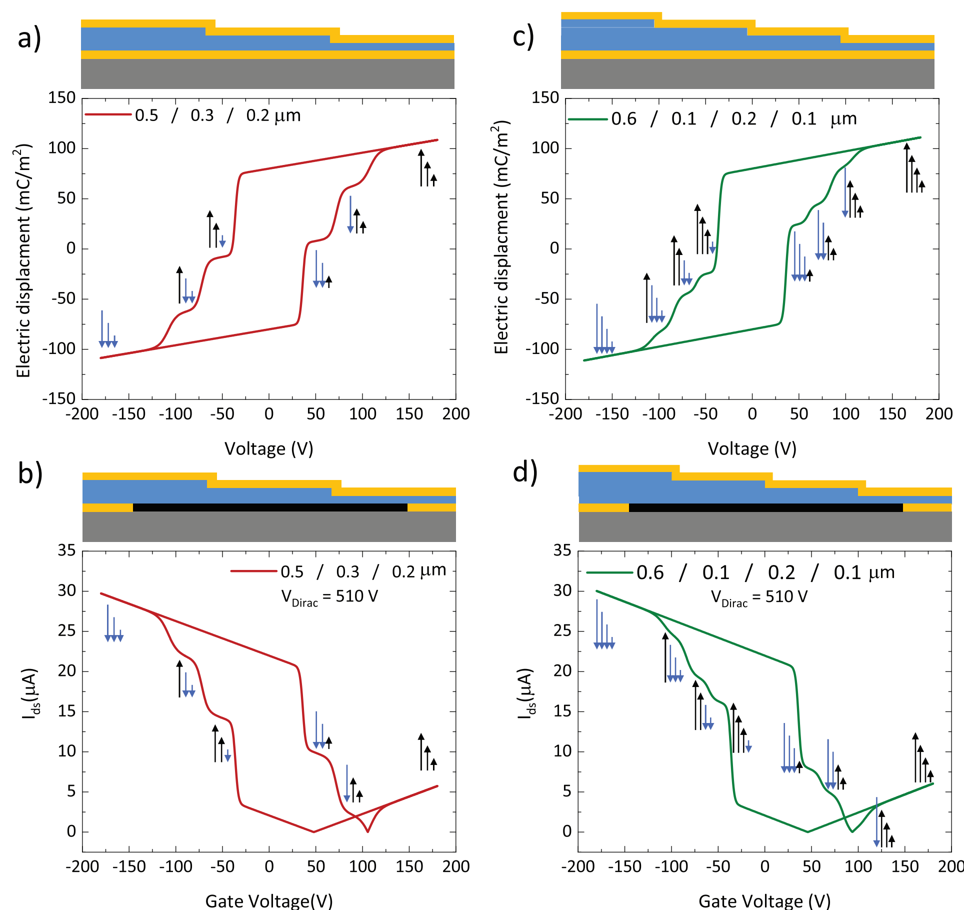

Figure 6. a) Schematic of ferroelectric layer with three topographic steps (top) and the simulated corresponding displacement–voltage characteristics in a capacitor (bottom). b) Schematic of ferroelectric transistor with three topographic steps (top) and the simulated corresponding transfer characteristics (bottom), clearly demonstrating six different resistance levels. c) Schematic of ferroelectric layer with four topographic steps (top) and the simulated corresponding displacement–voltage characteristics in a capacitor (bottom). d) Schematic of ferroelectric transistor with four topographic steps (top) and the simulated corresponding transfer characteristics (bottom), clearly demonstrating eight different resistance levels. The first row of the legend in every panel shows the fractional areal coverage for different thicknesses that are given in the second row below it.

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low-voltage operation of the resistance switching devices is required. The demonstrated patterned graphene Fe-FET operates at rather large voltages, because the primary goal is to demonstrate multi-level resistance switching and to establish the device physics. Nonetheless, the switching voltage of P(VDF-TrFE)-based memory devices could be reliably reduced to sub-3 V[38] upon reducing the thickness to below 20 nm. Therefore, low-voltage operation for the patterned Fe-FET could be realized by preparation of thinner P(VDF-TrFE) gate layers, which necessitated adoption of the P(VDF-TrFE) etching process to low etch rates.

3. Conclusion

Using an experimentally validated device model, we have outlined design rules for a quaternary graphene Fe-FET and experimentally demonstrated four stable resistance states of the designed graphene Fe-FET. By introducing a well-defined topographical pattern in the ferroelectric layer, four different switching voltages appear that enable programming of the gate polarization into four different states simply by application of an appropriate gate bias. We have predicted transistors with six and eight different deterministic resistance states. Based on the insight gained from the model, we propose introducing several trenches with various thicknesses within the ferroelectric gate layer to achieve multiple (>2) resistance states in a single transistor with deterministic resistance switching voltages. The device model presented here is generic, and can be adopted for graphene Fe-FETs that are fabricated with inorganic ferroelectrics or dual-gate ferroelectric transistor.[64] Analytical description for the dielectric displacement of the ferroelectric gate layer renders the proposed model applicable to other Fe-FETs based on various 2D materials. When the electrostatic description of the gate is coupled with an appropriate charge transport model, the model can determine the best operational conditions for the Fe-FETs based on the 2D material under study.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

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