Recent Diagnostic Developments at ASDEX Upgrade with the FPGA implemented Serial I/O System "SIO2" and "Pipe2" DAQ periphery

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ASDEX Upgrade (AUG) since many years has been using a built to purpose FPGA PCIe computer interface with fast serial interconnects – called "SIO" – connecting to peripheral crates based on a pipeline organized backplane – called "Pipe"[1][1] – containing modular DAQ devices. The combination of custom built input channels, aggregated into multi-channel FPGA controlled backplanes and streamed by one or more SIO2 FPGA cards via DMA into computer memory enables the deterministic delivery of data for real-time applications with minimum latency. The renewal of large diagnostics for the Mirnov probes, the Soft-X-Ray cameras and others have been successfully conducted. These diagnostics have undergone the transition from Solaris to Linux CentOS with real-time kernel. These systems, receiving a stream of measured samples from the SIO2 periphery via DMA, directly provide data for plasma control via sharing the DMA memory sections with dedicated application processes (APs) running on the same node as part of the AUG distributed discharge control system [2] [3]. The SIO2 DAQ is further applied to a Thomson-Scattering (TS) system located in the AUG Divertor (DTS). New GigaSample ADCs developed for this diagnostic expand the range of measuring periphery into the GHz range. The same ADCs are planned to be used to refurbish and real-time enable the main chamber Thomson-Scattering system. The paper describes the concepts of the "Pipe2" periphery and the "SIO2" interface card. It briefly summarizes specifics of the diagnostics mentioned above and puts further emphasis on design modifications of the FPGA firmware to address new requirements. It will also give a short description of the developed GSPS ADC/FPGA periphery cards.

Keywords: Data acquisition; Plasma diagnostic; Modular computer periphery; FPGA; Serial I/O; Thomson scattering

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1) "SIO" or "SIO2" and "Pipe" or "Pipe2" are the short names of the DAQ concepts described in this paper. The figure "2" in these names refers to the actual revision which is an extended version of the first approach developed already 2007.

1. Introduction

The ASDEX Upgrade Tokamak is a magnetic confinement experiment in operation for nearly 30 years. The experiment as well as its data acquisition in these years has undergone multiple modifications and transformations[1-3]. Having started with a unique software and hardware design featuring a general data structure [4] and a distributed concept of DAQ (abbreviations see Table 1) nodes [5] (reviewed with further references in Ref. [6]) system concepts have diversified in these past three decades but it was always intended to maintain a main concept for the majority of diagnostics. Simultaneously it was sought to keep the DAQ development compatible with the genuine baseline design. So over the years an in-house standard for DAQ systems was developed [7] which as much as possible decouples the extremely volatile progress in information technology from the well known but very particular and demanding diagnostics requirements of the experiment which were never completely addressed by commodity devices. This standard is meant to be adaptable to new technology, customizable for multiple requirements, expandable to growing demands, suited for real-time applications, extendable by public domain knowledge, and thus widely adaptable to new situations.

The design already presented in Refs. [7] and [8] shall not be subject of this paper. However, describing recent developments with respect to the base concept we will try to make clear what is meant by adaptability, customizability, expandability, real-time fitness, and open design extendability. This is achieved by the modularity of the design and by using FPGAs to implement the internal logic of the building blocks.

Table 1: Common abbreviations used in this paper without further explanation

ADC	Analogue to digital converter – a chip or device converting an analogue input signal varying over time into a series of digital values
AMP	Amplifier
DAQ	Data acquisition
DCS	Discharge control system
DMA	Direct memory access – a method to transfer data from a device into host memory under control of the periphery device without intermediate processor intervention
FPGA	Field programmable gate array – a chip designed to be configured with respect to its logical function by firmware
GSPS	Giga samples per second – taking data samples with a GHz clock frequency
IT	information technology
PCIe	Peripheral Component Interconnect Express – a computer periphery bus standard featuring one to multiple serial lanes today often connecting directly to the CPU
PCB	Printed circuit board

2. SIO2 and Pipe2 concepts

In fact the AUG serial I/O DAQ concept consists of two major pieces which are the Serial I/O

(SIO) computer interface and the "Pipeline" modular analogue to digital (or vice versa) peripheral device architecture. Differing from other DAQ concepts which integrate multiple DAQ channels and computer interface on the same PCB the SIO2/Pipe2 concept separates both into a more or less general purpose computer interface and the Pipe2 modular periphery hardware concept.

Today's Pipe2 architecture is an extended revision of the former Pipeline form factor featuring larger printed circuit board (PCB) format, enhanced power supply, and temperature management concepts to address the needs of modern large integrated circuits (ICs) like FPGAs. The underlying concept originated from the idea to break the complex design of all-in-one multi-channel transient recorders into pieces in order to modularize large multi-channel DAQ systems and simultaneously to separate and simplify the customizability of input channels.

SIO was developed to complement the Pipeline architecture with a computer interface providing the intended detachment between periphery and computer. Likewise SIO is designed to multiplex (merge) sample streams[2] from up to four Pipelines and one central time counter. (How Pipe2/SIO2 create merged sample streams is described below.) The final transfer direct into memory of the host computer occurs via DMA. Between time of sampling and the arrival of sampled values in computer memory a minimum delay (latency) is maintained as buffering of only one sample step is foreseen in the merge and transfer process[3]. Thus a maximum overall sustained data rate of 200 MiB/s from periphery to host memory[4] is achieved with the SIO2 implementation. Restricted to a consistent sampling rate for all channels on one SIO card, the number of channels and the sampling rate can be flexibly chosen observing the rule $\quad 2\ n_{channels}^{5}\ r_{sampling}\ \leq\ r_{data\text{-}max}\quad$.

2.1. Separating multichannel transient recorder functionality into modules

Off-the-shelf transient recorders come typically with a full bundle of DAQ functionalities: multi purpose analogue input channels configurable for a wide range of applications, sensitivities and signal bandwidth, a widely adjustable time resolution, an internal analogue or digital multiplexer to allow a flexible choice of channels, flexibly manageable internal memory, a complex configuration engine (sometimes a complete embedded computer system) and an internal storage and filesystem. The interfaces of such systems vary in media and protocol. To integrate these fully featured systems into an in-house diagnostic design additional host software is required, which is often proprietary, closed source, and platform dependent. Adapting proprietary device drivers and application libraries to one's own system

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2) The term "sample" is used in the sense of a single data element out of the chain of digitized discrete amplitude values of an analogue continuous time signal. See e.g. https://en.wikipedia.org/wiki/Sampling_(signal_processing) for a general definition of "sampling". A stream of samples in our meaning not only characterizes the data chain stemming from one signal but may describe also the stream of multiplexed data values from a multi-channel sampling device.

3) A FIFO buffer which is large enough to bridge short DMA transfer outages is implemented. However, an optimally configured and low latency tuned host computer would not interrupt running DMA transfers for a noticeable delay.

4) Provided the host computer memory is not overrun.

5) $n_{channels}$ is restricted to multiples of four due to a 64-bit alignment of all transfer buffers.

design is often difficult and cumbersome.

On the contrary, the requirements of diagnostics mostly are well defined, very specific and sometimes also very special. Nevertheless, designing a single input channel to a particular well defined purpose is mostly not that complicated. So breaking the above described complex transient recorders into simple modular pieces starts with defining an analogue signal conditioning and digital conversion function group as a module which is as simple as possible yet as versatile and customizable as required.

In general the output of such a function group is a series of digital values (words or blocks of words) over time. And mostly the time base can be defined as a continuous uniformly clocked stream of time values. Sometimes it is divided in bursts which can be periodic or event driven. Typically large fusion devices ask for a high number of similar channels for each type of diagnostic to allow for a high spatial resolution or simultaneous measurements at many locations. And typically all channels of a diagnostic are triggered and clocked synchronously.
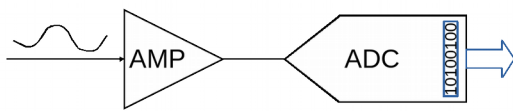

Figure 1: Base schematic of a single channel Pipe2 module carrying the basic functions: signal input conditioning, analogue to digital conversion, and digital output.

Figure 1 – depicting a single Pipe2 module – summarizes in a symbolic sketch what the Pipe2 concept defines as a module. In fact it's a standard PCB form factor carrying just the mentioned function groups: input socket, signal conditioning amplifier, anti-aliasing filter, sampling circuit, ADC (analogue digital converter), and a 16-bit output register. A backplane plug as rear interface connects the module to the backplane allowing aggregation of multiple modules in series.

While this is only a symbolic view of an ADC module, the real wealth of peculiarities of the Pipe2 module concept is demonstrated by the already available function modules listed in Table 2 [6].

Name of module / diagnostic	Sampling Rate	Resolution	Channels/module	Built #
± 10V ADC (ECE imaging)	900 kHz	14 bit	4	100
± 10V ADC	250 kHz	16 bit	4 (synchr.)	90
Fringe counter (Interferometry)	50 kHz		1	6
2-ch 8 bit latching scaler	na	8 (16)	2 (1)	44
General ± 10V ADC	2 MHz	16 bit	4	70
HotLink I Rcv. (Mirnov/SXR)	16 MHz $\triangleq$ 2 MB/s	2 Byte	4	140
1 GSPS ADC (TS)	1.25 GHz	14 bit	2 (synchr.)	75
± 10V ADC (Doppler backscattering)	20 MHz	16 bit	2	6

Table 2: List of a selection of periphery modules for the Pipe2/SIO2 concept. (Technical details up to the detail level of circuit design and manufacturing layouts can be provided on request by the authors.)

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6)   The respective designs and documentation can be provided for free on request. Language is German.

2.2. Assembling diagnostics from modules

Diagnostics typically need multiple channels of the same kind. As already mentioned Pipe2 features a backplane to hold the modules and transport data pipeline-wise upstream[7]. Figure 2 gives a schematic view of such a backplane. The rightmost slot (slot 0) of each Pipe2 backplane is always reserved for the Pipe2 controller card. This controller card not only provides a fast serializer to send data coming from the pipeline up the serial link, but also provides a slower bidirectional communication between host and the modules for configuration and testing.
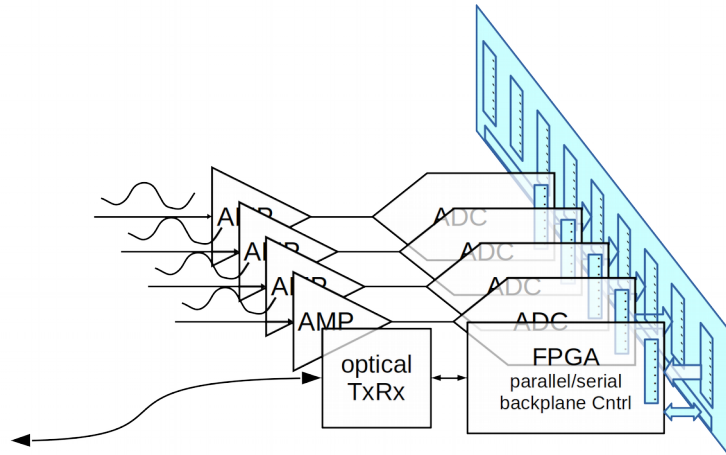
Figure 2: Pipe2 backplane providing eight slots of which four are populated with ADC modules while the rest is empty. The first slot is used for the uplink controller card. (See the online material for a PDF containing a sequence of slides showing the assembly of a PIPE2 crate starting with an empty backplane, populating it with modules, and depicting the steps of a single data sampling run. This image sequence is also available as a short animation illustrating the operation even more catchy.)
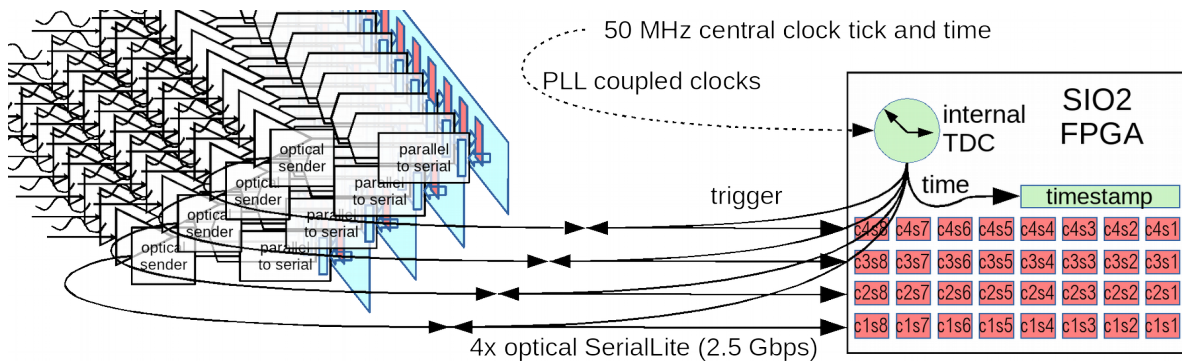

Figure 3: Four fully equipped Pipe2 crates connected to a SIO2 computer interface deploying a multiplicity of channels for a diagnostic. The internal TDC's 64-bit time counter of the internal clock is synchronized and PLL coupled with the central experiment clock tick. DAQ triggers and time stamps are internal generated by the TDC timing engine.

Pipe2 backplanes can be built with a flexible number of ADC slots from one to twenty[8]. Typically a diagnostic consists of multiple backplanes built to purpose in number and length to match the required number of channels and the maximum desired sampling rate. The uplinks of up to four backplanes can be connected to one SIO2 computer interface. A fully equipped SIO2/Pipe2 system then could look like shown in Figure 3. [9]. It should be

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7) Of course there is a down stream communication channel for configuration and control, but the main feature of the concept is its massive low latency upstream data acquisition capability.

8) In fact the maximum form factor derives from the width of a 19" crate.

9) A detailed Pipe2 description can be provided for free on request (contact the author) under a public commons license without any warranty for fitness, usability, safeness or reliability. Designs are in their last released form which might not contain latest modifications made during production. Language is German.

mentioned that the time is recorded in the SIO2 cards timing logic only, but since the periphery is stiffly synchronized to this logic no time skew is possible (also see below).

2.3. Managing DAQ timing with the SIO2 TDC logic

Before discussing the merge and transfer capabilities of SIO2 we need to know that one main function of SIO2 is the management of the DAQ timing. As already mentioned, SIO2 is synchronized to the central experiment clock. In fact SIO2 within the FPGA contains its own TDC ("time to digital converter" meaning a device latching a series of time counts when triggered by a series of events) as a logic building block. The internal time counter is synchronized in absolute time with the experiment time counter and obtains its clock from the central clock both running in locksteps representing nanoseconds since "the epoch"[10] [9].

This internal TDC features a series of registers and functions allowing simple timing operations: registers for start, delay, and increment values, repeat counts, time count comparison, etc.. Altogether these elements form a programmable timing engine which is configured by software commands from the host. Once armed, it operates independently and deterministically as the driving mechanism behind the whole DAQ and data transfer activities of the Pipe2/SIO2 system. It allows to define arbitrary trigger chains starting automatically from a command, a preset clock count, an internal start condition, or an external event, producing a certain timing pattern, terminating when reaching the preprogrammed end. These trigger programs may contain single, repeated, nested or chained sequences to implement the typically demanded pulse trains for triggered DAQ system.

The TDC timing engine thus produces the pacing for the whole DAQ operation consisting of taking a time stamp, initiating data capture in the periphery, merging time and data, and sending the result to the host. It's the "heart beat" of the SIO2's DAQ cycles.

Having integrated the DAQ time engine into the data transport device allows the straight integration between measured time and measured data at the source: the SIO device.

2.4. Integrating time and data – latency considerations

Figure 4 illustrates the internal operation of the SIO2 FPGA to achieve an "unsolvable" bond between time and data. Simultaneous to triggering a data conversion in the periphery SIO2 latches the 8 byte clock count from the central experiment clock into its internal timestamp FIFO. As the data conversion also includes the immediate upload of all samples for the triggered time step into the respective link FIFO's, one data sample acquisition cycle ends having the timestamp and all samples belonging to it in FIFO's in the FPGA. Under control of the merge and transfer logic the timestamp and all corresponding samples are combined and transferred into the output FIFO as a new data entity which we call "time-frame". So for each trigger finally one frame is created. As data rates on the input side as well as the limiting DMA transfer rates to the host are both well known, a design rule for a diagnostic is that the input rate must nor exceed the possible DMA rate. However, if this is ensured with a reason-able safety margin, it is also ensured that time-frames can be forwarded without congestion.

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10) the "epoch" here refers to the usual origin of time in POSIX compatible computer systems. See
     https://en.wikipedia.org/wiki/Epoch_(computing) for a detailed explanation of the meaning. The 64-bit
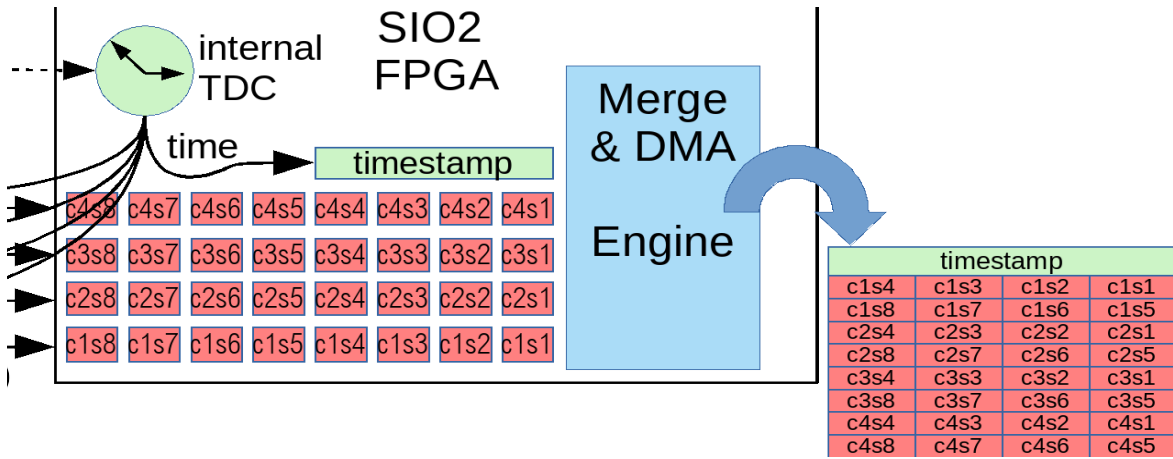   unsigned integer clock count used in TDC and SIO refers to the same origin but represents nanoseconds.

Figure 4: Detailed view of the SIO2 time and data merge and the subsequent transfer of a "time-frame" (a data block containing a timestamp and all samples belonging to that time - also called "SIO-frame") via DMA into the host. The timestamp data word is 8 byte wide while the samples are two byte wide. (Each sample in this figure is marked by its crate and sample index number.)

So finally frames will arrive in host memory with a minimum possible delay. So host applications working on this stream of time-frames will not be hindered by delayed data. This is a prerequisite to shape its own time behaviour to keep as close as possible in touch with real-time.

Example: A 1 MHz trigger rate in a 64 channel system would generate 1000 time-frames of 136 bytes in a millisecond. This yielding 136 kB per millisecond or 136 MB per second is easily transferred through Pipe2 backplanes, SIO2 FPGA and PCIe DMA into the host memory as a sustained data stream. However, the total delay of a measured quantity from the analogue input until arrival of data in host memory is not only depending on the sampling rate but also on the number of intermediate storage steps on the way from the ADC into host memory. Each step typically needs the time of a sampling cycle yielding a cumulated latency of all involved pipelines as ({# ADC pipeline steps} +{3 Pipe2/SIO2 steps}) / {sampling rate $[s^{-1}]$} = {latency [s]}

In fact the Pipe2/SIO2 system was successfully tested up to a sustained data rate of 200 MB/s between Pipe2 crates and SIO2 card using 4 crates delivering 50 MB/s each. The sustained data rate from the SIO2 to the host computer was benchmarked with 480 MB/s leaving headroom for future enhancements of the Pipe2 backplanes. Taking into account a factor of 3.5 between the given example and the tested maximum sampling rate the single frame transfer latency can become up to 3.5 times better. However, considering sources of analogue time delays for a signal like fibre, sensor, cable, and filter transit times and taking further digital delays like interrupt response times and sample averaging time windows into account, the latency caused by the Pipe2/SIO2 DAQ system is considered to be in the same order of magnitude as these effects or better. It was the goal to provide a DAQ system with a latency which can be neglected in most real-time diagnostics.

Regardless of latency considerations timestamps are always correct. Due to the directly embedded TDC which is in fact initiating the DAQ process the exact timestamp of the analogue to digital conversion is measured with an accuracy of 20 ns.

2.5. New SIO2 features for special requirements

As already described, the interface between DAQ modules and the Pipe2 backplane is as simple as possible. Nevertheless, the functionality of modules may be highly specialized and sophisticated.

The basic rules are:
- data acquisition uses a 16 bit parallel upstream shift register concept
- configuring modules occurs via an SPI downlink connection
- data acquisition and configuration are two separate operation modes
- modules operate in cadence with a timing determined by the upstream SIO2 card

When renewal of diagnostics such as Thomson-Scattering, Microwave-Reflectometry or event recording were considered, an extension of capabilities into the GHz sampling range and a more flexible timing for the Pipe2/SIO2 system was demanded. In particular this included the requirement of handling external event oriented triggering including timestamps. An additional constraint was to implement any extensions in firmware or as add-ons without modifying existing hardware.

As an implementation detail coming with high sampling rates in the order of $1 - 10$ MHz the merge and transfer engine was made programmable to allow flexible creation of time-frames. By providing an appropriate transfer program it is now possible to omit a configurable number of timestamps. This means all samples belonging to a configured time interval are packed behind the leading first timestamp into one time-frame. This reduces the overhead for recording time accordingly. However, in this mode sample triggers are still synchronously derived from the central experiment clock.

Going to even higher sampling rates up to the GHz range, the use of a timebase driven by the upstream SIO2 device has to be replaced by free running internal high speed clocks in the ADC modules themselves. In this case the modules typically feature their own output buffers into which a continuous stream of samples is directed. With this kind of periphery the SIO2 just periodically sends data requests to empty the periphery buffers. This happens in the already described manner under control of the internal TDC running a time pattern adapted to the external sampling rate and buffer size. Also here the clock ticks are generating periodic timestamps and thus triggering periodic SIO2 data requests. The Pipe2 periphery answers these requests by sending the last filled buffers.

According to this description and further requirements following capabilities have been added to the Pipe2/SIO2 system:
- SIO2 provides an extended data merge & transfer program configuration to combine data from multiple digitizing clock steps into one time-frame (also called "SIO-frame") carrying only the time of the first step as timestamp.
- SIO2 has been extended to provide a trigger input and output feature. A breakout card connecting to an already existing test socket on the main card provides six event input and two trigger output sockets. On detection of an external event SIO2 TDC latches a timestamp and executes the corresponding merge and transfer cycle. (One event creates one time-frame being transferred to the host with minimum latency.)
- To distinguish between the six different external events the TDC engine was modified

to store together with a timestamp a so called event tag encoding which input socket was triggered. This tag can be merged with timestamp and data and transferred to the host within time-frames.

- Interpreting the event tag the SIO2 transfer program may run into different branches to act for different events accordingly.
- Events (consisting of time stamp and tag) can be queued in a FIFO in the SIO2 logic to be responded on by the transfer engine deferred. This requires a corresponding multistage FIFO buffer in the ADC modules for intermediate buffering of samples belonging to each event until the deferred transfer is executed. This mode implies an increased latency for events happening shortly (meaning in the sub-μs time range) after each other.

These extensions to the Pipe2/SIO2 basis were mostly firmware and software upgrades to the FPGAs and device drivers. While these features have been introduced to address the requirements of concrete DAQ projects, they in fact extend the standard for supported diagnostics at ASDEX Upgrade described earlier [7] into a wider range in time resolution and into the field of event driven DAQ.

3. New DAQ modules for special requirements

Having created these necessary prerequisites in the Pipe2/SIO2 software basis, the planned diagnostics require specialized analogue input channels and digital converters ending up in the design of new Pipe2 modules for the system.

3.1. A 1 GSPS Dual-Channel ADC-Module for recording short events up to 8 μs

Some diagnostics (e.g. Thomson-Scattering, see below) require multi-channel transient recorders with an extremely high time resolution covering only a few hundred to thousand points in time followed by a large time gap. Such short signals typically originate from light or particle detectors. Contrary to recording analogue signals over a long period sample-by-sample we would like to call this "event recording". Typically time and shape (pulseform and height) of an event is of interest.

As already pointed out the Pipe2/SIO2 system is designed to aggregate a high number of similar modules into one DAQ system and takes a timestamp for each trigger received. So when the requirement of event recording in a great number of channels was to be evaluated the design of an appropriate module was considered.

It was only a small development step to upgrade the "traditional" sample-by-sample acquisition operation of the usual Pipe2 modules into the desired "event recording" operation mode. A built-in fast buffer in these new modules allows the acquisition of short series of samples initiated by a trigger thrown by the event. While the modules store the event as a sequence of samples in a local buffer, the SIO2 is recording the time for the same trigger. Only after having finished the recording of an event, data transfer from the Pipe2 periphery to SIO2 begins and the SIO2 frame, containing time, event tag and all channels and samples of the whole event, is transferred to host memory. For events with a low repetition rate compared

to the desired sampling rate this will allow sustained event recording over the full duration of a plasma discharge and end up in an effective reduction of the overall acquired data amount.

Figure 5 gives a simplified time scheme of the implemented event recording mode including pre- and post-trigger samples and the subsequent data transfer. While the shown case implies
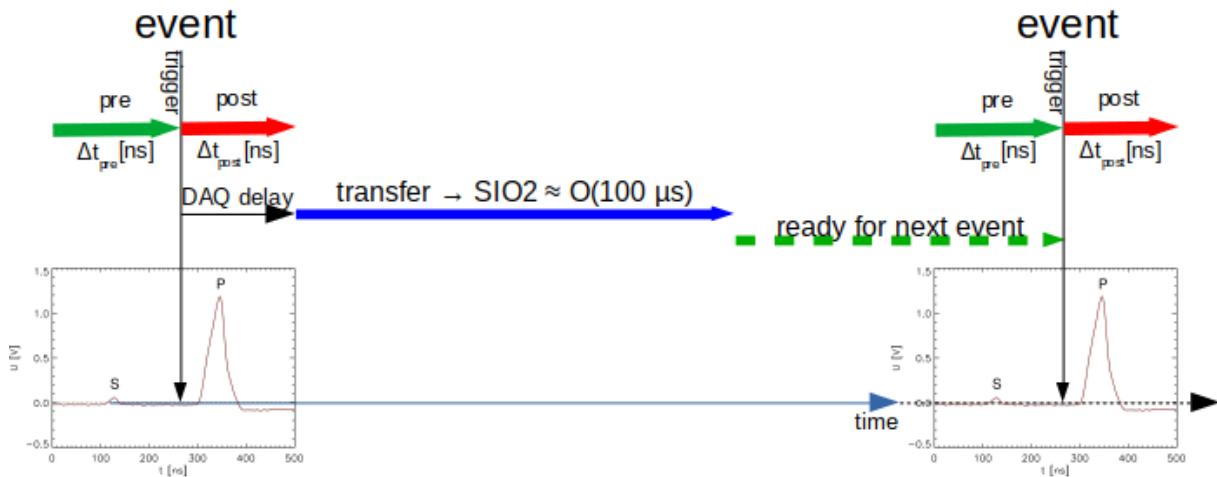

Figure 5: DAQ time behaviour of Pipe2 modules in "event recording" mode. The shown event example is taken from Thompson Scattering (see below Figure 10). More details in the text.

a required dead time between events during the data transfer from Pipe2 modules to the SIO2 card, the GSPS-ADC FPGA allows in fact recording of up to six events and an asynchronous upstream data transfer. (see below)

As core device for this ADC module the Analog Devices Dual Channel Converter AD9691 [10] was chosen. As shown in Figure 6 the design features two analogue inputs with separate signal conditioning chains (adaptation, offset correction, and amplification). The conditioned signals are captured by the AD9691channels A and B in parallel with a continuous sampling rate of 1 GSPS and an amplitude resolution of 14 bit. The digital output of the AD9691 circuit is realized as a serial JESD204B (subclass 1) interface [11] using 8 lanes and providing a total
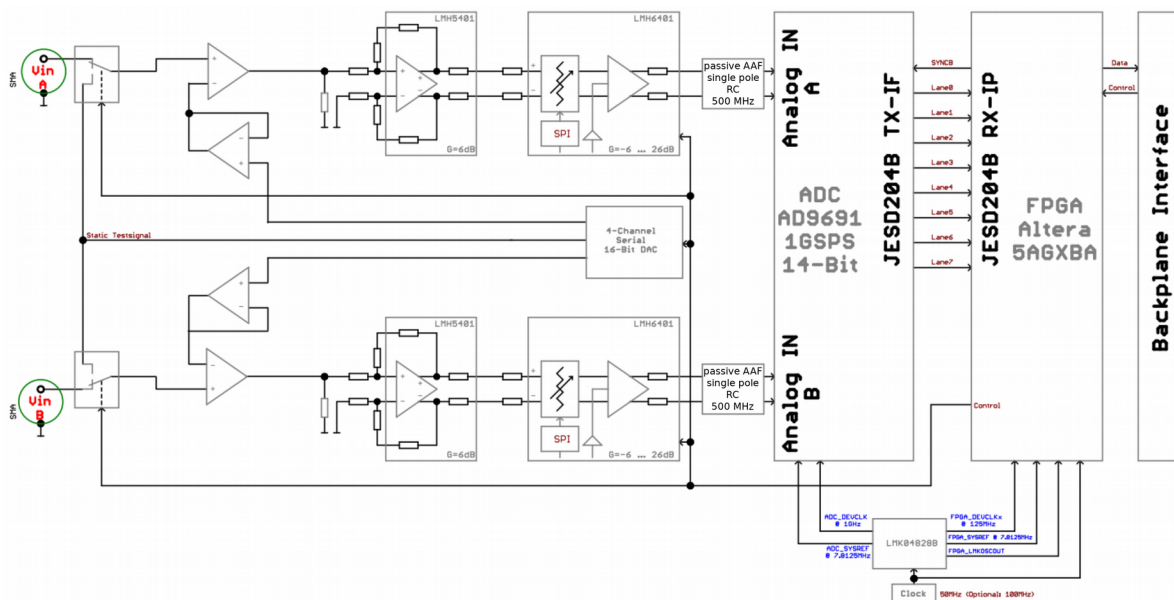

Figure 6: Block circuit of the 1 GSPS dual-channel Pipe2 ADC module

digital output bandwidth of 40 Gbps (5 Gbps per lane). This continuous distributed data stream is fed into a corresponding interface of an Altera ArriaV FPGA supporting the same JESD204B data communication protocol and providing the appropriate bandwidth. The continuously received data stream is transferred into a freely overflowing FIFO of a configurable depth. On external trigger – applying the configured pre- and post-trigger sample counts – the data flow into the FIFO is halted and the contents is frozen and held ready for transfer to the Pipe2 backplane. (As an anticipation to the requirements of the future plasma core Thomson Scattering diagnostic, in fact six of these FIFOs can be configured in the FPGA logic. This will allow to switch after a first scattering event immediately to up to five more events. So in total six scattering signals can be held in the ADC module for deferred transfer to the host computer.)

Configuring the size of the FIFO and the pre- and post-trigger counts, determines the event time window length and position in relation to the trigger time. In parallel the trigger must be sent to one of the event trigger inputs of the SIO2 card. On detection the SIO2 timing engine takes a time stamp and stores a corresponding event tag. The timing engine after a configurable delay starts the merge and transfer from all periphery modules to the host. Depending on the recorded event length the read-out of a single event lasts in the order of 100 µs. (A typical transfer speed of the Pipe2 backplane is 50 MByte/s or 25 samples/µs .) This also characterizes the latency for event data to be accessible by the host as well as the dead time between events[11,12].

3.2. Continuous signal recording with 20 MSPS

Contrary to the before described module e.g. Doppler Backscattering requires a continuous acquired signal with a sampling rate of 20 MHz which led to the development of a dual channel, 16 bit, 20 MSPS module. But due to the resulting high data rate an aggregation of multiple of these modules is not feasible. Instead it needs direct coupling to the Pipe2 controller and a SIO2 link to transport the resulting 80 MB/s. Featuring four Pipe2 links per SIO2 card four of those modules, totaling 8 channel, and delivering a data stream of 320 MB/s represents a reasonable dimension for a diagnostic. In fact the Doppler Backscattering diagnostic with a first exemplar of this module series went into operation. The full diagnostic consisting of 3 microwave Doppler interferometers will go into operation with the new campaign at ASDEX Upgrade end of 2019.

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11) In case of the DTS diagnostic the minimum time between two consecutive events is given as 50 ms by the maximum laser repetition rate of 20 Hz (see the details of DTS below).

12) The module design seems extendable by an implementation of multiple ring buffers for recording multiple fast following events.

4. New ASDEX Upgrade diagnostics

The above described developments have been carried out to answer particular requirements brought up by various ASDEX Upgrade diagnostics. In general the desire to answer physics questions demands new or extended measurement methods to get deeper insight into the underlying processes. In other cases the desire to get results in real-time or simply the need of refurbishing outdated hardware is the driving force. So this chapter will describe how the available building blocks fit together to form new diagnostics satisfying the particular demands. Table 3 gives an overview of recent Pipe2/SIO2 Linux based diagnostic projects.

name	channels	sampling rate	data rate	modules	SIO2 interfaces
continuously sampling diagnostics					
Soft-X-Ray (fast)	144	2 MHz	592 MB/s	72	3
Soft-X-Ray (slow)	96	800 kHz	160 MB/s	48	1
Mirnov Probes		1 MHz			2
Divertor X-UV	16	500 kHz	16 MB/s	8	1
Microwave-Reflectometry	7	20 MHz	336 MB/s	7	1
event driven diagnostics					
Divertor TS (1 laser)	108	1 GHz	5 MB/s	64	2
Core TS (6 laser)	116	1 GHz	30 MB/s	68	2

Table 3: Recently provisioned (green background) and in near future planned (pale orange) Pipe2/SIO2 Linux diagnostics. All these diagnostics are real-time capable. But at the moment only the Divertor X-UV is available for control purposes. (Mirnov and Soft-X-Ray would use this as well and others are to come.)

The following chapters will present only two representative configurations of the listed new diagnostics.

4.1. Enabling real-time X-Point detection

To determine and possibly control the X-point position of the separatrix in ASDEX Upgrade discharges in real-time, it was required to split-off one X-UV diode array from the existing X-UV measurement system and to set it up for real-time DAQ, analysis and communication with the DCS. Figure 7 shows the principle observation lines of the chosen X-UV diode array.
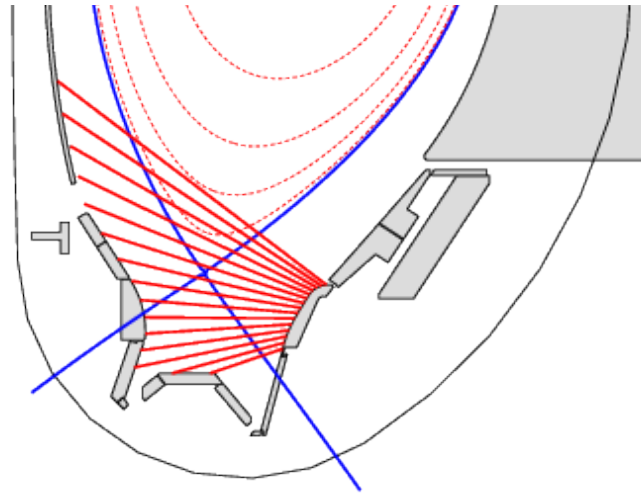
Being derived from an existing diagnostic it was no complete redesign but just the provisioning of an extra Pipe2 crate and backplane to comprise the ADC channels in question. As host computer a dual socket Fujitsu TX2550 M4 19" server system was chosen. It was set-up with a

Figure 7: Lines of sight of the real-time 16-channel X-UV emission observation in the ASDEX Upgrade Divertor. (The underlying separatrix and flux surface geometry represents a typical field configuration.)

CentOS Linux including real-time capabilities. The selected dual socket motherboard allows to assign real-time tasks and activities to the second socket CPU shielding this from the operating system activities. As well the Pipe2/SIO2 DAQ interface is clearly allocated to the second CPU minimizing CPU to CPU traffic during the real-time DAQ and data analysis phase. Bringing the DCS system, which is from its beginning already Linux based, and the SIO2/Pipe2 DAQ together on a common Linux real-time platform accomplishes a milestone in the intended full integration between plasma control and diagnostic at ASDEX Upgrade.[12]

First measurements with this real-time enabled diagnostic clearly show the movement of an X-UV radiation maximum through the observed region during the plasma discharge (see Figure 8, image provided by Matthias Bernert, ASDEX Upgrade team). A journal letter about the physics findings and control implications is about to be published [13].
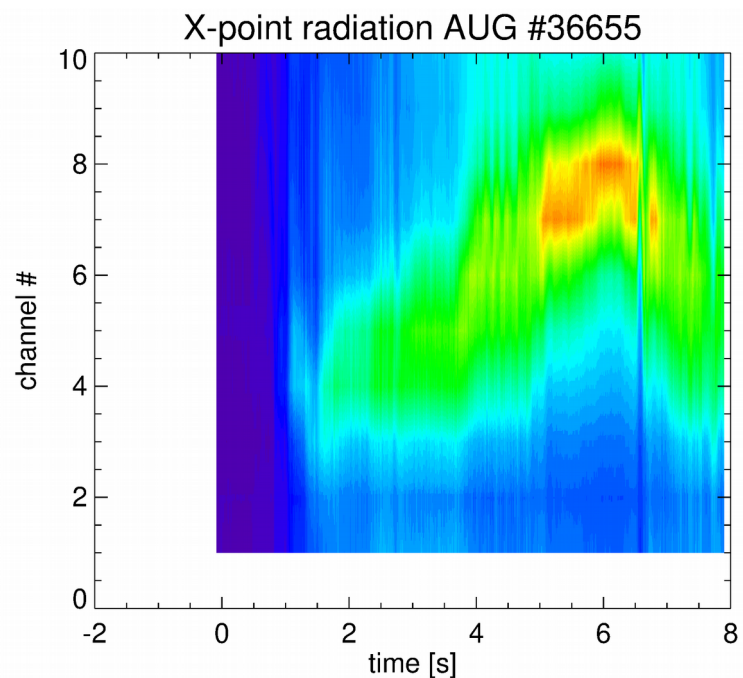

Figure 8: X-UV emission radiation measured over ten lines of sight in the ASDEX Upgrade divertor (image provided by M. Bernert, ASDEX Upgrade team). It's clearly visible how the radiation is developing and moving over time.

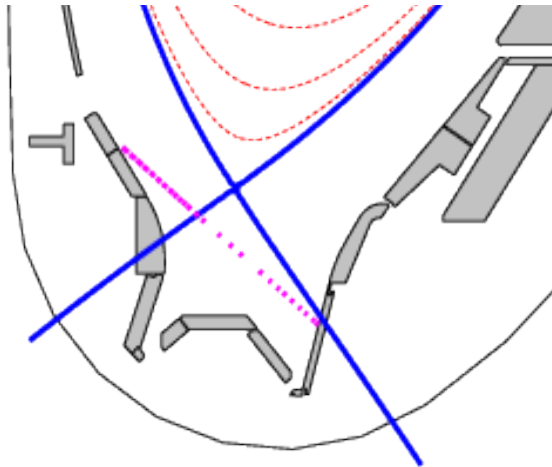## 4.2. Design and first results of Divertor Thomson-Scattering DAQ

Figure 9: Geometry of the Thomson Scattering laser in the ASDEX Upgrade Divertor region. The diagonal pointed line depict the observed scattering volumes of the diagnostics optic.(The presented flux lines just serve to illustrate a typical field equilibrium.)

Thomson-Scattering (TS) is a well known method to measure temperature and density in a fully ionized plasma. A short high intensity laser pulse is sent through the plasma and the light scattered by the free electrons is analysed with respect to intensity and Doppler-broadening of the spectrum.

The first DAQ system for a new TS diagnostic in the ASDEX Upgrade Divertor region is called "Divertor Thomson Scattering" (DTS). 26 observation points along the laser beam crossing the Divertor region are to be observed in 4 different spectral channels each. So in total 108 similar ADC channels (104 scattering + 4 monitor signals) with 1 GHz time and at least 10 bit effective resolution were requested.

The final diagnostic features 64 of the dual-channel GSPS ADC modules described above grouped in eight Pipe2 crates and driven by one Linux host comprising two SIO2 cards.

First measured signals of this diagnostic have been seen during calibration of the scattering channels. Figure 10 shows such a detector signal of a single channel. The time delay between S and P is caused by the path length difference. The amplitude relation between both in calibration measurements is used to calculate the calibration factor for each channel. In TS measurements during a real plasma discharge the calibration factor and the relation of these amplitudes finally yield the electron density at the observed volume.
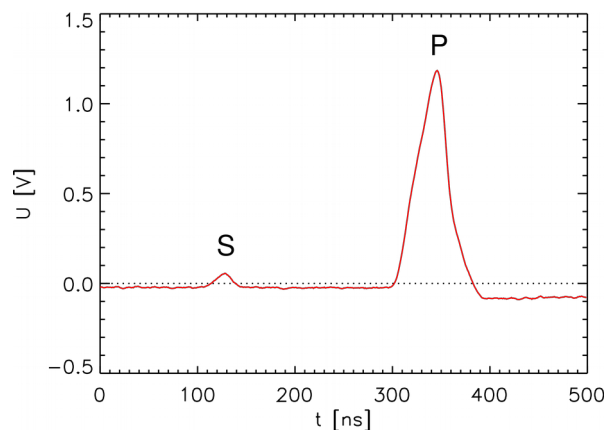

Figure 10: First measurements taken with the DTS diagnostic system. The curve shows the scattered light signal S and the laser pulse reference P in a single detector channel. (See further description in the text.)

5. Summary and outlook

Several feature extensions to the soft- and firmware and an additional breakout card for the Pipe2/SIO2 system enable the application of this system for a wider range of plasma diagnostics. Special attention has been laid on the low latency properties of the DAQ system and on the real-time capabilities of the data provisioning to other real-time processes in the same host computer system.

First installations of this kind of real-time diagnostics coupled with DCS application processes have demonstrated the fitness of the architecture and its implementation for the intended purpose.

Next steps will apply this system architecture to already planned diagnostic refurbishments partly replacing outdated hardware and partly with the intention to enable real-time experiment control on a broader range of diagnostics measurements and advanced algorithms.

6. Acknowledgement

References

1: K. Behler, H. Blank, H. Eixenberger, A. Lohs, K. Lüddecke, R. Merkel, G. Raupp, G. Schramm, W. Treutterer, M. Zilker, ASDEX Upgrade Team, Real-time diagnostics at ASDEX Upgrade - architecture and operation, 2008

2: W. Treutterer, R. Cole, K. Lüddecke, G. Neu, C. Rapson, G. Raupp, D. Zasche, T. Zehetbauer, ASDEX Upgrade Team, ASDEX Upgrade Discharge Control System—A real-time plasma control framework, 2014

3: B. Sieglin, W. Treutterer, L. Giannone, ASDEX Upgrade Team, DCS satellite: Enhanced plant system integration on ASDEX Upgrade, 2019

[4] F.R. Hertweck, J. Maier; Data structure for the description of tokamak diagnostics; Review of Scientific Instruments 57, 1986, https://doi.org/10.1063/1.1138801

5: P. Heimann, Proceedings of the Fourteenth Symposium on Fusion Technology, 1986

[6] K. Behler, H. Blank, A. Buhler, R. Drube, H. Friedrich, K. Förster, K. Hallatschek, P. Heimann, F. Hertweck, J. Maier, R. Merkel, M.-G. Pacco-Düchs, G. Raupp, H. Reuter, U. Schneider-Maxon, R. Tisma, M. Zilker, The Computer ScienceDivision, Garching Computer Centre, The ASDEX Upgrade Team; Review of the ASDEX Upgrade data acquisition environment - present operation and future requirements; Fusion Engineering and Design 43, 1999, https://doi.org/10.1016/S0920-3796(98)00392-5

[7] K. Behler, H. Blank, A. Buhler, R. Cole, R. Drube, K. Engelhardt, H. Eixenberger, N.K. Hicks, A. Lohs, K. Lüddecke, A. Mlynek, U. Mszanowski, R. Merkel, G. Neu, G. Raupp, M. Reich, W. Suttrop, W. Treutterer, M. Zilker, ASDEX Upgrade Team; Real-time standard diagnostic for ASDEX Upgrade; Fusion Engineering and Design 85, 2010, dx.doi.org/10.1016/j.fusengdes.2010.03.001

[8] K. Behler, H. Blank, H. Eixenberger, M. Fitzek, A. Lohs, K. Lüddecke, R. Merkel, ASDEX Upgrade Team; Deployment and future prospects of high performance diagnostics featuring serial I/O (SIO) data acquisition (DAQ) at ASDEX Upgrade; Fusion Engineering

and Design 87, 2012, https://doi.org/10.1016/j.fusengdes.2012.09.020

9: Gerhard Raupp, R. Cole, K. Behler, M. Fitzek, P. Heimann, A. Lohs, K. Lüddecke, G. Neu, J. Schacht, W. Treutterer, D. Zasche, Th. Zehetbauer, M.Zilker, ASDEX Upgrade Team, A "Universal Time" system for ASDEX upgrade, 2003

10: Analog Devices, Data Sheet 14-Bit, 1.25 GSPS JESD204B, Dual Analog-to-Digital Converter AD9691, 2015

11: Analog Devices, JESD204 Interface Framework, 2019

11: B. Sieglin, W. Treutterer, L. Giannone, the ASDEX Upgrade Team, DCS satellite: Enhanced plant system integration on ASDEX Upgrade, 2019

12: M. Bernert, F. Janky, B. Sieglin, A. Kallenbach, B. Lipschultz, F. Reimold, M. Wischmeier, M. Cavedon, P. David, M.G. Dunne, O. Kudlacek, R.M. McDermott, W. Treutterer, E. Wolfrum, D. Brida, O. Février, S. Henderson, M. Komm, the EUROfusion MST1 team, the ASDEX Upgrade Team, X-Point radiation and its control at the tokamak ASDEX Upgrade, 2019