Development of an active overvoltage protection for the new ASDEX Upgrade divertor coils

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There is proposed a new upper divertor for the ASDEX Upgrade (AUG) tokamak experiment [1]. It is planned to be equipped with internal coils for investigation of advanced magnetic configurations like e.g. „snowflake“ [2]. Due to the close vicinity of the coils to the plasma, high induced and very stiff voltages are expected during disruption events, as shown in [3],[4]. This voltage is a high risk for either damaging the connected power supplies and/or for turning into high currents causing damage to the tokamak by Lorentz forces. The proposed device named “ripping crowbar” detects and overtakes the full high voltage of up to 5 kV during a plasma disruption at full load current of up to 3 kA to protect the connected power supply which can deal with voltage not higher than 340 V absolute value. The concept will be given and discussed. Experiments were started at much lower current and voltage by use of commercially available hardware. This is a starting point to enhance the working regime in a time-saving way, because there exist no commercially available solution for the target values. The only known field with comparable power stage solutions can be found in the field of High Voltage Direct Current (HVDC) circuit breakers [5]. The final solution should be scalable in voltage, current and power to adapt it to other applications in and outside the field of fusion technology. Part of the development are the Insulated Gate Bipolar Transistor (IGBT) based powerstage, the drivers, the measurement unit to detect disruptions and the triggering unit. At the end, most important will be reliability of this safety relevant device to protect multi-million investments into power supply and new divertor.

Keywords: divertor coils, snowflake, FEM, disruptions, magnetic forces, power supply, crowbar

1 Introduction

The AUG new upper divertor, part of the Eurofusion Plasma Exhaust strategy (PEX) and currently in the fabrication phase, creates local flux regions by help of a magnetic dipole situated as close as possible behind the outer target plates [3],[4]. During normal operation, the dipole creates mainly torque (overtaken by a stiff ring-shaped support structure) but only small forces. In principal, the coils can be operated in counter-serial connection by help of a single power supply. In case of a plasma disruption, very high voltages are induced, but they almost compensate each other. The power supply can continue in normal operation mode [3].

For scientific reasons, small imbalances (< 20%) of the dipole currents are a mandatory requirement. This means, a second power supply has to provide the difference current to a single coil. This power supply needs protection from the high disruption voltage (approx. 5 kV while 340 V normal operation voltage). The concept for coil and power supply protection consists out of several elements [3]. One of them is the "ripping crowbar" which overtakes both, full current and full disruption voltage (up to 15 MW), for the period time of a disruption (up to 20ms). The concept of this active overvoltage protection system is presented, here.

2 Supply and Ripping Crowbar Concept

The electric overview circuit is shown in Fig. 1. The bipolar(!) turn-off capability is based on counter-serial operated IGBTs, the energy is absorbed by varistors which is a typical approach for DC breakers [5]. A detection unit is measuring the difference current with shortest possible delay. It activates the power stage via a trigger unit at an overcurrent event. The power stage is operated by a single driver unit which provides sufficient isolation between driver and power stage electric potentials. IGBTs and varistors need active (probably water-based) cooling due to the permanent conducting losses up to 15 kW per IGBT. Last safety is provided by so called “pyro fuses”, able to suppress the maximum inductive current and overtake the related energy within milliseconds for a single event [6].

The topology of the powerstage is planned to be scalable in voltage, current and energy. The voltage scalability is realized by taking advantage of the so called "transistor cascade" topology.

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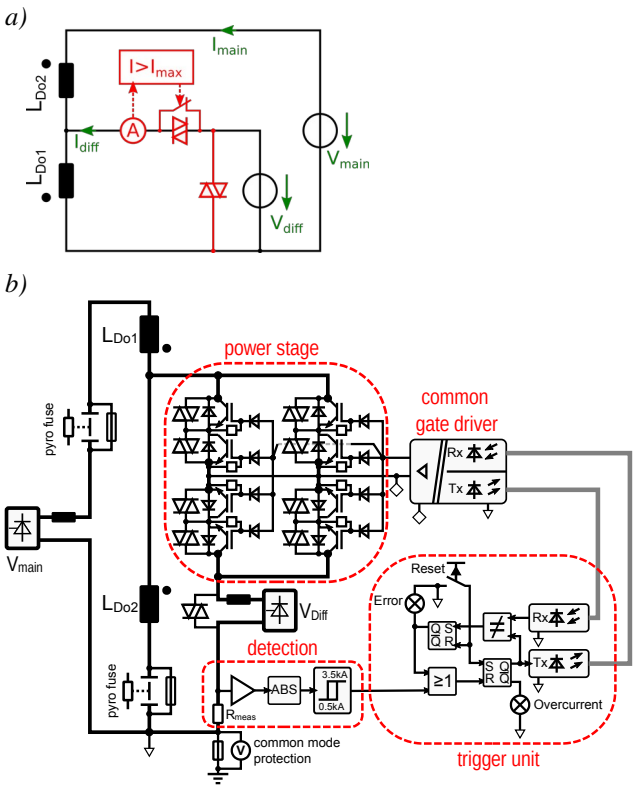

Fig. 1: (a) Concept [3] and (b) overview of the power supply for the divertor coils L_{Do1}, L_{Do2} with highlighted systems of the ripping crowbar. The bipolar powerstage consists out of four unipolar double-stage transistor cascades connected in combined serial and parallel operation to double current, double voltage and bipolar switching capability.

The original unipolar transistor cascade (Fig. 2) is operated by a single gate unit (this is same for the bipolar version as shown in Fig. 1). The isolation is overtaken by diodes (here: 3 diodes for 3 transistor stages, the diode of the lowest stage could be removed). Turning-on the cascade (Fig. 1a) is an asynchronous, step-wise process starting with the lowest stage, where the emitter potential is the same like the gate driver reference voltage.

If the lowest stage is fully on ($V_{CEon} \approx 0$), the emitter potential of the next stage also becomes almost equal to the gate driver reference. Diode D2 starts conducting and the 2nd gate charges by help of the gate driver. This continues until the whole cascade is turned on. Each stage is voltage protected by varistors. Of course, they cause losses during this asynchronous process, but the turn-on speed can be influenced by the maximum diode forward current capability of the diodes and the stiffness of the driver output. Here, the turn-on process can be done before operation of the divertor coils, thus it is uncritical. The turn-off process of the cascade (Fig. 1b) is much more challenging, even that it is a synchronous process. Here, it is typically triggered at full operating load current. The speed can not be influenced by the gate driver, which simply turns off the output (0V) and the gate discharging is done in a passive way by gate resistors. This process has to be slow, because the gate resistors can not be of low impedance, otherwise turning-on becomes impossible (or very hard for the driver and diodes). For the application shown here, the triggering of the cascade would be strongly delayed, slow (much slower than the period time of a disruption event < 20ms) and very lossy (several MW during that period). In total this is not acceptable. Of course, the use of multiple, highly isolated gate drivers would be an option, but simplicity and scalability are high values for this safety-relevant device.

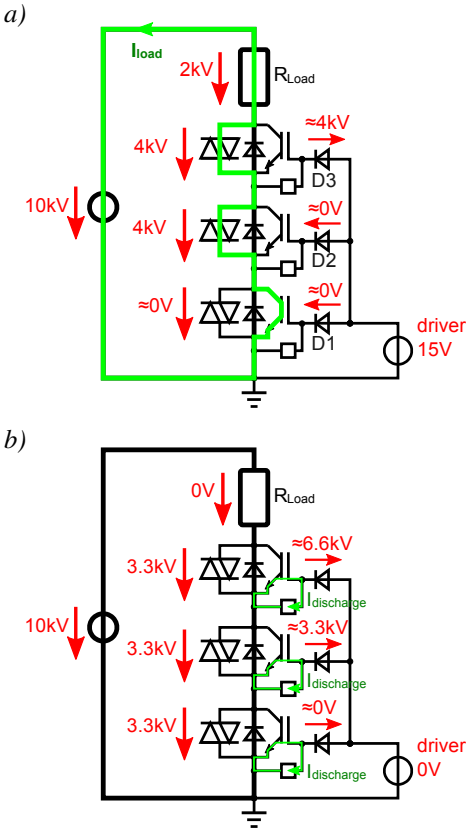

Fig. 2: The original unipolar transistor cascade consisting out of 3 stages, (a) while step-wise turning on (here: first stage on, 2nd+3rd still off), (b) while synchronous passive turn-off process via gate resistances.

An improvement of the cascade is proposed and shown in Fig. 3. The turn-off process now is supported by the small-signal PNP transistors which amplify the gate discharge currents. For a single stage, the turn-on process is shown in Fig. 4a. Here, the gate is charged with I_{gate} which is almost equal to I_{driver} if R_{OFF} is chosen to be of high-impedance. The PNP transistor is not active, because the basis voltage is slightly positive by the D_{ON} diode conducting the gate current in forward direction.

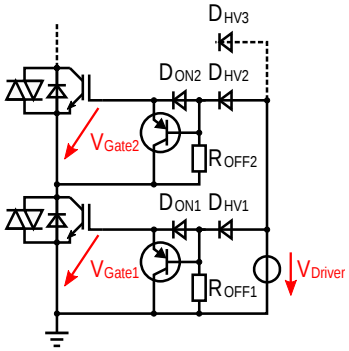

Fig. 3: Proposed cascade with improved turn-off performance.

This is different for the turn-off process while the driver voltage is 0V and the gate at a higher level V_{gate} (typ. up to 15 V), as shown in Fig. 4b. Here, both diodes are in blocking direction and the PNP basis conducts the basis current I_b, which is limited by R_{OFF}. Due to the current amplification β of the transistor, the collector current becomes $\beta \cdot I_b$. Thus, the gate discharge current is amplified to

$$I_{gate} = I_b \cdot (\beta + 1)$$

This is equal to passive discharging by help of a resistor of value $R_{OFF}/(\beta+1)$. Of course, this is all simplified with the assumption of neglectable diode forward voltage drop and transitor basis voltage. Also over-/undervoltage protection of the circuit by additional zener diodes (and small filter capacities) is highly recommended. The driver output voltage also needs to compensate the IGBT V_{CEon} and diode forward voltage drop, which increases in total with the number of serial stages.

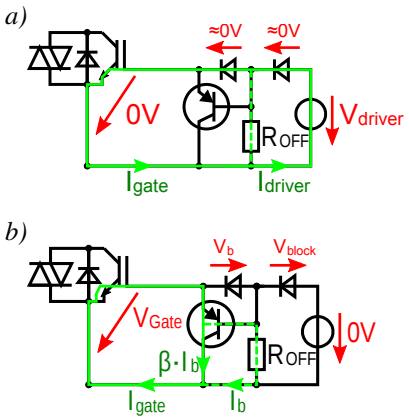

Fig. 4: Voltages and currents of a single stage while (a) turn-on and (b) turn-off process

3 The Power Stage

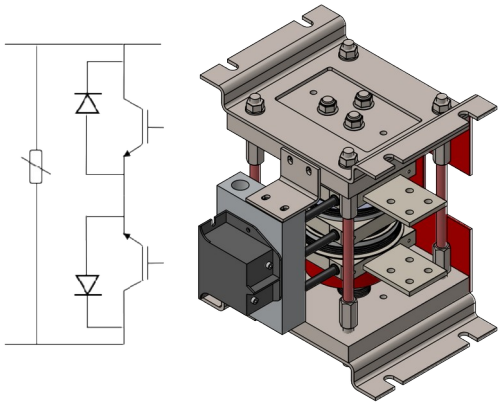

Fig. 5: Schematic (left) and CAD drawing (right) of the powerstage (special design by IXYS UK). For reduced scale experiments, a separately packaged varistor is sufficient (black component attached to the gray water distributor box)

Two stacks with four counter-serial connected 130 mm press pack IGBTs and water cooling are already prepared for the experiments (see Fig. 5). This should be sufficient to demonstrate parallel and serial scalability. The varistors for energy absorbtion and voltage balancing will be connected by extern cabling, for the first. The IGBTs are rated for 1.3kA, 3.6kV (DC) and 6kV (pulse). Water cooling is provided by a pump stand, circulating de-ionized water through a heat exchanger, able to cool-down up to 30 kW of heating power.

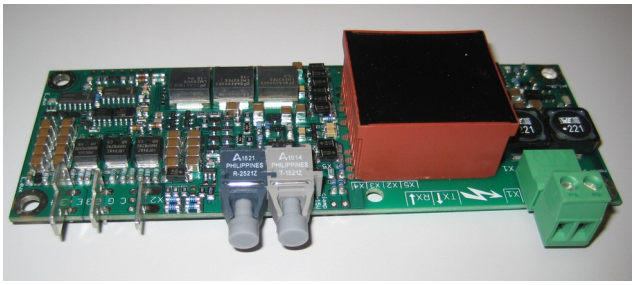

Fig. 6: Gate driver unit by WESCODE (special design)

A gate driver unit for first experiments is available (Fig. 6) and isolates up to 5 kV. For flexible serial scalability of the power stage, a new unit needs to be designed with even higher isolation voltage (min. 5 kV per stage). The modification should concern only the input transformer for power supply. The trigger and status signals are already transferred via waveguide. Driver power should not be relevant. The gates are charged before high current operation (which can be slow) and discharged independently from the driver as explained above.

4 The Varistors

The varistor is a critical component in the planned arrangement and it will be used in an untypical way. Typically, it is used for flash protection, this means very few and rare events. Plasma disruptions at ASDEX Upgrade can happen more than 10 times per day. The heat capacity of the shown disc (Fig. 7) is theoretically sufficient to absorb up to 27 kJ. The ripping crowbar has to absorb up to 100 kJ [3], this means 4 discs in parallel or serial connection could be sufficient. The breakdown voltage is approx. 1.7 kV at given current. Serial connection for higher voltage and energy requirements is possible and will be used.

Fig. 7: Hydraulic press and varistor disc

By help of a hydraulic press, we try to find out if the very high pressure in an IGBT stack (>10 tons) can be acceptable for the varistor discs. This information is not available even from manufacturer side because they are typically packaged in epoxy isolation at very low pressure for uncooled operation. The first results are promising.

The integration into the IGBT stack would be optimal in terms of (water) cooling and (low) stray inductance.

5 Outlook

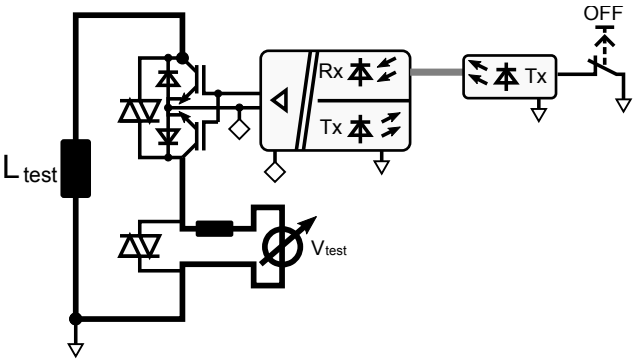

Fig. 8: Planned experimental setup to test and optimize the power stage

Before realizing the ripping crowbar, careful and stepwise testing of the components under controlled conditions is mandatory. The schematic of the planned, first experimental setup is shown in Fig. 8. A varistor-protected thyristor converter V_{test} generates and injects a defined DC current into a dominant-inductive test load which has to be disconnected by the IGBT powerstage. For the first, it will be as simple as possible, consisting of a bipolar IGBT stack as shown in Fig. 5 protected by an external wire-connected varistor. The stored energy in the circuit can be modified by variation of the load inductance and/or the current provided by V_{test}. The overvoltage seen by the powerstage and varistor will always be the maximum possible, this means the breakdown voltage of the varistor. This is due to the inductive behaviour of the load which avoids rapid current change due to stored energy related with it ($W_{L\_test} \sim I_{load}^2$). In this first phase, stray inductances can be measured and optimized and the cooling efficiency estimated. Unavoidable overvoltage peaks seen from the IGBT stack need to be measured and taken into account and/or filtered by snubber circuits. Also the integration of the varistor discs into the IGBT stack will be tested.

In the next phase, the cascade will be tested, even if it should not be required for the needs of the current project. The available IGBT maximum V_{CE} voltage could be sufficient for the AUG divertor application to limit the current rise enough for protection against destructive Lorentz forces during the short period of a plasma disruption. Anyhow, the scalability is important to turn the ripping crowbar into a mult-purpose tool for tokamak (in-vessel) coils. This could ease the integration of coils in many situations.

After this, parallel operation will be tested as well. This is expected to be uncomplicated due to negative temperature coefficient of the IGBTs.

Finally, the detection and trigger unit as well as the enhancement of the gate driver isolation has to be done. Of special interest are

- High bandwidth, low noise and offset-free measurement of the load current. Preferred is a robust shunt-based method.
- Sufficient low delay but high robustness of the trigger unit without any tendency for EMI and oscillations of the overall system.
- A mechanical assembly of all components making it easy to scale-up, keeping stray inductances small/predictable and cooling efficient and balanced.
- Integration of the ripping crowbar into the existing thyristor converter foreseen for the divertor coils operation. To compensate unavoidable delays, maybe a small serial connected inductivity is necessary to integrate into the high-current load circuit.

The test and development strategy is summarized by the list as follows:

1. Single IGBT stack with external varistor has to break an inductive current of stepwise increased energy content.
2. A water cooled varistor will be used for IGBT protection, integrated into the (already water cooled) IGBT stack as preferred solution. Aging of the varistor for a high number of cycles has to be estimated (AUG performs up to 10 plasma disruptions per day, 1500 plasma shots per year)
3. The cascade approach will be tested by serial connection of multiple stacks. A solution for a high voltage isolated gate driver unit (>10kV) needs to be found.
4. Parallel operation of multiple cascades for higher current (> 2kA) will be tested.
5. A fast trigger unit for safe, reliable and autonomous operation needs to be developed, including low delay overcurrent detection (< 500µs) and EMI robustness.

6. Packaging and adaption to AUG power supplies and magnetic coil system. Integration into AUG control system.

6 Summary

The concept and planned technical realization of the ripping crowbar is described in detail. The scalability in voltage and current is identified as mandatory requirement for flexible adaption into fusion-related applications. The well known concept of the transistor cascade was taken and significantly improved to simplify the arrangement and increase reliability of this safety relevant device. The power stage and driver units for first experiments were shown and explained. Commercial varistors were tested against high mechanical loads to finally integrate them into the water cooled IGBT stack. Varistors are used in an untypical way connected with the requirement of active cooling. Finally, the route consisting of many experimental steps for realization is given.

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