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Observation of Optically Addressable Nonvolatile Memory in VO_2 at Room Temperature

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Vanadium dioxide (VO_2) is a phase change material that can reversibly change between high and low resistivity states through electronic and structural phase transitions. Thus far, VO_2 memory devices have essentially been volatile at room temperature, and nonvolatile memory has required non-ambient surroundings (e.g., elevated temperatures, electrolytes) and long write times. For the first time, here, the authors report the observation of optically addressable nonvolatile memory in VO_2 at room temperature with a readout by voltage oscillations. The read and write times have to be kept shorter than about 150 µs. The writing of the memory and onset of the voltage oscillations have a minimum optical power threshold. Although the physical mechanisms underlying this memory effect require further investigations, this discovery illustrates the potential of VO_2 for new computing devices and architectures, such as artificial neurons and oscillatory neural networks.

1. Introduction

Phase-change materials (PCMs) are important candidates for next generation computing devices and systems, including artificial neurons and neuromorphic computing that aim to improve power consumption and speed in data transfer.[1–10] A PCM gaining much interest for such applications is the transition metal oxide, vanadium dioxide (VO_2), which can reversibly change between its insulator and metal states by thermal,[11] electrical,[12,13] optical,[14] or mechanical stimuli[15] or by ionic liquid gating.[16–18] The phase transition has an hysteresis that is utilized for memory[15–17,19–21] and the negative differential resistance (NDR) regime of the VO_2 leads to voltage or current oscillations.[12,22–24]

Thus far, the VO_2 insulator-metal transition (IMT) due to a structural phase transition (SPT) has been volatile at room temperature, making a VO_2 memory cell power-inefficient. Nonvolatile phase-change has been observed in VO_2 on a piezoelectric substrate, but the nonvolatility is due to remnant strains in the piezoelectric material rather than the VO_2 itself.[15] Tuning the oxygen vacancy concentration using a gated electrolyte[16] or hydrogenation[17] of VO_2 can lead to nonvolatile, reversible phase transitions but, to date, it is very slow (requiring minutes and up to hours) as summarized in Table S1, Supporting Information. Other observations of nonvolatile VO_2 memories required an external bias, in the form of a raised temperature or applied voltage, to maintain their memory states.[19–21] Here, we report the observation of nonvolatile VO_2 memory at room temperature with sub-millisecond writing and reading times. The nonvolatile memory state is accessed within the narrow hysteresis of the first major transition in current-biased VO_2; it persists in the ambient environment without the application of an external bias or excitation. Interestingly, compared to typical nonvolatile memory, where the readout is measured by two or more distinct physical states, our written memory is read out as voltage oscillations between the insulator and metal states.

2. Results

Before discussing the details of the experiments, we first provide an overview of the device operation and the observed phenomenon. The device consisted of two electrical terminals patterned on an etched VO_2 microwire (**Figure 1**a). A typical VO_2 microwire exhibits a voltage-current (VI) relation as shown in Figure 1d, which consists of two major transitions at I_{T1} and I_{T2}, between which is a NDR region. It is often believed that I_{T1} corresponds to a mostly carrier-induced onset of the IMT, whereas I_{T2} corresponds to a largely thermally-driven Peierls SPT transition.[13,25,26] Smaller step transitions can also often be observed at currents near I_{T2} in thicker (~30 nm or more) films of VO_2 on TiO_2 due to nanoscale line cracks,[27] but they do not

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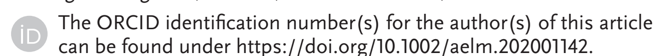
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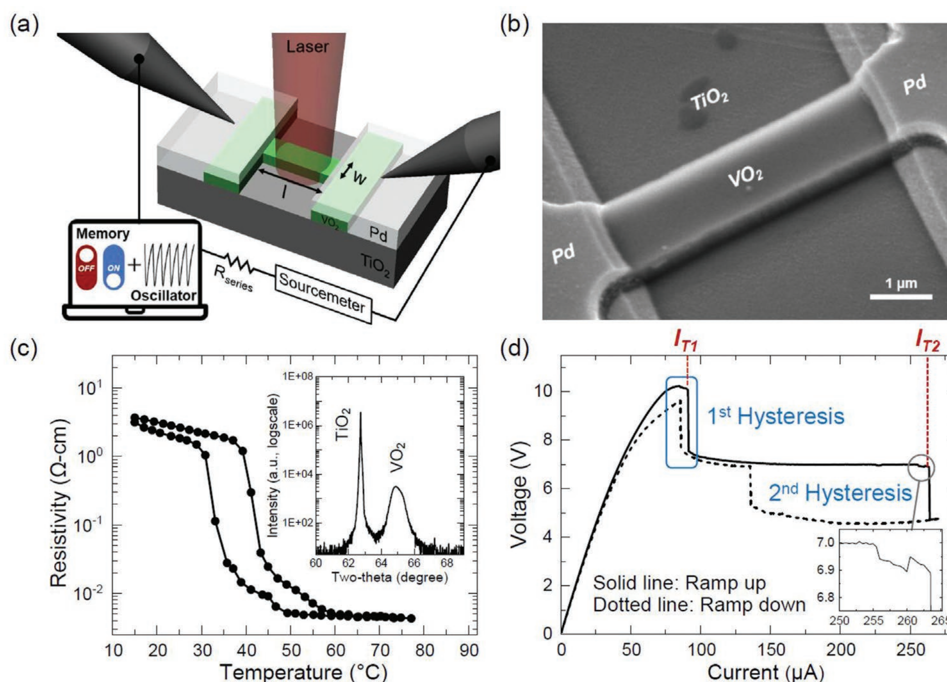

Figure 1. a) 3D schematic of the device and experimental setup. b) A scanning electron micrograph of a representative VO_2 microwire with palladium (Pd) contacts. c) Measured resistance of a VO_2 device as a function of stage temperature. Inset, X-ray diffraction (XRD) spectrum of a VO_2 film on a TiO_2 (001) substrate. d) Typical example of *VI* measurement at room temperature, showing two abrupt transitions. The first and second major step of phase transitions corresponds to a largely carrier-induced transition and largely thermally-driven full SPT, respectively. The phase transition currents, I_{T1} and I_{T2}, are labelled. Inset, small transition steps are observed near I_{T2}.

occur near the observed memory phenomenon. To prepare the device for memory writing, it was first held at a constant current bias in the insulating-monoclinic phase (M_1-phase) near I_{T1}. To write the memory, an excitation, which was a weak optical pulse at a wavelength of 1550 nm in our experiment, was illuminated at normal incident. The excitation generated excess carriers to drive the VO_2 into what we refer in this manuscript as the "oscillating state" (O-state). Generally, the O-state persists between I_{T1} and I_{T2} as indicated in Figure 1d. In the O-state, the device exhibits NDR (see Figure 1d) and the coexistence of the both M_1-phase and metallic-rutile phase (R-phase) induces voltage oscillations, due to the periodic discharging and charging of the VO_2 capacitance across its IMT.[12,24] After the writing with an optical pulse, the current bias near I_{T1} was turned off within a fall-time of <150 µs. When the memory-writing bias current was applied again with a sufficiently short rise-time of <180 µs, contrary to the expectation of the VO_2 returning to the M_1-phase, the device was consistently found in the O-state characterized by persistent voltage oscillations. The device could be reset, that is, the memory could be erased, by applying a bias current less than the hysteresis loop of the first major transition.

2.1. Experimental Setup and Material Properties

Next, we discuss the details of the experimental investigation. Figure 1a shows the schematic of the device and the experimental setup (see Figure S1, Supporting Information, for more details). The microwire VO_2 device was defined using conventional microfabrication processes in a 360 nm thick VO_2 film on a titanium dioxide (TiO_2 (001)) substrate formed by pulsed laser deposition (PLD). Figure 1b shows a scanning electron micrograph (SEM) of a device. The VO_2 film on TiO_2 (001) substrate was strained along the *c*-axis by −1.2% due to the lattice mismatch,[16] which resulted in a phase transition temperature (T_C) of ≈41.5 °C (314.65 K) as shown in Figure 1c. Across the phase transition, the VO_2 resistivity changed by about three orders of magnitude. Room-temperature X-ray diffraction (XRD) measurement (inset of Figure 1c) confirms the composition of the material to be VO_2,[28] and an atomic force microscopy shows that the film had a root-mean-square roughness of ≈0.55 nm (Figure S2a, Supporting Information) and nanoscale line cracks, but the VO_2 wire device was fabricated such that line cracks were avoided as shown in the SEM (Figure 1b).

2.2. Device Voltage–Current Characteristics

The memory measurements were conducted at room temperature and in the ambient environment. The DC *VI* plot for a device with VO_2 wire dimensions $w \approx 1.7$ µm and $l \approx 4.7$ µm is shown in Figure 1d. We ramped the current between 0 and 270 µA in 500 nA increments with a resistor connected in series ($R_{series} = 5$ kΩ). The resistor did not affect I_{T1} and I_{T2}, but was kept in the setup so the current-biased experiments would be identical to the voltage-biased experiments in Section S1, Supporting Information (voltage-biased measurements require

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a series resistance to quench the current). As can be seen in the DC *VI* plot, when the current was increased (solid line), the voltage across the device dropped from ≈10 to ≈4.7 V through the first major step of the phase transition (T_1) at I_{T1} ≈91 µA and second major step of the phase transition (T_2) at I_{T2} ≈264 µA, which constituted the full phase transition from the M_1-phase to R-phase including SPT. Much smaller transition steps existed near I_{T2} (see the inset of Figure 1d). When the current was decreased (dashed line), the reverse metal-insulator transition occurred at different currents; thus, both T_1 and T_2 were hysteretic, with a smaller hysteresis width for T_1 and the larger hysteresis width for T_2 due to the predominantly thermal-driven SPT.

2.3. Nonvolatile Memory and Voltage Oscillations

To investigate the nonvolatile memory effect, we used a combination of an electrical current bias and optical writing pulse in T_1. **Figure 2**a shows the DC *VI* plot of T_1 of the device corresponding to Figure 1d at a temperature of 23 °C. The hysteresis loop was between I_{H1} ≈82.4 µA and I_{H2} ≈87.6 µA, obtained by repeating the measurements 10 times. Before writing to the memory, we held the VO_2 microwire at a current bias of I_B, which must be between I_{H1} and I_{H2}, at ≈85 µA ($I_{H1} < I_B < I_{H2}$ as denoted by Point 1 in Figure 2a) for ≈3 s. To write to the device, we turned on a ≈180 ms-long laser pulse at a wavelength of 1550 nm, incident power of ≈470 µW, and with a full-width-at-half-maximum beam diameter of ≈4.3 µm. The duration of the laser pulse was due to the instrumentation and can be reduced in the future using an optical modulator. The incident light induced the biased VO_2 device to transition to Point 2 in Figure 2a with a DC electrical resistance reduction of ΔR = 28.9 kΩ (≈31.2% of the full transition) and voltage oscillations (i.e., device was in the O-state). Figure 2b shows the DC voltage measured without (red) and with (blue) an incident laser pulse. In the blue curve, even after the incident writing laser was turned off, the DC voltage readout of the device remained at ≈6.9 V for at least 1 h (Figure S3, Supporting Information), indicating the voltage oscillations continued. As we will discuss in the next paragraph, this DC voltage was the average of an oscillatory signal. After we removed I_B for an arbitrarily long period of time, we abruptly reapplied I_B to read out the device state. We measured a DC voltage of ≈6.9 V during the read time

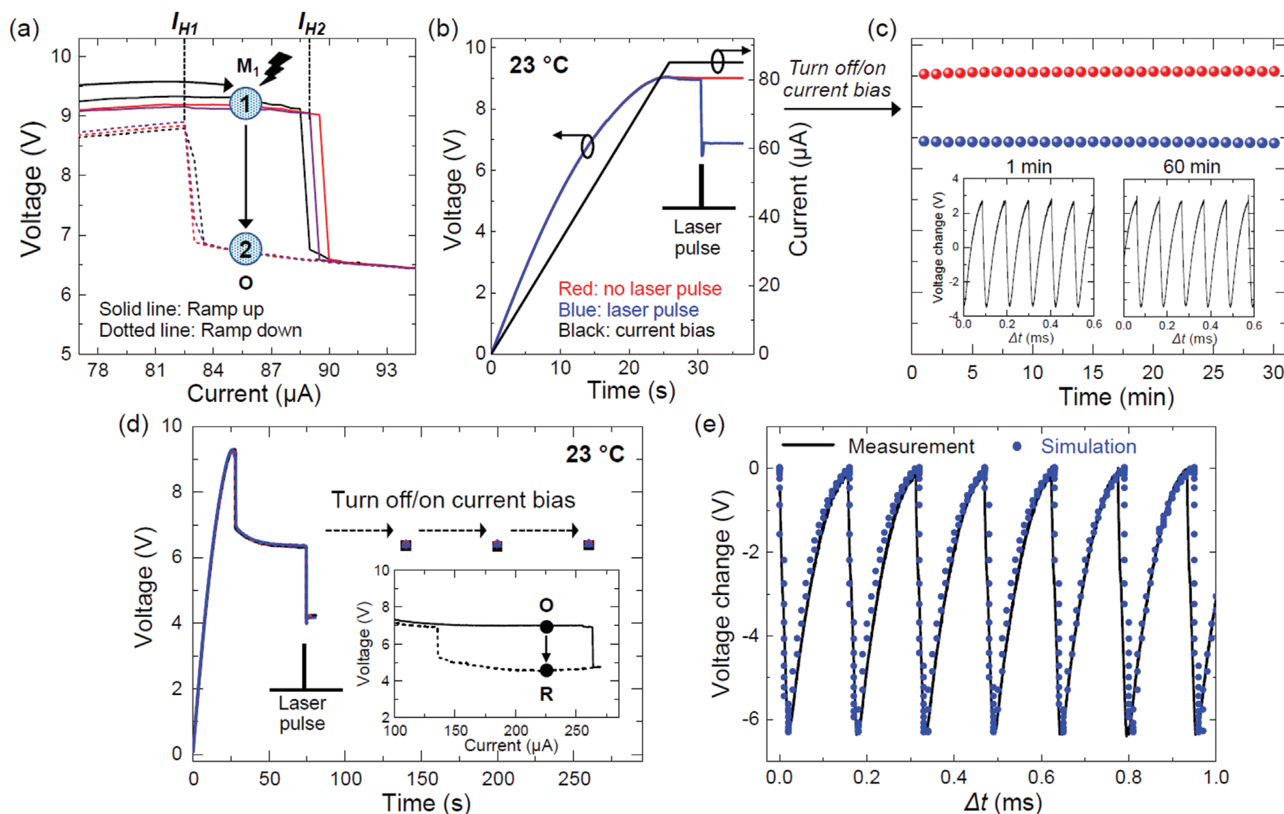

Figure 2. a) 1st hysteresis of the device (solid line: current ramp up, dashed line: current ramp down). The forward and backward transition currents are I_{H1} and I_{H2}, respectively. b) Time trace of the DC voltage across the device during a ramp up of the bias current and holding at ≈85 µA (right *y*-axis) followed by no incident optical pulse (red), and a ≈180 ms-long optical pulse at an incident optical power of ≈470 µW (blue) showing optical memory writing. c) The DC voltage readout after turning off and on the current bias every 1 min. If an optical pulse was incident (blue dots) a voltage of ≈6.7 V was read. If there was no light (red dots) a voltage of ≈9.1 V was read. Inset, voltage oscillations corresponding to the DC voltage readout of the blue dots measured after 1 and 60 min. d) Three overlapping real-time measurements of the device voltage using a bias current at the 2nd hysteresis loop (ramp up to ≈230 µA) and an incident optical pulse with power of ≈1.1 mW, including turning off and on the current bias. Inset, 2nd hysteresis loop of the device. The device returned to the O-state indicated in the inset after the bias is removed. e) Simulated and measured voltage traces in the O-state. The trace is not centered at 0 V since it was captured immediately after the transition and the DC component was not yet filtered.

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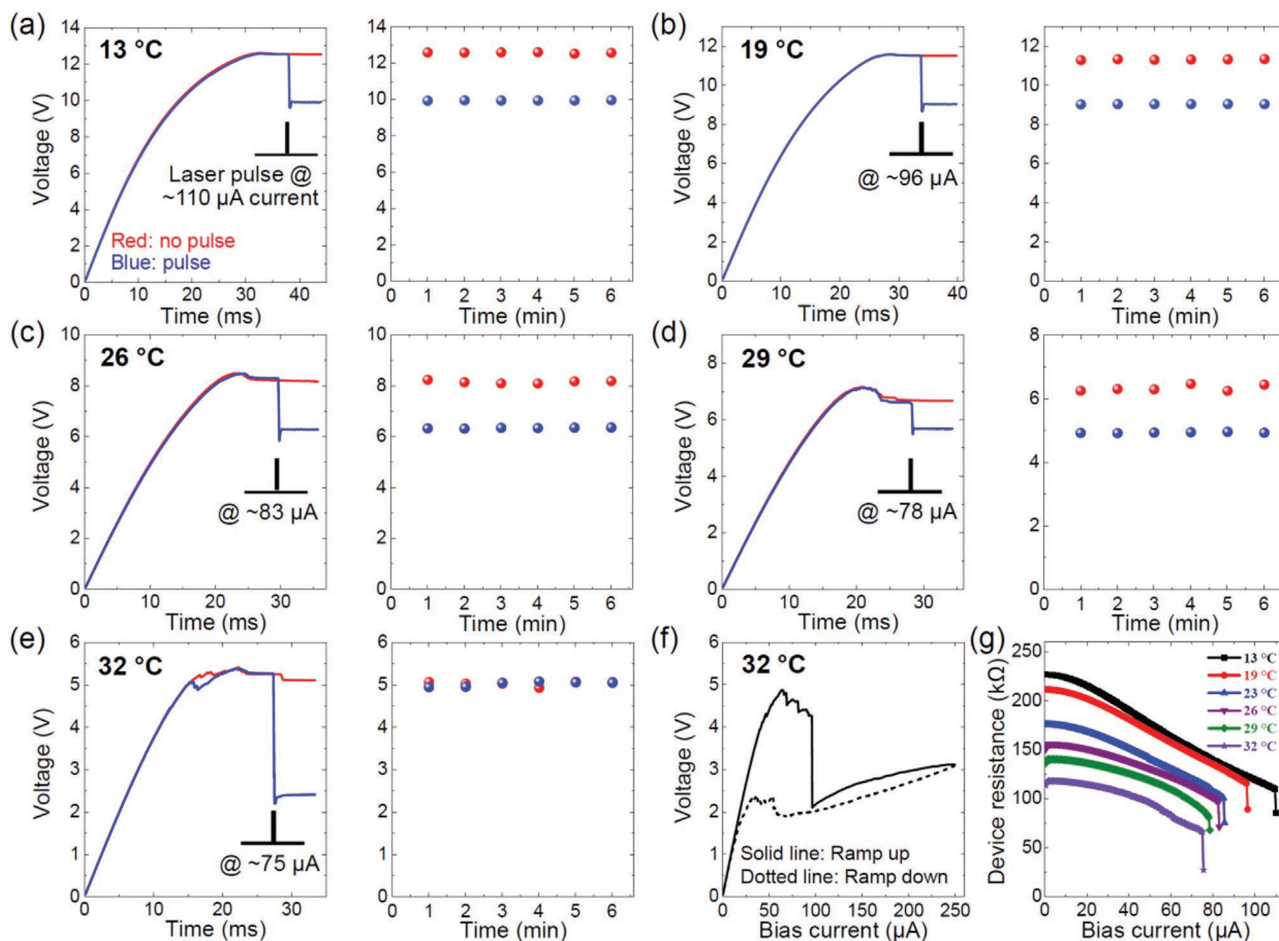

Figure 3. a–e) At temperatures ranging from 13 to 32 °C, a real-time voltage trace of the current-biased device with optical memory writing, and the tests of nonvolatile and volatile memory with the current bias turned off and on every minute. The identical optical pulse duration (~180 ms) and power (~470 μW) were used in the measurement at 13–29 °C. An incident laser power of ~1.1 mW was used at 32 °C for full SPT. f) *VI* measurement at the temperature of 32 °C. g) Device resistance changes with bias currents and a light pulse at different temperatures.

even after 3 days and without any other optical or electrical input between the writing and reading steps. Figure 2c plots the first 30 min of the voltage readings with I_B being turned on and off every minute, showing the O-state was observed every time and the memory was nonvolatile (blue dots). The red dots in Figure 2c show that when the writing optical pulse was not applied, the device remained in the M_1-phase with a DC voltage readout of ~9 V. This phenomenon was unique to the T_1 transition and the current bias operation. When we repeated the experiment at room temperature by applying a bias current in the hysteresis loop of T_2 transition (Figure 2d) or a voltage bias (Figure S4 and Supporting Information text), the device completed the SPT and functioned as a volatile memory (i.e., the R-phase did not persist without applying a current or voltage bias).

Figure 2e shows the oscilloscope time trace of the sustained voltage oscillations of the VO_2 device in the O-state after the writing incident light was turned off at a bias current of I_B. The oscillations with I_B had a frequency of ~6.5 kHz and an amplitude of ~7 V, corresponding to the full voltage drop between the M_1 and R phases in Figure 1d. The oscillation frequency in the absence of incident light was independent of the optical power of the write pulse but depended on the applied current bias. In addition, as shown in the inset of Figure 2c, oscillations were repeatedly observed each time when I_B was applied for the voltage readout. Using a circuit model for our VO_2 device (Section S3 and Figure S5, Supporting Information), the simulated oscillations (blue dots in Figure 2e) agree well with the measurements. The sustained oscillation frequency could be precisely tuned by the incident optical power of a continuous-wave laser after the memory writing process (Section S4 and Figure S6, Supporting Information) and was dependent on the external circuit component, such as capacitor and resistor.[12]

To test the hypothesis that the nonvolatile memory would not be present if the thermal energy was sufficiently high to enable the full insulator-metal phase transition including SPT,[29] we repeated the experiment at different temperatures and bias conditions. As the sample stage temperature was increased from 13 to 29 °C (**Figure 3**), the current bias for the phase transition decreased due to the increase in thermally generated carriers,[30] but the device could still function as a nonvolatile memory. When the sample stage was above 32 °C, the device could no longer function as a nonvolatile memory (Figure 3e), and the

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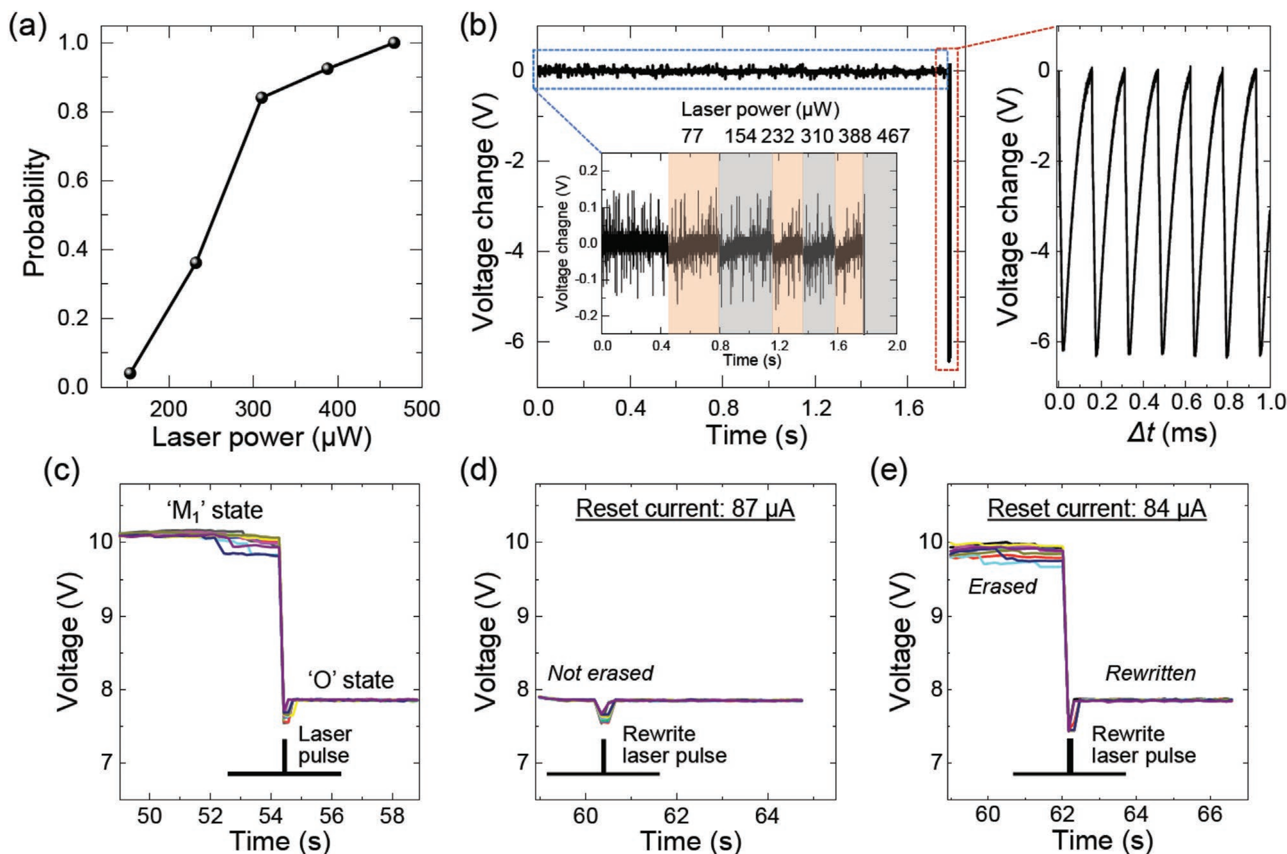

Figure 4. a) Probability that a ~180 ms-long light pulse at a wavelength of 1550 nm induces the first major transition at different optical powers. The results were determined from DC voltage measurements. b) Voltage change across the device with incident laser pulses with varying powers. The magnified plots of blue and red box regions are in the inset and right side of (b), respectively. c) Optical memory writing on a current-biased device at ~88 μA. d,e) Erasing and rewriting test with different reset bias currents. 10 measurements are overlapped.

full SPT was evident from the *VI* characteristic (Figure 3f). The device resistance as a function of the bias current and after an incident light pulse is shown in Figure 3g. For stage temperatures between 13 and 29 °C, the insulating VO_2 (with device resistance, R, > 100 kΩ) transitioned to the O-state (R = 65–85 kΩ) with the application of bias current and an optical pulse. At 32 °C, however, the device fully transitioned to the R-phase (final R ≈25 kΩ). These observations are further supported by thermal simulations (Section S5 and Figure S7, Supporting Information), which show that for a substrate temperature <~30 °C, the maximum temperature reached in the device, even with an applied bias current for the T_1 transition, remained below the full SPT temperature. To maintain the nonvolatile memory after the current bias is removed, the device temperature must be stabilized because the T_1 hysteresis shifts with temperature. However, since the device operates near room temperature, maintaining a set device temperature should not be difficult.

2.4. Threshold Optical Power

A minimum optical power was found to be necessary for memory writing and to initiate the oscillations. **Figure 4**a plots the probability of the phase transition versus the peak power of a ~180 ms-long incident light pulse with the device biased at ~86 μA. The probability was obtained from 50 measurements at each optical power (Figure S8, Supporting Information). The phase transition probability increased with the incident optical power due to the increased photo-induced carrier generation. A threshold optical power of about 470 μW was required for reliable writing of the VO_2 microwire. The inset and right side of Figure 4b show the voltage trace within the blue and red box on a magnified scale, respectively, and the sustained voltage oscillations were observed. The minimum optical power required for memory-writing can be reduced by applying a bias current closer to the transition edge.

2.5. Erasing and Rewriting the Memory

To erase the VO_2 microwire memory, the bias current should be reduced to a value outside of the hysteresis loop of T_1 transition (less than I_{H1}). After writing to the VO_2 microwire using a laser pulse (Figure 4c), we erased and rewrote to the device by applying reset currents and reapplying the ~180 ms-long and ~470 μW incident laser pulse (Figures 4d,e). In this measurement, the device was initially biased at I_B ≈88 μA, since the hysteresis loop had slightly shifted to I_{H1} ≈85 μA and I_{H2} ≈89 μA. The reset current is the current that is applied after the initial

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electrical current has been completely removed. When a reset current of ~87 µA was applied, the VO_2 was not erased and stayed in the O-state because the current was greater than I_{H1} (Figure 4d). For a reset current of ~84 µA less than I_{H1}, however, the erasing and rewriting processes were repeatable (Figure 4e). Finally, we determined how fast the bias current must be turned on and off to read the memory without erasing it. By applying trapezoidal waveforms with different slopes, we found that the maximum 0–100% rise/fall-time for the memory readout was about 150 µs (Section S6 and Figure S9, Supporting Information).

3. Discussion and Conclusion

The nonvolatile memory property reported in this manuscript, to our knowledge, has not been previously reported in VO_2. A possible explanation for this effect is an intermediate metastable phase (M*) in VO_2 in the first major transition, even though we were not able to directly characterize this phase in this work. Without M*, when the read current is reapplied after the writing process, the VO_2 should have returned to the M_1-phase and voltage oscillations would not occur. We are currently investigating the structural and dynamic properties as well as the methods to control M*. Nevertheless, the observations here show that M* can be leveraged to create nonvolatile memory devices. The nonvolatile memory behavior can also be addressable by a current as observed in the rise/fall-time experiments (described in Section S6 and Figure S9, Supporting Information). Thus, our VO_2 device could serve as both an electronically and optically written memory with oscillations. In addition, it may be possible to write to the VO_2 memory with much shorter pulses than our demonstration, potentially less than ~1 ps long.[31–33]

The recent years have witnessed a growing number of demonstrations of VO_2 memristors and VO_2 oscillator networks for neuromorphic computing (see, for example,[5,8–10]). VO_2 memristor-based artificial neurons have been shown to be exceptionally biomimetic, exhibiting most of the known dynamics of biological neurons.[5] Image recognition has been performed by a three-oscillator-VO_2-network using the phase differences between oscillations.[10] These results demonstrate the exciting computing capabilities of small networks of VO_2 coupled oscillators, though thus far without the capability of in-device memory. In comparison with optically addressable memory using other phase change materials, such as $Ge_2Sb_2Te_5$ (GST), our demonstration here required more optical energy (~8 µJ versus 13 to 600 pJ) for memory writing (see Table S1, Supporting Information); however, the energy could be reduced by reducing the device size, or shortening the optical pulse width. In addition, the absorbed optical energy could be significantly improved by integrating VO_2 wire on optical waveguides, utilizing evanescent-wave coupling which increases the interaction length, in turn, reducing the overall optical writing energy. As well, the oscillatory property of VO_2 is not present in GST, and can be exploited for oscillator-based computing. The observation of nonvolatile memory reported here can enable in-device memory in VO_2 to simplify system architectures and open new concepts for phase-change photonics and electronics.

4. Experimental Section

Device Fabrication: A 360 nm thick VO_2 film was formed on a titanium dioxide (TiO_2 (001)) substrate by pulsed laser deposition (PLD) using a VO_2 target at a temperature of 380 °C. The devices were fabricated using aligned electron-beam lithography (EBL), dry etching, and metal deposition. First, 20 µm × 20 µm tungsten alignment markers for the EBL were sputtered onto the VO_2 film. Microwires, each of which is connected to rectangular areas of size 3 µm × 48 µm at the two ends forming "H" shaped regions, were written by EBL (Raith EBPG 5000+) using ZEP-520A positive tone resist and then inductively coupled plasma-reactive ion etching (ICP-RIE) was carried out. The rectangle/square at the two ends of the wires provides a large surface area between the VO_2 and the contact pads. A gas mixture of CF_4 (10 sccm) and Ar (20 sccm) at a total pressure of 50 mTorr was used. For a fully etched VO_2, an ICP power of 300 W and RF power of 50 W was applied for 30 s. Microwires with varying lengths of 2–5 µm and widths of 1–3 µm were fabricated. Finally, palladium (Pd) electrical contact pads were formed atop of the VO_2 through EBL, thermal evaporation deposition, and lift-off processes. Pd was chosen for electrical contacts with the VO_2 due to the low work function mismatch.

Measurement Setup: The experimental setup is illustrated in Figure S1, Supporting Information. The sample was mounted on a temperature-controlled stage and accurately adjusted by a thermoelectric cooler (TEC) controller (5235 TEC Source, Arroyo Instruments) to 0.01 °C. The memory tests were performed in ambient conditions at temperatures ranging between 13 and 32 °C. The sourcing and measuring of device current/voltage were accomplished by contacting tungsten probes to the two Pd pads using a precision SourceMeter (2636A SourceMeter, Keithley) with a R_{series} = 5 kΩ resistor in series, which protected the device from being overdriven during the phase transition. For the optical addressing of the device, a 1550-nm-wavelength optical beam from a tunable laser source (81600B, Agilent) was focused on the VO_2 wire through a 100× objective lens. The full-width at half maximum (FWHM) beam spot diameter was ~4.3 µm and the incident laser power on the device ranged from 80 µW to 2.5 mW. The incident laser pulses were ~180 ms-long, limited by the time to turn the laser on and off via SCPI commands. A silicon CCD visible and InGaAs infrared cameras were used to align the device and laser beam spot, respectively. The generated voltage waveforms were measured by a 1 GHz bandwidth oscilloscope (InfiniiVision DSOX3104A, Keysight) connected to a C_{ext} = 10 nF capacitor in parallel with the VO_2 device including R_{series} via a 6 MHz oscilloscope probe (Tektronix 2220, 1× mode) (Figure S1b, Supporting Information). In Figure 2e and Figure 4b, the DC offset is not removed due to RC transients.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

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Data Availability Statement

Research data are not shared.

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