Development of a MMC demonstrator for nuclear fusion devices power supplies

A. Magnanimo[a,], G. Griepentrog[b], F. Santoro[c], C. Terlizzi[d], M. Teschke[a] and the ASDEX Upgrade Team[a]*

[a] *Max-Planck-Institute for Plasma Physics, 85748 Garching, Germany*
[b] *Technical University of Darmstadt, 64283 Darmstadt, Germany*
[c] *Consorzio RFX, 35127 Padova, Italy*
[d] *University of Rome 'Tor Vergata', 00133 Rome, Italy*

The modular multilevel converter (MMC) has become one of the most attractive converters for high-power applications such as high voltage DC (HVDC) converters, but also for fusion devices power supplies. The combination of this technology with a high power density energy storages such as supercapacitors (SC) represents a promising alternative to power the toroidal field (TF) magnets of the ASDEX (Axially Symmetric Divertor Experiment) Upgrade experiment operated at the Max-Planck-Institute for Plasma Physics (IPP) research center. After a first feasibility study, a single MMC submodule (SM) composed by four insulated-gate bipolar transistors (IGBT) forming a 4QC (4-quadrant chopper), a SC module and a power stage filter has been developed and successfully tested. Therefore, three additional identical modules were built to test their series and parallel operation in order to prove their capability to be scaled up.
This work shows the step-by-step development of the MMC demonstrator, highlighting the results of the SM synchronized operation which is fundamental for the scalability of the system. The outcome of these experiments is relevant not only for the specific application of ASDEX Upgrade TF coils, but also for many other applications due to the flexible four-quadrant operation of the converter.

Keywords: ASDEX Upgrade, Converter, Inverter, Modular Multilevel Converter, Pulsed power, Supercapacitors.

1. Introduction

The modular multilevel converter (MMC) has received considerable attention since the beginning of this century, and it has recently become one of the most attractive converter topologies for high power applications and high voltage DC (HVDC) transmission [1]-[3]. MMC have significant advantages compared with two-level converters, such as a scalable output voltage, distributed stored energy and the option to replace failed submodules (SM) in case of fault [4], while the main challenge consists in controlling simultaneously a huge number of semiconductor switches. The converter for three phase systems consists of six arms, each of which contains a series connection of n SM and an arm inductor (L_{arm}). There exist several SM configurations [5], but the most common ones are the half-bridge and full-bridge ones. Fig. 1 shows a schematic of a conventional MMC with full-bridge SM: the SM in this configuration is composed by an insulted-gate bipolar transistor (IGBT) full-bridge module (4-quadrant chopper, 4QC) and a SM capacitor, mainly acting as energy storage system. The SM capacitor is charged at voltage $v_{\mathrm{c}}(t)$ which is influenced by the phase current flowing through the three-phase load (U, V, W). Each SM can be toggled between four states: depending on the state, SM's output voltage (v_{SM}) can be v_{SC}, $-v_{\mathrm{SC}}$ or 0 (v_{SM} is 0 in two different states). In this way, the series connection of n SM per arm can be used as a discrete-leveled voltage source. If r cells of n are in the ON-state (with $0 \leq r \leq n$), the sum voltage of these r capacitor voltages is generated over the U phase of the load, and the same applies to the other two phases. These advantageous features are becoming more and more interesting to the fusion world, and at the Max-Planck-Institute for Plasma Physics (IPP) in Garching (Germany) a small-scale prototype of a revised version of the MMC has been built. ASDEX Upgrade – the largest German Tokamak – is operated at IPP, and the whole power supply is currently provided by three flywheel generators (FG) due to its pulsed power requirements [6]. The main concern about ASDEX Upgrade's present power supply system is that, in case of a permanent fault, there would be no available replacement for one or more of the three FG. For this reason, a feasibility study has been started to power ASDEX Upgrade in future with a MMC-like converter and the prototype described in this paper has been built as a demonstrator. In order to increase the available stored energy of the SM, the capacitors were replaced by supercapacitors (SC) modules. This is not the first SC-based power supply developed for fusion applications [7]-[9], but it is the first MMC-based one that has been studied to be scalable, fault-tolerant and suitable also for energy storages apart from fusion applications, such as 50 Hz grid stabilization purposes.

The next two chapters of this paper give an overview of the concept of the converter and of the developed control strategy, while the last two describe the demonstrator, providing information about the criteria used to choose the components and discussing the obtained experimental results.

*corresponding author: antonio.magnanimo@ipp.mpg.de

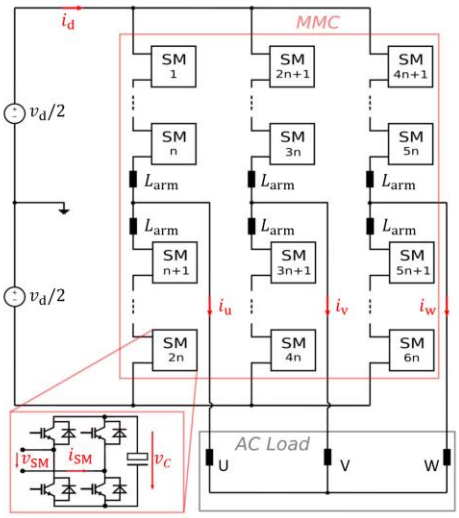

Fig. 1. *Conventional MMC with SM in full-bridge configuration [10].*

2. The proposed converter topology

Since the first prototype was built for ASDEX Upgrade's TF coils – a DC constant load - the proposed converter is an extension of a conventional MMC arm (single-phase), with the option to increase the available stored energy and output current by adding several parallel SM. This results in a *n* x *m* matrix of SM, where *n* and *m* are the number of SM in series and in parallel, respectively (see Fig. 2). SM were initially intended to be half-bridge SM - which would be theoretically enough for DC loads - but in order to increase the flexibility of the topology and make it suitable for AC loads, the full-bridge SM configuration has been chosen. This choice is optimal also in terms of reliability: in case of any SM internal fault (e.g. fault of an IGBT switching) the SM can still be by-passed thanks to the other available half-bridge without affecting the operation of the whole SM matrix, which would not be possible with the half-bridge SM configuration. In this way the converter can safely operate and failed SM can be replaced directly after the operation. The *m* parallel SM receive all the same commands and are toggled synchronously in order to simplify their control: the converter indeed can be modeled as a variable voltage source with $2n + 1$ possible voltage levels. The synchronization of the parallel SM is ensured thanks to the EtherCAT communication protocol [11]-[12]. The main objective of the converter for this application is to generate a constant output current of 54 kA for about 10 s, limiting ramp-up and ramp-down phase durations to reduce losses. During the 10 s of the flat-top phase, the current may have a ripple that must not exceed the 0.1% of current nominal value (≈ 50 A) [13]. This value directly depends on the voltage difference among different levels (Δv), on the load inductance and on the switching frequency of the converter. Since the load inductance is constant and Δv depends on the SC modules voltage, the current ripple can be reduced by increasing the switching frequency of the converter. Considering the maximum Δv as worst case at the beginning of the operation (during the operation it decreases due to the discharge of the SC modules) an output switching frequency of 25 Hz would ensure the current ripple to not exceed 50 A. The details of the full operation of this topology are presented in [13]. Note that the inductive energy stored into the TF coils during the pulse can be restored into the SC modules with the full-bridge SM.

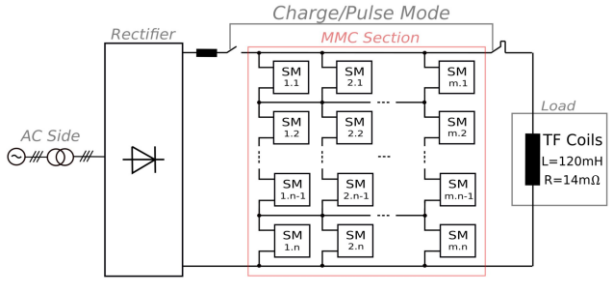

Fig. 2. *Proposed MMC-based power supply for ASDEX Upgrade's TF coils.*

3. The control strategy

The adopted control strategy of Fig. 3 is based on a closed loop current control: the load current $i_L(t)$ is measured and compared with a reference current $i_{ref}(t)$, generating an error $e(t)$. The error is then used as input for the main current controller (PI type), which provides a normalized reference voltage $v_{rn}(t)$ that can be expressed as follows:

$$v_{rn}(t) = \frac{v_r(t)}{v_{SC}(t)} \tag{1}$$

where $v_r(t)$ is the reference output voltage of the converter and $v_{SC}(t)$ is the SC modules voltage measured in real time. The internal structure of the PI controller and methods used to size its parameters have been described in [14]. The signal $v_{rn}(t)$ is then used as input by the modulation and balancing control block. This block firstly rounds the signal $v_{rn}(t)$ to the closest integer value in order to define the number of voltage levels required (modulation), and then it enables the needed number of SM depending on their respective SC module voltages (balancing). According to the real time measurements of $i_L(t)$ and $v_{SC}(t)$, a sorting algorithm arranges the SM in ascending/descending order depending on the $i_L(t)$ sign and on the rounded $v_{rn}(t)$: in this way the first *r* SM of the sorted list are selected to be enabled. On the top of this, power stages (IGBT) temperature and error signals are also checked to detect potential overheating or short circuits. Therefore, the modulation and balancing control block generates *n* output signals forwarded to each row (composed by *m* parallel and synchronized SMs) which can assume four different states:

1. SM enabled in direct mode ($v_{SM} = v_{SC}$);
2. SM enabled in reverse mode ($v_{SM} = -v_{SC}$);
3. SM by-passed ($v_{SM} = 0$);
4. Freewheeling mode.

The converter then produces the required output voltage $v_L(t)$ over the load, which generates the requested $i_L(t)$. The load current is finally measured and a new control cycle takes place. Considering maximum output current

ripple and the PI stability constraints [14], a control frequency f_C of 125 Hz has been chosen.

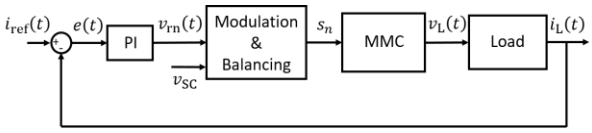

Fig. 3. *Control strategy simplified block schema.*

4. The demonstrator

The demonstrator has been designed, built and tested step-wise: the first step indeed consisted in developing a single SM. The knowledge acquired from the 1-SM prototype has then been used to extend the prototype first to a 2-SM one and then to the 4-SM demonstrator. The single SM has been tested to analyze the behavior of the SC module in a switched operation, while series and parallel operation of the developed SM could be tested with 2 SM. Finally with the 4-SM demonstrator the serial and parallel tests have been repeated with a higher number of SM and it has also been possible to operate the converter in combined serial/parallel operation.

SM configuration and components

The designed SM is mainly composed by a SC module, a power stage filter (L_{Filter}, C_{Filter}) and two IGBT-based half-bridges. The combination of two half-bridges allows the SM to operate as half-bridge or full-bridge, depending on the toggled IGBT. The SC module is a custom module from SPSCAP company, composed of 48 x 2.7 V SC cells connected in series for a total voltage of 130 V, a capacitance of 67 F, a maximum peak current of 2 kA, an equivalent series resistance (ESR) of 10 mΩ and an equivalent series inductance (ESL) of 1.5 µH. The half-bridge modules type is FF600R07ME4_B11 from Infineon Technologies with a nominal current of 600 A and a maximum collector-emitter voltage of 650 V.

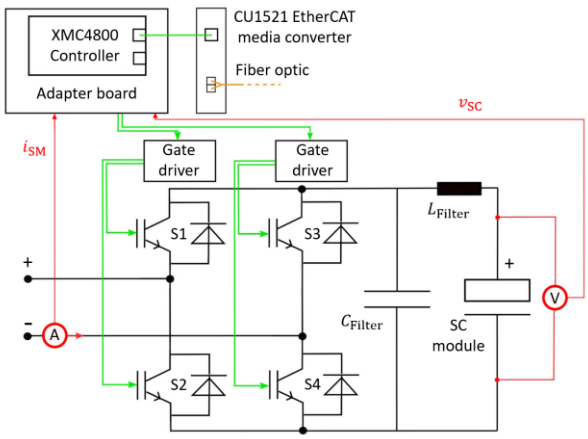

Fig. 4. *SM main components schema: in stand-alone operation only one CU1521 media converter is present, while in the 4-SM prototype each SM has two media converters for redundancy.*

The IGBT are toggled by two *2SP0115T2C0-06* gate drivers from Power Integration company, which are controlled by a XMC4800 microcontroller integrated into a custom adapter board providing power to the whole electronics of the SM. Fig. 4 and Fig. 5 show respectively a schema of the experimental setup and a photo of the SM prototype. A detailed description of the SM components can be found in [15].

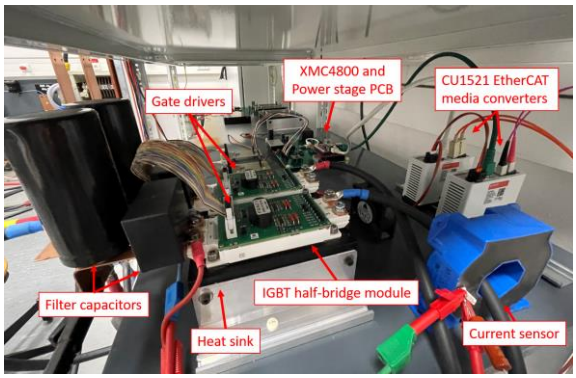

Fig. 5. *SM setup components.*

4-SM prototype

The final demonstrator was built by assembling the SM described in the last subsection together with 3 additional identical SM. The converter is controlled by a virtual PLC running on a laptop thanks to the TwinCAT software. The main controller is isolated from the converter due to the full optical communication system (EtherCAT protocol - ring topology). SM are connected to each other only by power connections, while SM electronics and controllers are isolated among each other. In Fig. 6 a photo of the prototype in parallel configuration is shown. SM are connected by two symmetric copper bars with a specific impedance, which has been defined in order to obtain a balanced current sharing during the parallel operation of the SM. More details about the parallel operation and how the bus bars were designed are provided in the next section.

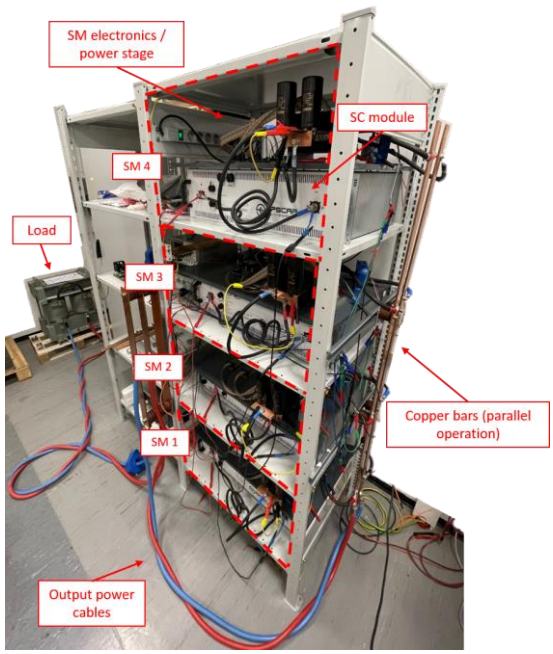

Fig. 6. *Prototype setup in parallel configuration.*

5. Experimental results

The experimental results shown in this section refer to three different configurations of the demonstrator: parallel, serial and combined serial/parallel configuration.

Parallel operation

The first configuration analyzed is the parallel one: this is the most critical operation mode since the scaling of the converter strictly depends on it. The main concern comes from the impedance of the SM interconnections ($Z_{i-1,i}$ in Fig. 7). Even though SM are toggled synchronously (the measured jitter of 10-50 ns has no relevant effect and can be neglected) a different effective load impedance for each SM causes a different time constant (τ) for the SM currents and unbalancing during transients.

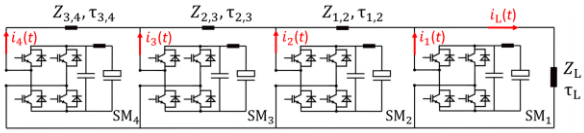

Fig. 7. *Parallel configuration schema.*

The tests consisted in charging the SC modules at $v_{SC}(t) = 20$ V and a subsequent discharge to an inductive load, emulating a small-scale TF coil. Therefore, the four SM alternate their state between states 1 and 3 (described in section 3) with a switching frequency of 50 Hz. The load which replicates the small-scale TF coil is a 8 mΩ / 750 μH inductor whose time constant τ_L is large enough to ensure a continuous conduction mode with these operating parameters. During state 1, S1 and S4 are ON (see Fig. 4), so the SC modules are connected to the load: the SM currents $i_{1...4}(t)$ pass through the SC modules' ESR and filters resistances, which damp any transient oscillations; during state 3 instead the currents by-pass the SC modules and they decrease following the natural response of the formed RL circuit according to the formula:

$$i_i(t) = I_{i0} e^{-\frac{t}{\tau_{i-1,i}}}, \tag{2}$$

where i=1…4, and I_{i0} is $i_i(t = 0)$. By applying the superposition principle the time constants can be defined as follows:

$$i_1(t) = I_{10} e^{-\frac{t}{\tau_{0,1}}}. \tag{3}$$

$\tau_{0,1}$ is τ_L (neglecting the parasitic parameters of the cables) which can be calculated as:

$$\tau_L = \frac{L_L}{R_L} = \frac{750\ \mu\text{H}}{8\ \text{m}\Omega} = 0.09\ \text{s}. \tag{4}$$

By applying the procedure to the i parallel SM, and considering that the designed $Z_{i-1,i} = Z_c$ (with an inductance L_c, a resistance R_c and time constant τ_c), $\tau_{i-1,i}$ is:

$$\tau_{i-1,i} = \frac{L_L + (i-1)L_c}{R_L + (i-1)R_c}. \tag{5}$$

In order to obtain a perfect current sharing during transients, all the time constants must be imposed to be equal. Therefore, combining (4) and (5):

$$\frac{L_L}{R_L} = \frac{L_L + (i-1)L_c}{R_L + (i-1)R_c}, \tag{6}$$

leading to the solution:

$$\tau_c = \tau_L. \tag{7}$$

The copper bus bars were designed considering as main constraint the load L-R ratio to be equal to 0.09 s. The second considered constraint was resistance value, to be kept as low as possible in order to reduce losses and additional unbalancing in steady state conditions. By imposing $R_c = 0.05$ mΩ (steady state unbalancing lower than 1 A among first and last parallel SM), the required $L_c = 4$ μH has been calculated. Fig. 8 and Fig. 9 show the experimental results obtained by performing the experiments with the designed bus bars. In Fig. 8 the total load current is shown in green and it is exactly four times the single SM currents (i_{SMi}) in both States 1 and 3. In Fig. 9 the same test is shown with a different time-scale: in this case the focus is on the transient during the transition from State 1 to State 3; apart from a negligible residual current difference (less than 2 A for 500 μs) due to the non-ideality of the components, the measured curves confirm the proper copper bars calculation and design. These results demonstrate the scalability of the system, since a balanced current sharing of the SM current leads to a symmetrical distribution of the losses over the parallel SM, crucial for the lifetime of the SC modules and their respective power stages.

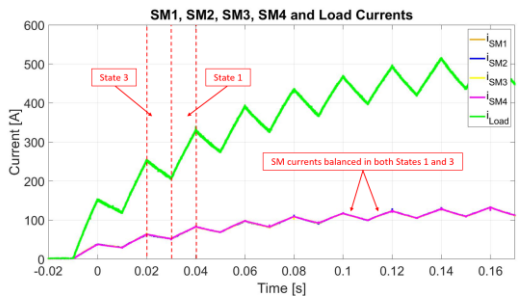

Fig. 8. *Measured currents in parallel configuration; load current in green; SM current overlapped with the magenta line.*

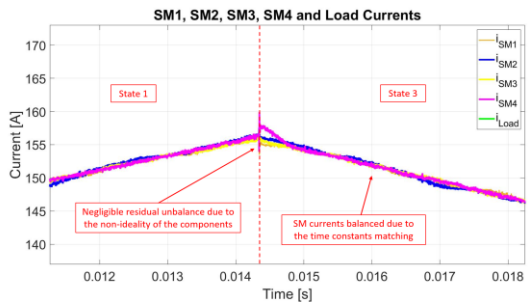

Fig. 9. *Measured currents in parallel configuration with a focus on a transient.*

Serial operation

The serial connection of the 4 SM has been useful to test the developed control strategy. The main purpose of these

tests was to define a reference load current similar to the one required by the ASDEX Upgrade's TF coils, and generate with the converter an output current as close as possible to the reference, keeping the current ripple below a specific value and the SC voltages balanced. Fig. 10 shows the electrical scheme used for the experiments.

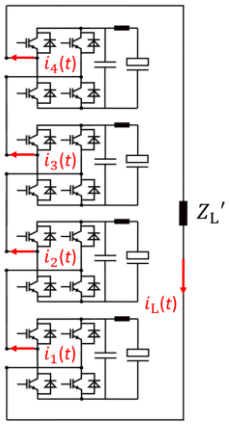

Fig. 10. *Serial configuration schema.*

In this case the load current is conducted through the four SM, therefore $i_1(t) = i_2(t) = i_3(t) = i_4(t) = i_L(t)$. The tests consisted in charging the SC modules at $v_{SC}(t) = 15$ V and to perform then a 2 s discharge with a reference current $i_{ref}(t) = 200\ A$. Since the load current ripple Δi depends on L_{Load}, on the switching frequency f_{sw} and on the voltage applied on L_{Load} [13], a new load (25 mΩ / 5 mH) with a higher inductance has been used, in order to obtain a relatively low Δi even operating at low power conditions.

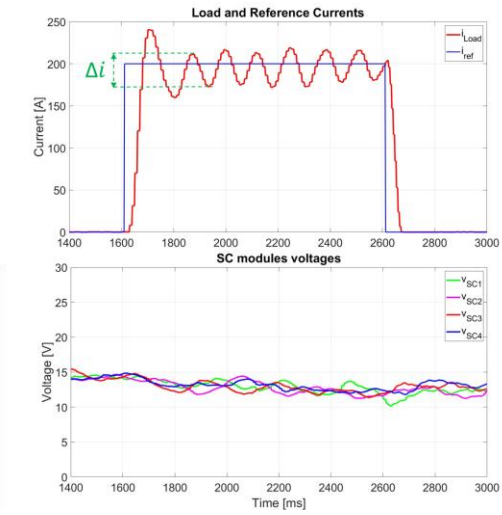

Fig. 11. *Measured load current and SC module voltages during a 200 A / 2 s experiment.*

In Fig. 11 the experimental results are shown: $i_L(t)$ raises rapidly during the ramp-up phase and reaches the reference with a small overshoot coming from the fact that the controller enables all the available SM during this phase; since the SM (and the controller) are rated for 600 A, its step response is slightly underdamped. During the flat-top phase the controller alternates the number of enabled SM between 2 and 3 in order to limit the current ripple, which is approximately 35 A for the whole flat-top, while once the reference current is zero again, the controller disables the 4 SM (State 4) and the inductive energy stored into the load conducts through the antiparallel diodes of the SM' IGBT recharging the SC modules of a few hundreds of mV. As shown in the lower curves of Fig. 11, the controller enables the SM depending on their voltage levels according to the voltage balancing algorithm and the maximum voltage variation (Δv) between different SC modules is lower than 2 V.

Combined serial/parallel operation

Having validated both serial and parallel operation, the combined serial/parallel operation has been used to repeat the tests done for the serial configuration, but with twice the available energy from the single row, composed first by a single SM, while in this case by two of them in parallel. Furthermore, by connecting in parallel two SM, their ESR (as well as the parasitic resistances of their circuits) was halved, becoming negligible compared with the load resistance. This was not the case for serial connection of 4 SM, where the sum of their circuits' resistances was larger than the load resistance (Z_L' in Fig. 10 includes indeed such equivalent resistance), limiting significantly the possible maximum load current.

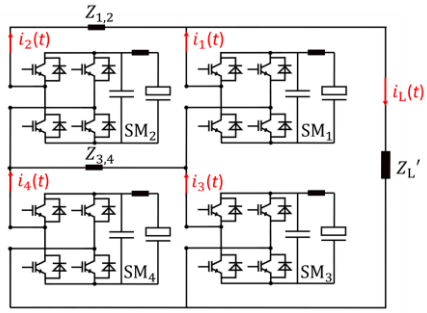

Fig. 12. *Combined serial/parallel configuration schema.*

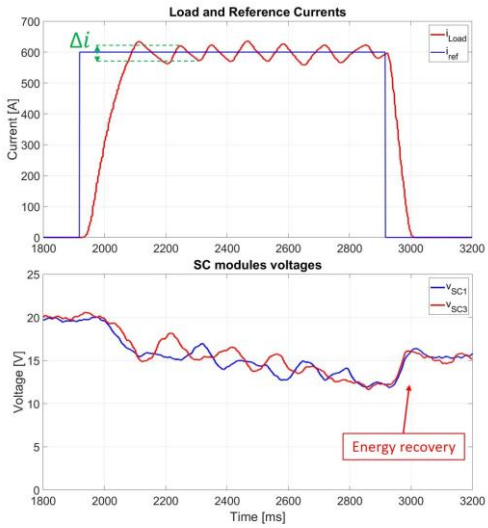

Fig. 13. *Measured load current and SC module voltages during a 600 A / 2 s experiment.*

In this configuration (see Fig. 12) $i_1(t) = i_3(t)$ and $i_2(t) = i_4(t)$ in steady state conditions, therefore $i_L(t) = i_1(t) + i_2(t)$. The same experiment performed in the serial configuration was repeated, with the differences of $v_{SC}(t) = 20$ V and $i_{ref}(t) = 600$ A due to the higher available energy. The better power matching between

source and load leads in this case to a Δi reduction in comparison with the previous case. Due to the higher SM currents the amount of energy consumed (proportional to SC voltages) has also increased and this can be clearly seen in the bottom side of Fig. 13: the SC voltages drop from 20 to 12.5 V during the test and recover 2.5 V at the end of it, corresponding the stored energy into the load inductance.

6. Conclusion

SC represent a promising solution in the new generation of power supplies for tokamaks and the combination of the attractive features of this technology with the MMC can play a key role in the fusion field as well as in many other pulsed power applications. This paper shows the development of a MMC small-scale demonstrator hardware with 4 SM and the results of some experiments performed. The tests were able to show the operation of the demonstrator in three different configurations: serial, parallel and combined serial/parallel. The outcome of the experiments in the parallel configuration is important to scale up the converter since they confirmed that with a proper ratio among L_c and R_c (inductance and resistances of parallel SM interconnections) the steady state current displacement among first and fourth SM is less than 1 A, while during transients it can be neglected due to low amplitude (2 A) and short duration (0.5 ms). The calculations can be adapted for larger numbers of parallel SM and proper values of L_c and R_c can ensure a balanced current sharing for full-scale devices as well. The serial operation has been implemented to test the developed control strategy, demonstrating that the converter output current is able to follow its reference with a ripple limited only by the circuit parameters, meaning that the controller has been properly designed. Finally, the combined serial/parallel operation has confirmed the results obtained in the previous case by repeating the tests with a higher available energy and output current. The developed and tested demonstrator can be used as a starting point to build a middle-scale or full-scale power supply for ASDEX Upgrade or other fusion devices, and apart from it, due to the flexible 4-quadrant operation it can be useful for non-fusion applications as well.

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