학사학위논문

Improvement of Two Dimensional Lead Free Perovskite Transistor Performance by Using Polymer Dielectrics

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1. Introduction

Perovskite is the most promising material, which can be applied in various optoelectronic fields due to its high optoelectronic properties and advantages of easy manufacturing processes. Applied to field-effect transistor (FET), the prominent electronic components for electronic devices, research on perovskite FET is actively underway. As Pb-based perovskite has toxicity issue, it makes commercialization of Pb-based perovskite FET difficult. Therefore, the importance of research on Sn-based perovskite in the application of FET is improving. However, Sn-based perovskite field-effect transistor also generates several problems such as ions movement and air stability.

The main aim of the project is to solve the air stability problem of Sn-based perovskite field-effect transistor. In this research, the improvement of 2D lead free perovskite FET performance will be studied by comparing the device performance when using different polymer dielectrics in optimum configuration.

1.1. Field-effect transistor

Field-effect transistors, so called FETs are semiconductor devices that are widely used in various electronic applications due to their intrinsic advantages, such as excellent electric signal amplification function, multi-parameter accessibility, high reliability and endurance, low cost, and easy implementation in a wide range of circuits.[1]

1.1.1. The principle of FET

A field-effect transistor is type of device using electric field to control the current flow through a semiconductor channel. It has three-terminal, source, drain and gate. The source and drain are connected to the semiconductor and the gate is isolated by the dielectric layer. Charge carriers flow from source to drain.

When the gate voltage is applied, an electric field is created between the source and gate inducing the current in the channel area between the source and the drain electrodes. This electric field regulates the conductivity of the channel as well as the current flow between source and drain electrode. A positive voltage applied to the gate of FET with an *n*-type of channel attracts free electrons, enhancing its conductivity and facilitating greater current flow between the source and drain. A negative gate voltage on a *p*-channel FET repels holes, enhancing conductivity. The conductivity and current flow across the channel can be adjusted by changing the gate voltage and drain voltage as shown in Figure 1.[2]

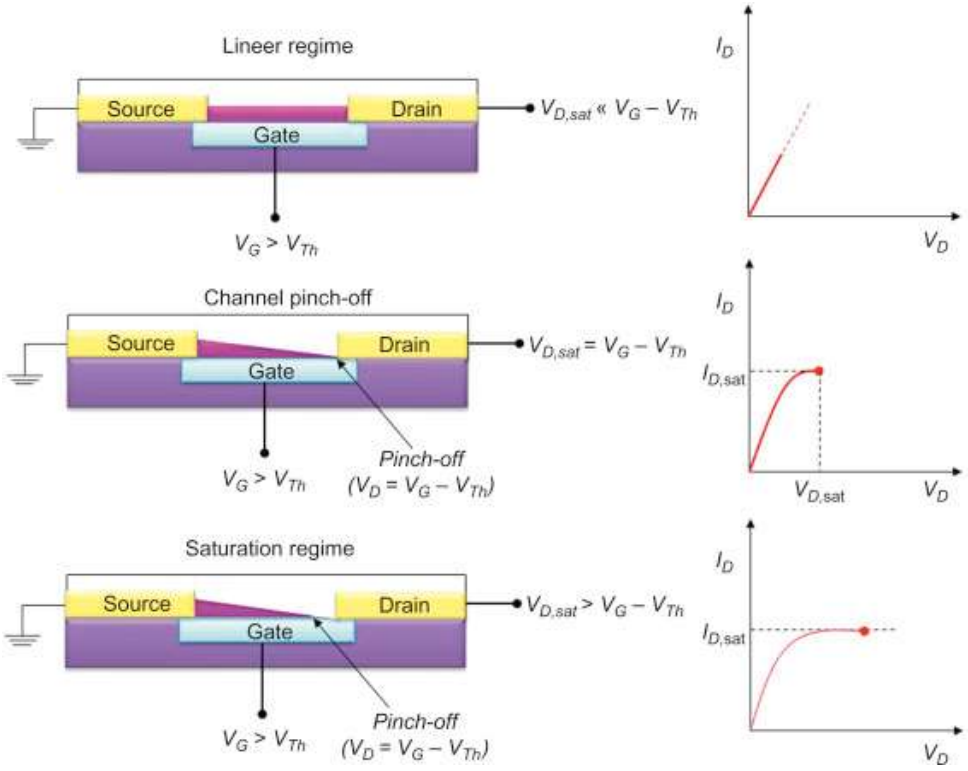

Figure 1. *Scheme of FET working mechanism[2]*

1.1.2. Device configuration

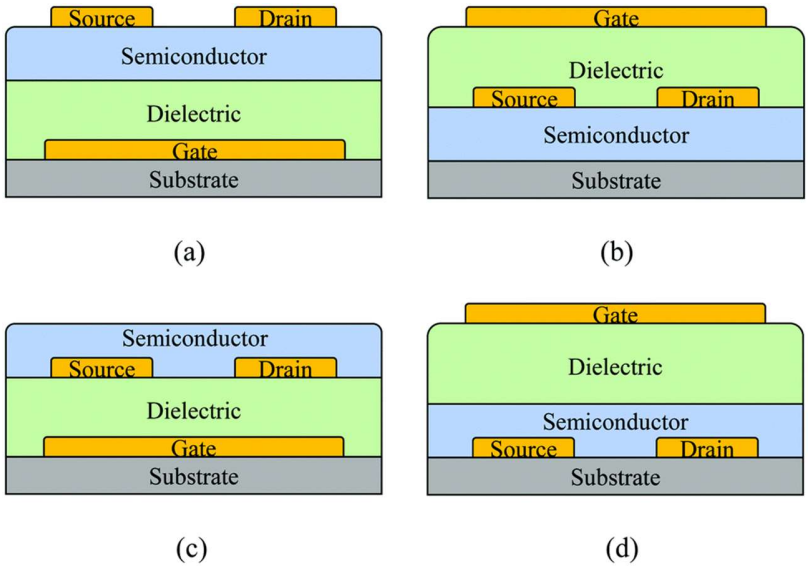

Figure 2. *Device structures of perovskite FETs with four different configurations. (a) bottom gate, top contacts (BGTC), (b) top gate, top contacts (TGTC), (c) bottom gate, bottom contacts (BGBC), and (d) top gate, bottom contacts (TGBC). [3]*

Field-Effect Transistors have four configurations as shown in Figure 2, bottom gate, top contacts (BGTC), top gate, top contacts (TGTC), bottom gate, bottom contacts (BGBC), top gate, bottom contacts (TGBC). Particular arrangement of each configuration varies, but have following rules in order. The source and drain electrodes must be in direct contact with the semiconductor material, and the gate electrode, which is used to regulate the current in the channel created between the source and drain electrodes, has to be isolated from the semiconductor material by a dielectric layer.

The transistor is built up layer by layer. Source and drain electrodes are always metal contacts like Cr and Au, deposited by thermal evaporation. Gate electrodes can be a metal like Al or a conducting polymer. Semiconducting layer can be deposited with solution processes such as spin-coating and drop-casting or vacuum processes.

1.1.3. Device performance

To measure device performance and determine operating properties, several key parameters should be determined. For example, field-effect mobility (μ), threshold voltage (V_{TH}), on/off current ratio (I_{ON}/I_{OFF}), hysteresis, and subthreshold swing (SS). These parameters are affected by various factors, such as material properties, semiconductor film morphology and device geometry. In general, high μ, low V_{TH}, large I_{ON}/I_{OFF}, low hysteresis and small SS values are required for a well- performing transistor.[4]

The performance of FETs is usually characterized by measuring the output and transfer characteristics. Output characteristic of FET is the variation in the drain source current I_{DS} with varying drain source voltage V_{DS} under defined gate voltage V_{GS}. Transfer characteristics of FET is the variation in the drain source current I_{DS} with varying gate voltage V_{GS} under constant drain source voltage V_{DS}.

1.1.3.1. Field-effect mobility (μ)

By the charge carrier mobility measurement, performance of charge carrier transport is defined. If mobility is high, it indicates that charge carriers can be transported efficiently along the conducting channel, and the efficiency of the FET devices is increased as the drain current rise up. The field-effect mobility is calculated in either the linear or the saturation regime. In Linear regime the current simply increases with voltage according to Ohm's Law, where $V_{DS} << V_{GS}-V_{TH}$. In the saturation regime the current reaches a maximum value showing constant value with increased voltage, where $V_{DS} > V_{GS}-V_{TH}$. Each mobility of linear and saturation regime are calculated using Eq.(1) and Eq.(2), respectively.[5]

$$\mu_{linear} = \frac{dI_{DS}}{dV_{GS}} \cdot \frac{L}{WC_iV_{DS}} \qquad \text{Eq.(1)}$$

$$\mu_{saturation} = \frac{2L}{WC_i} \left(\frac{d\sqrt{I_{DS}}}{dV_{GS}}\right)^2 \quad \text{Eq.(2)}$$

where W is channel width, L is channel length and C_i is the dielectric capacitance per unit area.

1.1.3.2. Threshold voltage (V_{TH})

The V_{TH} of the FET is minimum gate bias voltage required to observe on-state current flow, the voltage at which the FET turns to the on-state from the off-state. Device show on-state current flow when V_{GS} is higher than V_{TH}. The device with low V_{TH} is preferred because it offers high speed performance and low power operation.

1.1.3.3. On-off ratio (I_{ON}/I_{OFF})

On-off ratio is ratio between on-current and off-current through the channel. The on-current is defined as the maximum current at given gate voltage and the off-current is defined as the current at the gate voltage at 0 volts. High on-off ratio is preferred as it indicates that the FET is highly switchable, therefore, device responses in high speed.

1.1.3.4. Hysteresis

Hysteresis is discrepancy in forward and reverse pathways of state transitions. Large hysteresis is generated by ion migration and charge traps inside a gate dielectric layer. This is undesired because it leads to an inaccurate estimation of the device efficiency. Therefore, hysteresis should be minimized or eliminated to improve the device stability and reliability.[6]

1.1.3.5. Subthreshold swing (SS)

The meaning of subthreshold swing is the minimum required gate voltage to improve drain current by one order of magnitude. The smaller the value, the steeper the slope in transfer characteristics, resulting in less trap density of the device, indicating better ability of channel control.

1.2. Perovskites

Perovskites are a class of materials with specific crystal structure of molecular formula AMX_3, where *A* is an organic cation (e.g. methylammonium (MA), formamidinium (FA), CS^+), *M* is a metal cation (e.g. $Pb2^+$, $Sn2^+$), and *X* is a halide anion (e.g. I^-, Br^-, Cl^-, F^-), having specific crystal structure as indicated in Figure 3.

Figure 1. *The perovskite crystal structure with the general form ABX_3.[7]*

It was named after Russian mineralogist L. A. Perovski (1792–1856), who first discovered original perovskite material, $CaTiO_3$. As changing material of each *A*, *B*, and *X* cite, perovskites obtain different size, wide- range optoelectronic properties, and various applications.

1.2.1. Advantage of perovskites

Perovskites are among the most extensively investigated materials in the second decade of the twenty-first century due to their exceptional intrinsic optoelectronic properties, which includes tunable band gap, relatively high charge carrier mobility, diffusion length, high absorption coefficient, and photoluminescence quantum yield obtained by its special crystal structure.[8]

They also have the advantages of better feasibility, easier processing by solution processing method, and greater flexibility when fabricated into devices, compared to conventional semiconductors.[5]

1.2.2. 2D/3D Perovskites

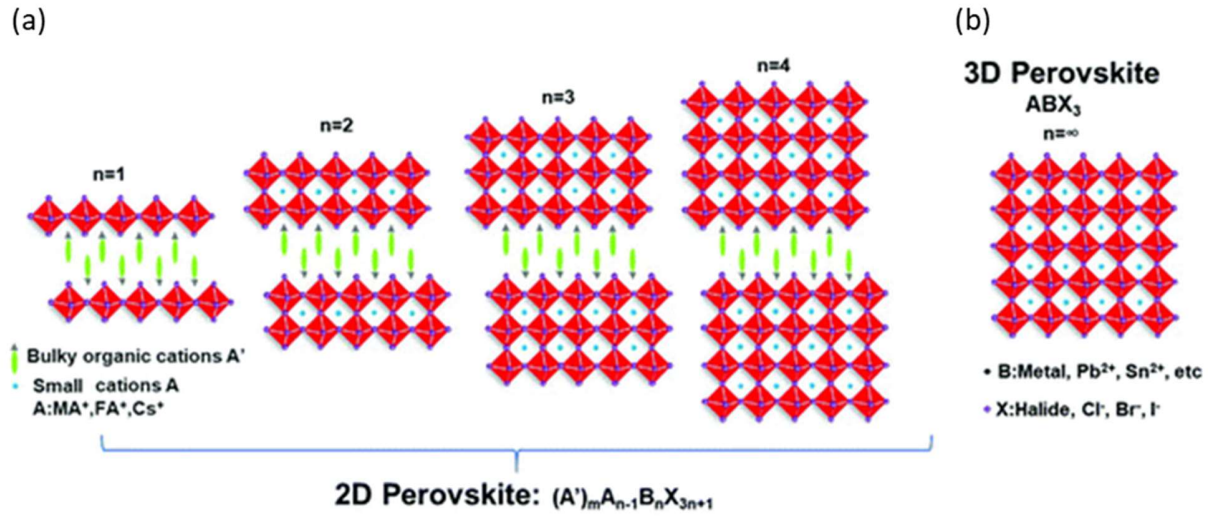

***Figure 2**. Schematic illustration of (a) 2D and (b) 3D perovskite materials.[9]*

The 3-dimensional (3D) and 2-dimensional (2D) halide perovskite semiconductors with Van der Waals layered crystal structure are shown in Figure 4. Despite its high transport mobility, the application of 3D perovskite materials has the problem of poor long-term stability and easy destruction in the surrounding environment due to its hydrophilic nature and sensitivity to temperature and humidity.

Improved moisture stability was observed for 2D perovskite materials compared to 3D perovskites due to the application of air stable organic cations. 2D perovskite semiconductors are obtained by combining large organic cations, such as phenylethylammonium (PEA) in the *A* site. These bulky organic cations are introduced into octahedral Pb-I repeating units to form 2D halide perovskites, and thereby, environmentally stable.[10]

1.3. 2D perovskites field-effect transistor

Due to their optoelectronic properties, metal halide perovskites have a wide range of applications including solar cells, lasers, photodetector, light-emitting diodes (LEDs), and neuromorphic devices.[11, 12] Perovskite field-effect transistors (FETs) are also known as a potential area of an application for perovskite.

Perovskite is used as semiconducting channel in FET. A perovskite field-effect transistor can be used as fundamental component for modern digital integrated circuits and also the platform to determine physical properties like charge transport property.[13] Through their adaptable substrate and controlled charge transport mechanism, field-effect transistors (FETs) can offer a great platform into the evaluation of transport physics of perovskites.[14]

1.3.1. Sn-based perovskite FET

Lead halide perovskites have demonstrated excellent performance in application of various optoelectronic devices like light-emitting diodes, solar cells, and FETs. However, the toxicity of lead (Pb) significantly hinders its widespread use and commercialization. Since there's a risk of human exposure to Pb during the manufacturing and handling of perovskite devices, the European Union restricted exposure up to 1000 ppm in all electronic devices to prevent problems related to Pb.

Recently, attention has been focused on replacing Pb with low-toxicity and non-toxic cations. Ideal lead-free candidates should have low toxicity, narrow direct bandgap, high optical absorption coefficient, high mobility, low exciton binding energy, long carrier lifetime, and stability. Several potentially less toxic and chemically compatible materials, such as Sn, Bi, and Ge have been proposed as alternatives to Pb to not only reduce the toxicity of Pb but also preserve the unique optoelectronic properties of perovskites. Among them, Sn, which is an environmentally friendly material, is widely used in various promising optoelectronic devices such as solar cells and FETs as it fulfils the prerequisites of charge balance, ion size, and coordination. [8] Sn is a group 14 element in the periodic table, and it has a similar ionic radius (115 pm) to Pb (119 pm). Like Pb, Sn has inert outer orbitals, which are important for achieving the special electrical and optical properties of metal halide perovskites. Compared to Pb-based perovskites, Sn-based perovskites also exhibits similar excellent optoelectronic properties of narrow band gap of about 1.3 eV, high charge mobility of about 600 $cm^2V^{-1}s^{-1}$, long carrier diffusion and lifetime, and high absorption coefficient about 10^{-4} cm^{-1}.[15] However, due to poor stability of Sn in moisture and oxygen-presence environment, it shows lower performance compared to Pb. Therefore, for the sake of the environment and humans, continuous and intensive research is required to solve the problem of poor performance when replacing Pb with Sn in perovskite field-effect transistor.

1.3.2. Problem in Sn-based perovskite FET

As lead toxicity threatens human health, and thereby affect commercialization and market accessibility, Sn-based perovskites are found to be a safe alternative. However, it brought efficiency decrease and other new problems such as ion migration and stability, resulting significant negative impact on device performance. Ion migration within perovskites shields the applied gate electric field, causing instability in optoelectronic devices with low field-effect mobility and large current-voltage hysteresis.[16]

Main challenge of tin perovskite is air instability. Sn^{2+} easily oxidase to Sn^{4+} in oxygen, moisture environment and brings severe damage in device performance. Many methods such as adding additives or using 2D Sn perovskite have been discovered to solve this problem, but still, there's no significant solution. Thereby, further research is required to solve the problem for commercialization and effective use of the device.

1.3.3. Solution

Mentioned problems in perovskite transistor, especially air stability, can be improved by changing transistor configuration from bottom gate, top contacts (BGTC) to top gate, bottom contacts (TGBC). Unlike BGTC configuration which has SiO_2 dielectric layer underneath perovskite layer, TGBC shows dielectric layer coated on the perovskite layer. Various polymer can be used to form the dielectric layer. Therefore, the dielectric layer can protect the perovskite layer from surrounding environment including moisture and oxygen. By changing polymer dielectric, further increase in device performance is expected.

1.4. Purpose of experiment

The purpose of this experiment is first, to make Sn-based perovskite FET with applicable performance, and second, to protect the perovskite layer with different polymer dielectrics. As mentioned, Sn-based perovskite FET has problems of ion migration and poor air stability. In BGTC Sn-based perovskite FET, Sn^{2+} easily oxidase to Sn^{4+} in air, affected by oxygen and moisture, and crystal structure destroys. It causes serious damage to the device performance.

In this research, the main object of the project is to solve the air stability problem by changing and optimizing device configuration from BGTC to TGBC. By using TGBC Sn-based perovskite FET, dielectric layer can act as a protection film of perovskite layer, deposited on top of it. Various polymer dielectrics will be tested to find optimum dielectric layer, which can effectively encapsulate perovskite layer from air condition. Increasing the stability and device performance of TGBC Sn-based perovskite FET could make it possible to apply Sn-based perovskite transistor to various fields and make great progress in commercialization.

2. Materials and methods

2.1. Chemicals

2.1.1. $(PEA)_2SnI_4$

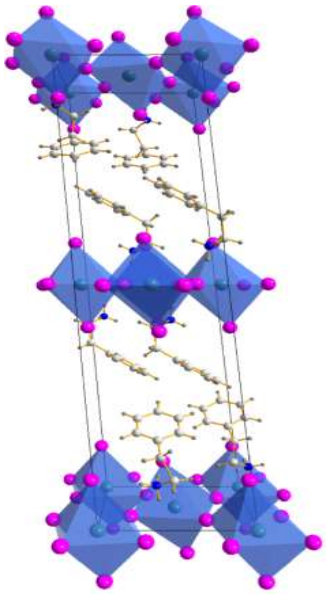

Figure 3. *2D $(PEA)_2SnI_4$ perovskite structure. Magenta represents I atoms, dark green represents Sn atoms. [17]*

In this project, $(PEA)_2SnI_4$ is used as a perovskite layer. The material has structure of two-dimensional Sn−I octahedron layers, stacked on top of each other, separated by two layers of organic cations, PEA^+ as indicated in Figure 5.

In order to make the solution, PEAI 24.9mg, SnI_2 18.6mg, DMF 250µl, and DMSO 250µl were stirred at rotation speed of 380rpm for 3 hours. In spin coating process of the perovskite layer, parameters of 60s/4000[1/min]/2000[$1/s^2$] was used and afterwards, heated for 60 min at 90°C.

2.1.2. Polymer dielectrics

The gate dielectric plays a key role in FETs, such as insulating and capacitive properties. Among the variety of materials that can be selected, polymer-based gate dielectrics offer several merits when constructing FETs with their functional molecular structure and inherent flexibility. It also has advantage in processing that it requires low temperatures which is more energy-efficient methods.[18] As device have wide range of performance with different use of polymer dielectrics, further research is required to find optimum polymer dielectrics for better device.

Various masses of Poly(methyl methacrylate) (PMMA), including 15kDa, 77kDa, 97kDa, 110kDa, 350kDa, 996kDa, various masses of Polystyrene (PS), including 35kDa, 190kDa, 192kDa, 280kDa, 350kDa, 500kDa, and other polymer dielectrics including Poly(α-methyl styrene) (PMS) 72kDa,

Poly(4-tert-butylstyrol) (PTBS) 50-100kDa, Polydimethylsiloxane (PDMS) 74kDa, Polyvinylidenfluorid (PVDF) 275kDa, polyethylene oxide(PEO) 400kDa, Polyethylene (PE) 35kDa, Polyvinylidene fluoride (PVPF) 29kDa, Poly(4-vinylphenol-co-methyl methacrylate) (PVP-co-PMMA) 220kDa have been used to determine the optimum dielectric.

Polymers were dissolved in solvent, chlorobenzene with the concentration of 30mg/ml. In spin coating process of the dielectric layer, parameters of 60s/2000[1/min]/500[1/s^2] was used and afterwards, heated for 60 min at 90°C.

2.2. Methods

2.2.1. Profilometer

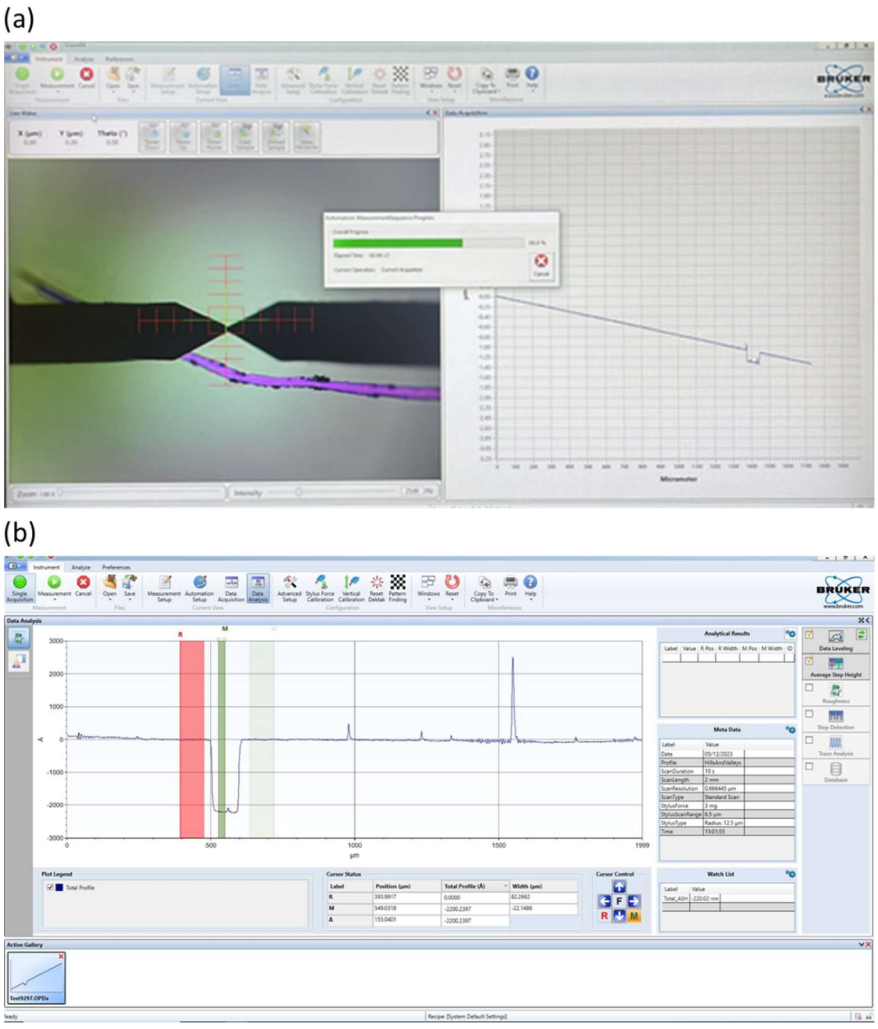

Figure 4. *Display of measurement of thickness using profilometer. (a) measurement proceeding, (b) calculation of thickness.*

To find optimum polymer dielectrics to increase performance of the device, checking thickness of each dielectric layer with different polymer is required. If the thickness is too thin, it cannot perform well as a dielectric layer, and it is same in opposite case. To set the criteria, optimum thickness will be defined by measuring device performance of different thicknesses.

Thicknesses are obtained using the profilometer (Bruker DektakXT® stylus profilometer) at ambient conditions. It was measured in following setting: standard scan type, range of 6.5µm, profile of hills and valleys, radius of 12.5 µm, stylus force of 3mg, length of 2000µm, duration of 10s and resolution of 0.666µm, as shown in Figure 6.

2.2.2. AFM

AFM used to confirm surface morphology of perovskite layer. Information such as uniformity of the surface, roughness, and grain size can be obtained by the method.

Scans were obtained using a Bruker Dimension Icon FS AFM in tapping mode at room temperature, at ambient conditions.

2.2.3. XRD

In order to confirm the perovskite structure 2θ scans of deposited films onto SiO_2 were performed by using an X-Ray diffractometer (Rigaku D/MAX 2600 V) with Cu Kα (λ = 1.5406 Å) radiation. The interlayer distance was calculated from Bragg's law: $2dsin\,\theta = n\lambda$, where θ = 5.66° and n = 2, respectively.

2.2.4. UV-VIS-Spectroscopy

Absorption values are obtained using a Helios-Fire pump-probe setup (Ultrafast Systems).

3. Results and discussion

3.1. Perovskite Morphology

3.1.1. AFM

In order to confirm the typical surface morphology, commonly observed in the literature, the AFM analysis was performed for $(PEA)_2SnI_4$ sample obtained according the deposition procedure described in previous chapter. Different scale of AFM images of the perovskite are presented in Figure 7. Perovskite forms uniform layer by the spin coating method with grain size of 2 μm which is commonly obtained at the literature[19].

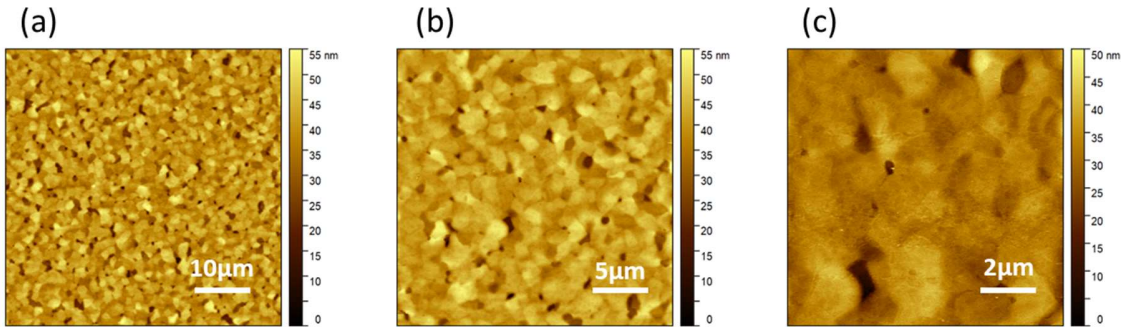

Figure 5. *AFM images of the* $(PEA)_2SnI_4$ *perovskite film with different scale. (a) 50μm*50 μm, (b) 25μm*25 μm, (c) 10μm*10 μm.*

3.1.2. XRD

The XRD pattern of the film in Figure 8 exhibits typical (00l) diffractions peaks (l = 2, 4, 6, 8, 10, and 12), confirming a layered and well-ordered structure of the $(PEA)_2SnI_4$ films. The interlayer spacing of 16.2 Å is obtained. The full width at half-maximum (FWHM) of the (002) diffraction peak is 0.16°. From FWHM, by using the equation Eq.(3), coherent length is calculated and it is equal to 50 nm. As thickness is 49 nm, it corresponds with the obtained value. This suggest that single grain is obtained in the direction of the film thickness.

$$C_L = \frac{\lambda K}{FWHM \cdot cos(2\theta)} \qquad \text{Eq.(3)}$$

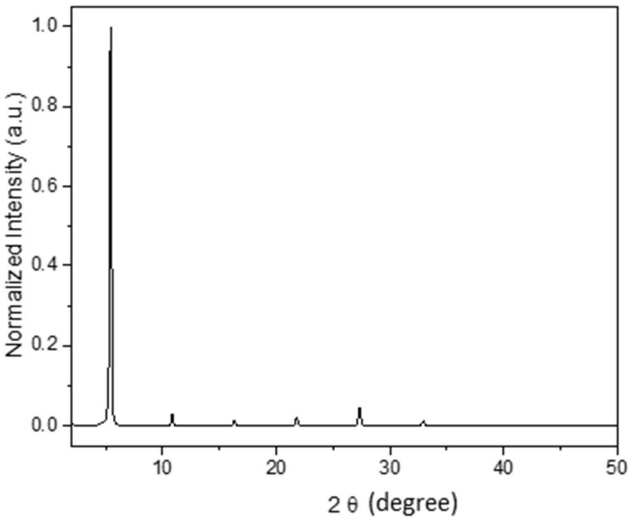

Figure 6. *X-ray diffraction of* $(PEA)_2SnI_4$ *perovskite films.*

3.1.3. UV-VIS-spectroscopy

The perovskite structure can be additionally confirmed by three observed peaks in the absorption spectra located at: 430 nm, 520 nm, 610 nm. The absorption peak located at 430 nm (corresponding to 2.88 eV) is attributed to the high-energy exciton transition energy levels. The absorption peak located at 520 nm (2.38 eV) is assigned to the charge transfer from PEA^+ organic cations to adjacent $(SnI_4)^{2-}$ octahedron layers, whereas the sharp absorption centered at 610 nm (2.03 eV) is attributed to the intrinsic exciton absorption of the tin iodide lattice.

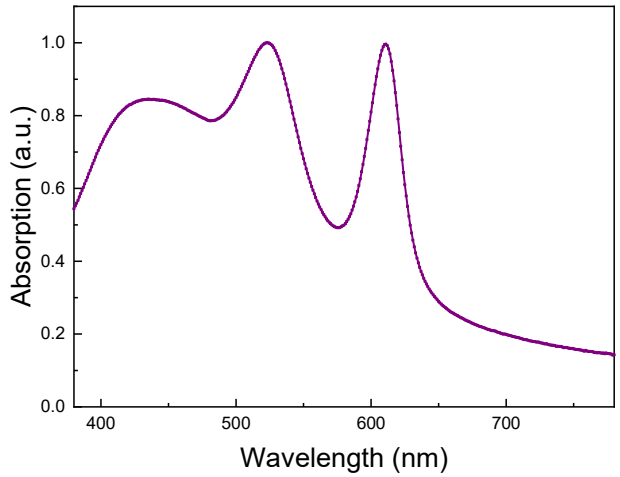

Figure 7. *UV−vis absorption spectra of* $(PEA)_2SnI_4$ *perovskite films.*

The absorption peaks observed in Figure 9 confirm the perovskite phase of $(PEA)_2SnI_4$ perovskite.

3.2. BGTC FET

Transistors based on $(PEA)_2SnI_4$ perovskite has been firstly characterized in commonly used BGTC configuration. As it was mentioned in previous chapter the used architecture has two main drawbacks; first of all, the charge trapping is observed due to the presents of the OH group at dielectric surface, secondly, the environmental stability is very low. Figure 10 shows the comparison of (a) two BGTC devices measured right after fabrication (named as 0s) and (b) two BGTC devices measured after 7 days. The air stability is analyzed by the comparison of mentioned perovskite transistor. Device measured after 7 days shows overall decrease in device performance, including factors of lower field-effect mobility (μ) from average 0.05$cm^2/V{\cdot}s$ to 0.03$cm^2/V{\cdot}s$, smaller on/off current ratio (I_{ON}/I_{OFF}), higher hysteresis compared to the device measured just after fabrication.

The main aim of the project is solve the air stability problem. Changing device structure from BGTC to TGBC makes depositing additional dielectric layer upper the perovskite possible, which can protect the perovskite layer from air, therefore increase stability.

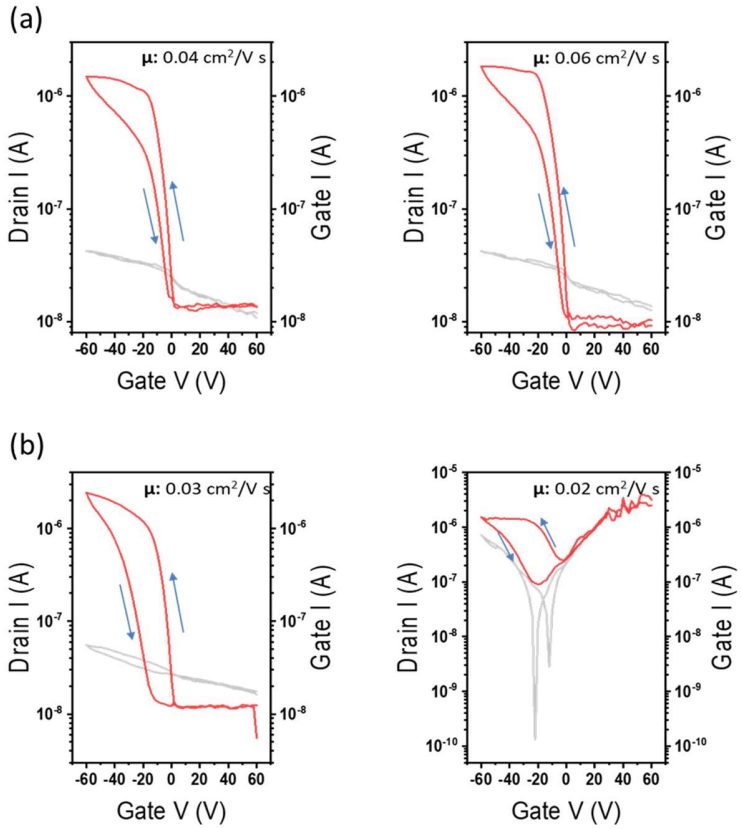

Figure 8. *Device Performance of bottom gate top contact FET. (a) two BGTC devices measured at 0s. (b) two BGTC devices measured after 7 days.*

3.3. Dielectric thickness

Before fabrication of the top gate transistors, the thickness of the dielectric layer needs to be optimized. From this reason, the experimentally compared thickness of polymers with various molecular weight of various polymers is presented in Table 1 and Figure 11. Polymers exhibit hydrophobic nature, forming hydrophobic surface upper perovskite layer, thereby possess ability to protect perovskite layer against humid environment. All the polymers were dissolved in chlorobenzene with the concentration of 30mg/ml except for the PDMS 74kDa, PVDF 275kDa, PEO 400kDa, PE 35kDa and PVPF 29kDa, PVP-*co*-PMMA 220kDa, which didn't dissolve in the solution.

Polymers	PMMA						PS						PMS	PTBS
MW (kDa)	15	77	97	110	350	996	35	190	192	280	350	500	72	75
Thickness (nm)	90	95	115	110	210	160	210	205	250	180	225	250	135	140

Table 1. *Comparison of thickness of polymer dielectric layer.*

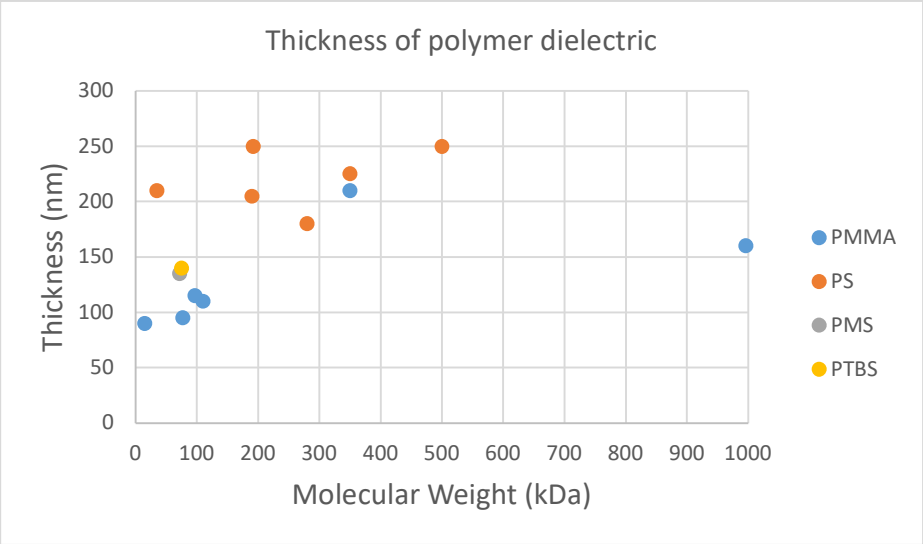

Figure 9. *Comparison of thickness of polymer dielectric layer in graph.*

By the result, thickness tends to increase as the molecular weight of polymer increases. Thicknesses are concentrated around 100-250 nm.

3.4. TGBC FET

3.4.1. PMMA FET with different concentration

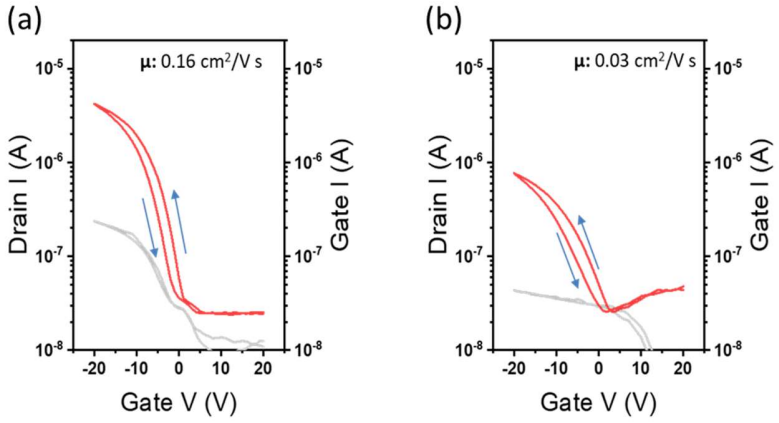

Figure 10. *Device transfer characteristics of PMMA top gate bottom contact FET in different concentration. (a) 30mg/ml and (b) 60mg/ml.*

In order to determine the optimum dielectric thickness for TGBC perovskite FET, result of device transfer characteristics of different concentration of PMMA were obtained. When compared, 30mg/ml PMMA TGBC showed better performance to 60mg/ml PMMA TGBC. Device of 30mg/ml concentration shows higher field-effect mobility (μ) of 0.16 $cm^2/V \cdot s$, 5 times higher when compared to the device of 60mg/ml concentration as presented in Figure 12. Also, larger on/off current ratio (ION/IOFF) of around 170 is observed, which is 30 in device of 60mg/ml concentration. Lower hysteresis, smaller subthreshold swing (SS) observed in device of 30mg/ml concentration.

As a result, 30 mg/ml with around 200 nm is determined as the optimum dielectric thickness. PMMA 350kDa and PS 350kDa were selected for next step as they have thickness around 200 nm, which is shown in Table 1.

3.4.2. FET in different polymer dielectric

When compared, TGBC perovskite FET with PMMA show better performance compared to TGBC perovskite FET with PS. Device with PMMA shows higher field-effect mobility (μ) of 0.2 $cm^2/V \cdot s$ compared to the device with PS as indicated in Figure 13, which shows value of 0.02$cm^2/V \cdot s$. Device with PMMA also indicates larger on/off current ratio (ION/IOFF) of around 150, which is only 20 in device with PS. Lower hysteresis and smaller subthreshold swing (SS) is observed in PMMA, which indicates better performance of the device. As depositing PMMA dielectric layer remove effect of charge trapping compared to BGTC perovskite FET, at which surface hydroxyl

groups cause charge trapping, TGBC perovskite with dielectric layer show better transfer characteristics.

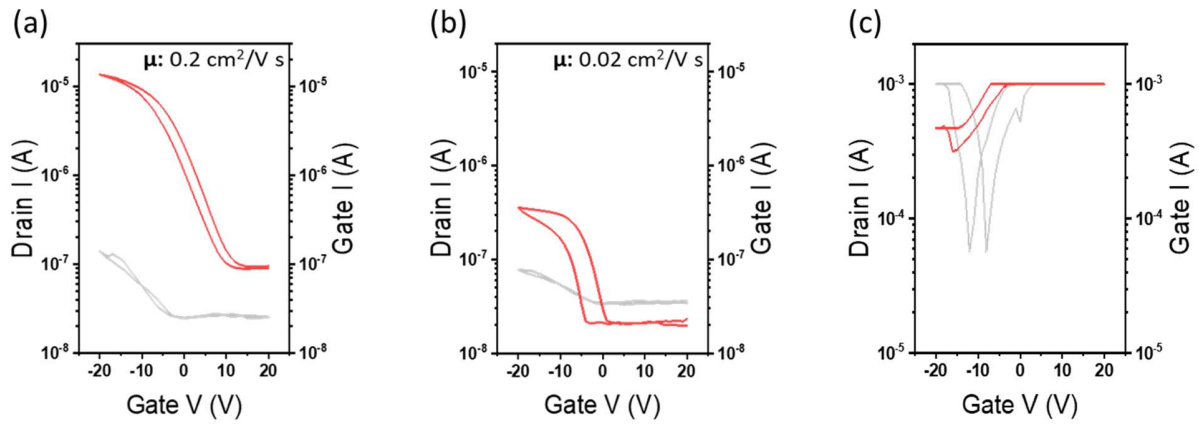

Figure 11. *Device Performance of top gate bottom contact FET in different polymer dielectric. (a) PMMA TGBC FET, (b) PS TGBC FET and (c) PDMS TGBC FET.*

Additionally, PDMS TGBC FET was tested to be compared, but the device didn't work. When analyzing the morphology of the device, it is found out that PDMS cannot form stable uniform layer on perovskite layer. As chloroform, used as solvent to dissolve PDMS has hydrophobic nature, it is difficult to crate uniform layer on hydrophilic perovskite layer.

3.4.3. Environmental stability - light dependence

As TGBC perovskite FET with PMMA showed better performance to TGBC perovskite FET with PS, it was selected for further approach. To check the time dependence of TGBC perovskite FET with PMMA, device was measured right after fabrication, after 1 hour of the first measurement, and after 5 days in the glove box. For BGTC configuration, even small amount of oxygen (ppm level in glove box) influence the device performance.

As passage of time, device showed some overall performance decrease after 1 hour, but there was no significant performance change when measured after 5 days. Device showed lower field-effect mobility (μ) from 0.29cm^2/V·s to 0.17cm^2/V·s, but stayed 0.17cm^2/V·s after 5 days. On/off current ratio (I_{ON}/I_{OFF}) stayed 27 regardless of time. Higher hysteresis and larger subthreshold swing (SS) were shown after 1 hour, but no noticeable change observed in device measured after 5 days. The TGBC perovskite FET with PMMA dielectric layer have better stability compared to the BGTC perovskite FET in Figure 10.

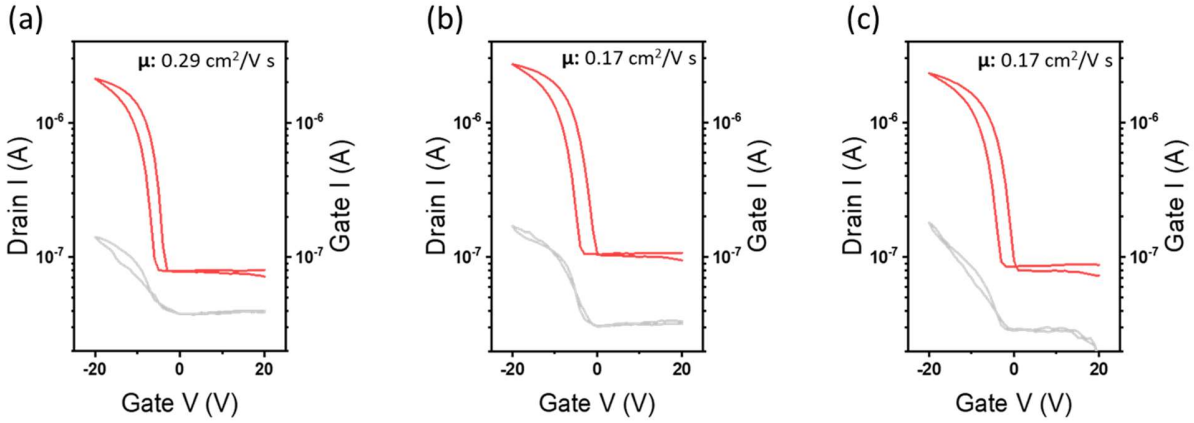

Figure 12. *Device performance of PMMA top gate bottom contact FET in time difference measured with light. (a) device measured at 0s. (b) device measured after 1 hour. (c) device measured after 5 days.*

Time dependence of device is also checked in condition without light to check light dependence in measurement. Compared to the device performance with the condition of light, the device performance measured without light showed even better performance in passage of time. Field-effect mobility (μ) slightly dropped from 0.32cm^2/V·s to 0.3 cm^2/V·s to 0.26 cm^2/V·s. On/off current ratio (I_{ON}/I_{OFF}) changed from 59 to 63 to 67, which is rather increased value as time passed. No noticeable change in hysteresis, and subthreshold swing (SS) was found as shown in Figure 15. This result, measured without light shows more stable and better performance compared to the BGTC perovskite FET in Figure 10.

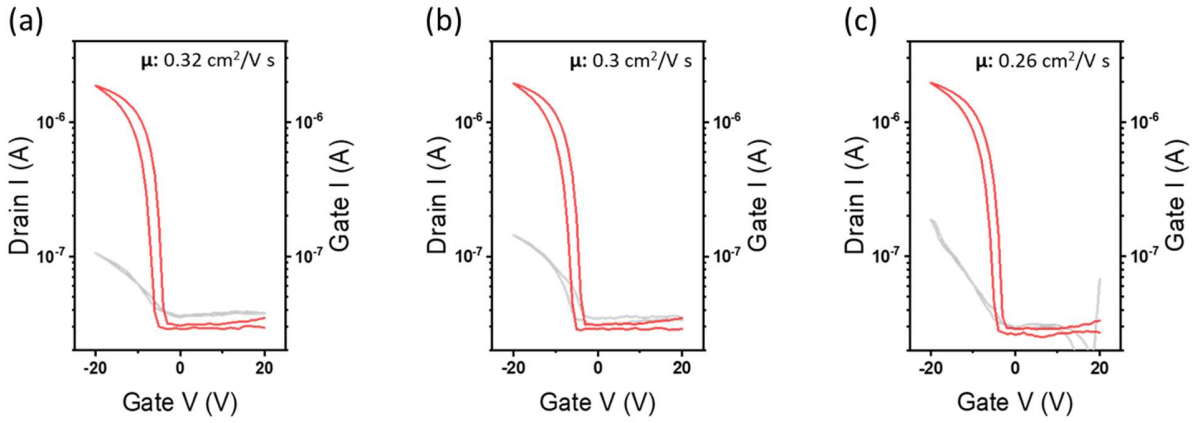

Figure 13. *Device Performance of PMMA top gate bottom contact FET in time difference measured without light. (a) device measured at 0s. (b) device measured after 1 hour. (c) device measured after 5 days.*

When comparing Figure 14 and Figure 15, TGBC perovskite FET with PMMA dielectric layer measured in dark condition show better performance in field-effect mobility, on/off current ratio (I_{ON}/I_{OFF}), and hysteresis compared to light condition. Field-effect mobility value of dark condition decreased about 20% from 0.32$cm^2/V{\cdot}s$ to 0.26 $cm^2/V{\cdot}s$, which is smaller compared to light condition, which decreased about 40% from 0.29$cm^2/V{\cdot}s$ to 0.17 $cm^2/V{\cdot}s$. Also, each value of mobility showed higher. Threshold voltage shifted to left, on/off current ratio increased average 27 to 63, and smaller subthreshold swing. In addition, higher off current was observed compared to the light condition.

The difference of device performance between device measured with light and device measured without light is caused by specific optoelectronic property of perovskite. It can be concluded that perovskite measurement should be done without light because when with light, light affects the device more than gate itself.

4. Conclusions

This study implemented a method for improving 2D lead free Sn-based perovskite FET using different polymer dielectrics. BGTC Sn-based perovskite FET have been fabricated, and showed significant decrease in device performance as time goes by, which indicates device instability in air. By changing the transistor configuration from BGTC to TGBC, the stability and device performance increased through encapsulation effect of polymer dielectric layer on the perovskite layer. Optimum dielectric, 30mg/ml PMMA was identified through comparison of various polymer dielectric thickness through profilometer and further device performance analysis. By comparing device performance changes in transfer characterization of BGTC perovskite FET and TGBC perovskite FET with PMMA over time, it is found that the device parameters such as mobility, threshold voltage, subthreshold swing and hysteresis are significantly improved in devices with TGBC perovskite FET with PMMA. By measurement of device with different light condition, it was found that light affects the device more than gate does, which can be explained by the optoelectronic property of perovskite. Light-dependent property of perovskite device have been checked.

As a result, PMMA dielectric layer used in TGBC device configuration have ability to protect perovskite layer from air, increasing stability and device performance. It is expected that studies which increase device performance and stability of Sn-base perovskite FET in air condition will continue to be performed and make commercialization with great efficiency possible.

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