NANO LETTERS

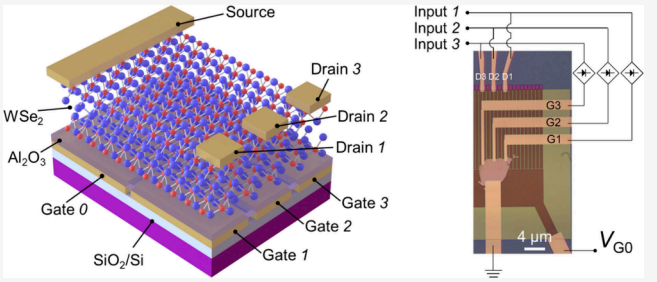
pubs.acs.org/NanoLett
Letter

Parallel Logic Operations in Electrically Tunable Two-Dimensional Homojunctions

Yuliang Chen,* Zhong Wang, Chongwen Zou, and Stuart S. P. Parkin*

Cite This: *Nano Lett.* 2024, 24, 14420−14426

ABSTRACT: Two-dimensional materials show great potential for future electronics beyond silicon materials. Here, we report an exotic multiple-port device based on multiple electrically tunable planar p−n homojunctions formed in a two-dimensional (2D) ambipolar semiconductor, tungsten diselenide (WSe_2). In this device, we prepare multiple gates consisting of a global gate and several local gates, by which electrostatically induced holes and electrons are simultaneously accumulated in a WSe_2 channel, and furthermore, at the boundaries, p−n junctions are formed as directly visualized by Kelvin probe force microscopy. Therefore, in addition to the gate voltages in our device, the drain/source bias can also be used to switch the 2D WSe_2 channel on/off due to the rectification effect of the formed p−n junctions. More importantly, when the voltage on the global gate electrode is altered, all p−n junctions are affected, which makes it possible to perform parallel logic operations.

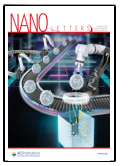


KEYWORDS: *2D semiconductor, logic device, p−n junction, encryption, parallel logic operation*

Silicon-based metal−oxide−semiconductor field-effect transistors (MOSFETs) are the basic electronic components of today's logic circuits. Continually shrinking their size over the past 4 decades has led to dramatically increased performance.[1,2] However, the further shrinkage in the size of these silicon-based transistors has met their physical limits. Hence, the development of electronic chips based on novel materials and technologies has become of high importance.[3−6] 2D materials, stacked layer by layer via van der Waals forces, have attracted considerable attention owing to their remarkable physical properties[7] and are considered to be one of the most promising candidates for next-generation electronics.[8] In particular, transition metal dichalcogenides (TMDs) that display semiconducting properties are an ideal platform for 2D nanoelectronics.[9,10] Nanodevices based on TMD homo- and heterojunctions, which have been fabricated by transfer techniques[11−13] and direct growth,[14,15] are prospective candidates for random access memories, logic elements, and neuromorphic devices and circuits.[16−27] Electrically tunable homojunctions (ETH) with ambipolar TMD channels show highly interesting field-effect characteristics,[28−31] in which holes and electrons are independently electrostatically doped into a 2D channel by two gates, resulting in a p−n homojunction at the boundary. In ETH devices, not only the gates but also the drain/source bias are knobs to switch the 2D channel on/off due to the rectification effect of the p−n junction, and these novel physical principles at the component level allow for advanced logic circuits. To this end, various logic gates have been built by cascading multiple ETH devices.[32,33] Although ETH devices can, in principle, carry out similar functions as MOSFET-based logic circuits, the integration of ETH devices faces challenges in complicated cascading designs and preconfigurations owing to limited ports per device because usually only one p−n junction is formed in a single ETH device.[20,23,25,32−37]

Here, we report a novel multiple-port ETH device for parallel logic operations using WSe_2, an ambipolar TMD, as the channel material. As distinct from previous ETH devices with two input ports due to one p−n junction,[18−20,23,25,33,35,36] our multiple-port devices possess several p−n junctions in a single ETH device resulting from a unique multiple-gate design consisting of a global gate and multiple local gates. These p−n junctions can be dynamically formed and/or erased by independently tuning each gate voltage, which has been directly visualized by Kelvin probe force microscopy (KPFM). Furthermore, when the voltage on the global gate electrode is altered, all p−n junctions are affected. Accordingly, parallel logic operations are anticipated using our unique multiple-port ETH device. Indeed, in experiments, we demonstrate that multiple inputs can be exerted simultaneously in logic

Received: September 4, 2024
Revised: October 23, 2024
Accepted: October 24, 2024
Published: October 30, 2024



https://doi.org/10.1021/acs.nanolett.4c04337
Nano Lett. 2024, 24, 14420−14426

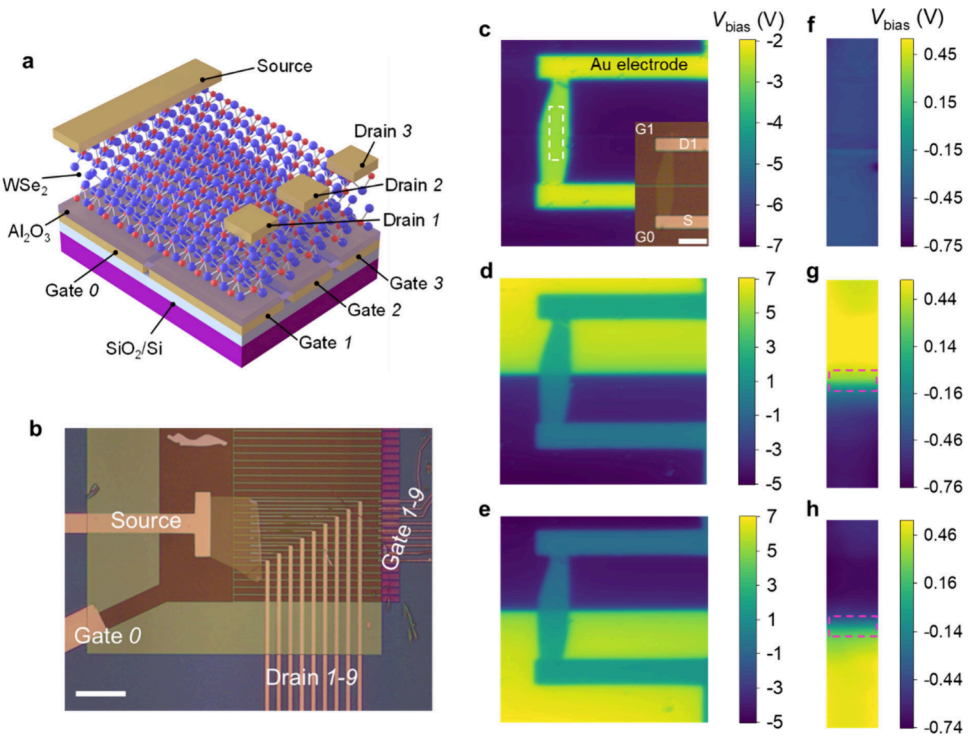


Figure 1. Structure of the ETH device and KPFM results. (a) Schematic illustration of a multiple-port ETH device with a WSe_2 bilayer channel. Red and blue balls represent W and Se, respectively. (b) Optical image of a 10-gate ETH device. Scale bar: 10 μm. (c–e) KPFM results from device 1 (shown in the optical micrograph in the inset of panel c (scale bar: 4 μm)) for different gate voltages. $V_{G0} = V_{G1} = -8$ V (c), $V_{G0} = -8$ V and $V_{G1} = 8$ V (d), $V_{G0} = 8$ *V* and $V_{G1} = -8$ V (e). (f–h) Extracted data from (c–e) as indicated by the white dashed box of area 1.25 μm × 5 μm in (c) are replotted in (f–h), respectively. We use V_{bias} of the Au electrodes as a reference for processing the experimental data.The pink dashed boxes in (g, h) mark the p–n junctions.

operations in one multiple-port ETH device and can be extended to practical applications such as information encryption. In addition, symmetric and asymmetric encryptions based on logic operations are implemented in a confidential communication route integrated with two multiple-port ETH devices. Our studies have not only realized the direct observation of electrically tunable 2D p–n junctions but also demonstrated a practical and scalable 2D unit for multiple-terminal logic computation, which shows unique advantages for future integration circuit fabrication.

Structure and KPFM Characterization. A schematic diagram of the multiple-port WSe_2 ETH device is shown in Figure 1a. Multiple split gate electrodes are designed with one global gate (G0) and several local gates (G1, G2, and G3) in parallel with one another (see details in Figure S1a; note that previous ETH devices only have two gates,[28−30] e.g., Figure S1c,d and the inset of Figure 1c). The separation between the global gate and the local gates is ∼230 nm (see scanning electron microscope (SEM) image in Figure S1b). An Al_2O_3 dielectric layer is deposited to cap all gate electrodes, and then a few-layered WSe_2 flake as the channel is transferred on top of the Al_2O_3 layer. Finally, one source electrode (S) and multiple drain electrodes (D1, D2, and D3) are fabricated on the WSe_2 flake at the positions defined by the corresponding bottom gates. Figure 1b shows an optical image of a 10-gate device formed with a WSe_2 bilayer (∼1.4 nm) flake.

When a voltage is applied between the gates and the source, electrostatic doping takes place. We visualize the accumulated holes or electrons in the WSe_2 channel by KPFM, which examines the local variation of the surface potential with high resolution. The potential difference between the KPFM tip and the sample causes the tip to mechanically oscillate which is compensated by applying a DC bias voltage (V_{bias}) whose magnitude is related to the work function of the sample.[38−40] When electrons accumulate in the WSe_2 channel, empty band states are occupied, which thereby reduces the work function and otherwise increases when holes accumulate.

To facilitate the KPFM tests, we measured the formation of a single junction between one local gate and the global gate. Hence, we used a 2-gate WSe_2 bilayer device as previous 2-port ETH devices[28−31] with one global gate G0 and one local gate G1 (device 1, inset of Figure 1c and Figure S1c,d). During the tests, the S and D1 terminals on the WSe_2 channel were shorted and grounded. We first consider symmetric configurations; i.e., the same gate voltages are applied to G0 and G1. In Figure 1c,f, when −8 V was applied to G0 and G1, the results showed that no junction was produced, but, rather, significant hole accumulation occurred in the entire WSe_2 channel because V_{bias} was lowered by 0.5 V compared to that of the Au electrodes (Figure S2p). The work function of intrinsic WSe_2 is 4.3 eV, and Au has a 5.1 eV work function.[41] If there is no hole doping, WSe_2 should have a higher V_{bias} than that of Au, which was also confirmed via a test at $V_{G0} = V_{G1} = 0$ V (Figure S2d,h). Additional KPFM results from symmetric configurations of G0 and G1 show that not only the doped charge types can be switched between hole and electron by switching the polarities of gating voltages but also the amount of charges accommodated in the WSe_2 channel can be successively adjusted by tuning the magnitude of the gating voltages (Figures S2 and S3). Notably, the offset of V_{bias} between $V_{G0} = V_{G1} = 8$ V and $V_{G0} = V_{G1} = -8$ V is up to 1.2 eV, which is consistent with the 1.3 eV bandgap of WSe_2 as in

https://doi.org/10.1021/acs.nanolett.4c04337
Nano Lett. 2024, 24, 14420−14426

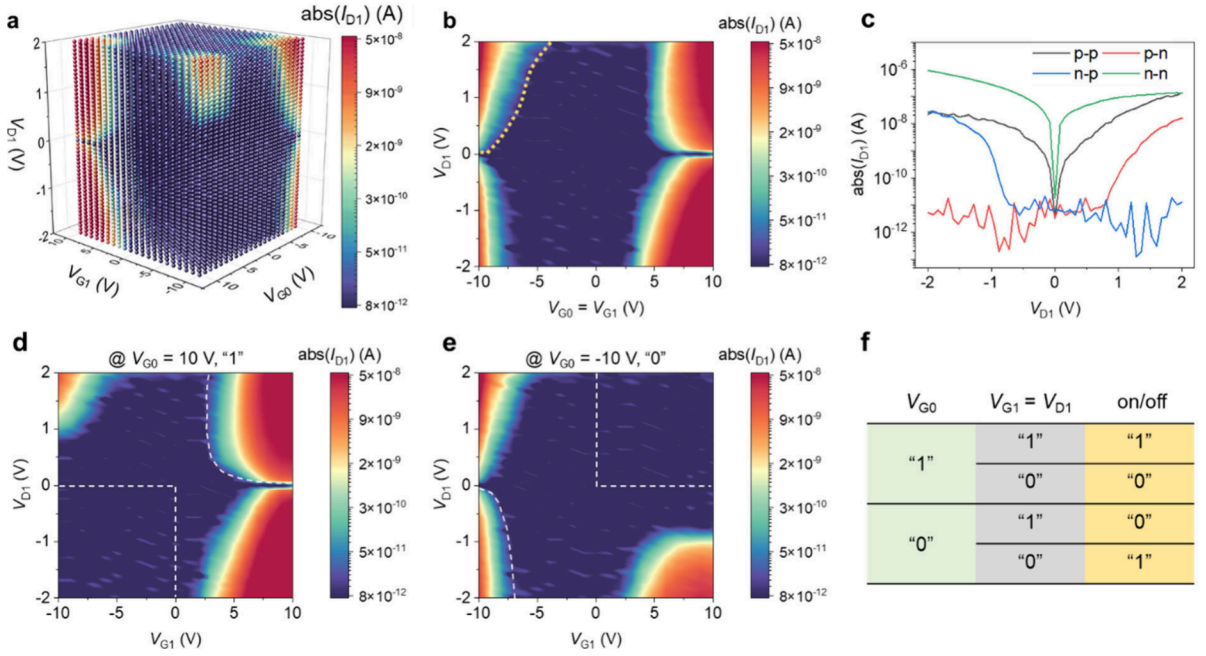


Figure 2. Electrical measurements and logic principles for ETH devices. (a) A set of electrical results from device 1. (b) Diagonal plane of (a) (V_{G0} = V_{G1}). (c) Four vertical edges of (a), indicating reconfigurable rectifications. "n" and "p" indicate electron and hole doping in the two regions of the WSe_2 channel, respectively. (d–f) Extracting the logic rules. Front surface (d) of (a) (V_{G0} = 10 V in logic state "1") and back surface (e) of (a) (V_{G0} = −10 V in logic state "0") suggest that the logic states carried by a pair of drain/gate can be dynamically converted by V_{G0}. The logic rules are concluded in (f). The dashed lines in the first and third quadrants of (d, e) are for highlighting the available regions for logic rules. The yellow dots in (b) give an example for defining the thresholds, which can also work in (d, e).

previous reports,[41,42] which means that electrostatic doping can shift the Fermi level (E_F) into the valence band or the conduction band across the whole bandgap. Accordingly, the KPFM results strongly suggest that our device is anticipated to become an ambipolar FET by means of symmetric configurations of the gate voltages.[9,43]

Furthermore, different voltages, i.e., asymmetric configurations, can also be applied to G1 and G0. KPFM demonstrated that different polarities of V_{G0} and V_{G1} allow for holes and electrons to be simultaneously accumulated in distinct WSe_2 segments. In Figure 1d,g, where V_{G1} = −V_{G0} = 8 V, electrons (holes) were accumulated in the top (bottom) half segment because of the positive (negative) voltage on G1 (G0). Swapping the polarities of the gate voltages results in opposite charge accumulations (Figure 1e,h). Since holes and electrons are accumulated in different portions of the WSe_2 channel, a p−n homojunction is formed at their boundary. A depletion region ∼600 nm in width was visualized in the form of a successive evolution of V_{bias} along the WSe_2 channel (pink dashed boxes in Figure 1g,h and Figure S4). We also tested another device (device 2), showing KPFM results similar to those of device 1 (Figure S5). Note that here we used one local gate with the global gate G0 to produce one junction, but if more local gates are used, more junctions can be produced, for example, a 10-gate device can form 9 junctions as shown in Figure 1b. However, subjected to the limited capacity of our KPFM device, we did not measure this device.

Electrical Measurements and Physical Principles for Logic Operations. The KPFM results show that the p−n homojunction in the ETH device can be dynamically formed/erased if the gate voltages are switched between the symmetric and asymmetric configurations. In the following, we performed electrical measurements on device 1 based on its KPFM results. In the symmetric (asymmetric) configurations of gate voltages, we predict that the conductive states of the channel are independent (dependent) of the polarity of readout bias applied between the source and drain electrodes due to only one (two) type(s) of charges that are doped in the WSe_2 channel. To check these conjectures, V_{G0} and V_{G1} were independently varied from −10 to 10 V in steps of 1 V, for a total of 441 configurations. At each configuration, V_{D1} was swept from −2 to 2 V in steps of 0.04 V, and the current I_{D1} was recorded. The source electrode was grounded. The test results are shown as a 4-dimensional data cube in Figure 2a, in which the color represents the absolute value of I_{D1}. Figure S6a shows the back view of the data cube.

First, we check the symmetric configurations of gate voltages by chopping through the data cube to expose the diagonal plane of V_{G0} = V_{G1} (Figure 2b), which confirm that both hole and electron doping can make the WSe_2 channel conductive (ambipolar FET) irrespective of the polarities of V_{D1} when the gate voltages exceed certain thresholds (yellow dots, see the caption of Figure 2). The extracted transfer characteristic curve from Figure 2b at a fixed V_{D1} of 1.04 V shows that the on/off ratio is $>10^3$ for p-channel (holes accumulated) and $>10^4$ for n-channel (electrons accumulated) (see Figure S6b), which indicates this ETH device has a high quality. We also notice that the leakage currents of I_{G0} and I_{G1} are always below $\sim10^{-10}$ A level in all tests (Figure S6c). Then, we check the asymmetric scenario. Figure 2d is the front plane of the data cube, where V_{G0} is fixed at 10 V. It is observed that when V_{G1} is positive and exceeds certain thresholds, the WSe_2 channel can be turned on regardless of the polarities of V_{D1}. It should be noted that in this case V_{G0} and V_{G1} have the same polarity but different amplitudes that are distinct from the symmetric configuration where V_{G0} = V_{G1}. Nevertheless, when V_{G1} is

https://doi.org/10.1021/acs.nanolett.4c04337
Nano Lett. 2024, 24, 14420−14426

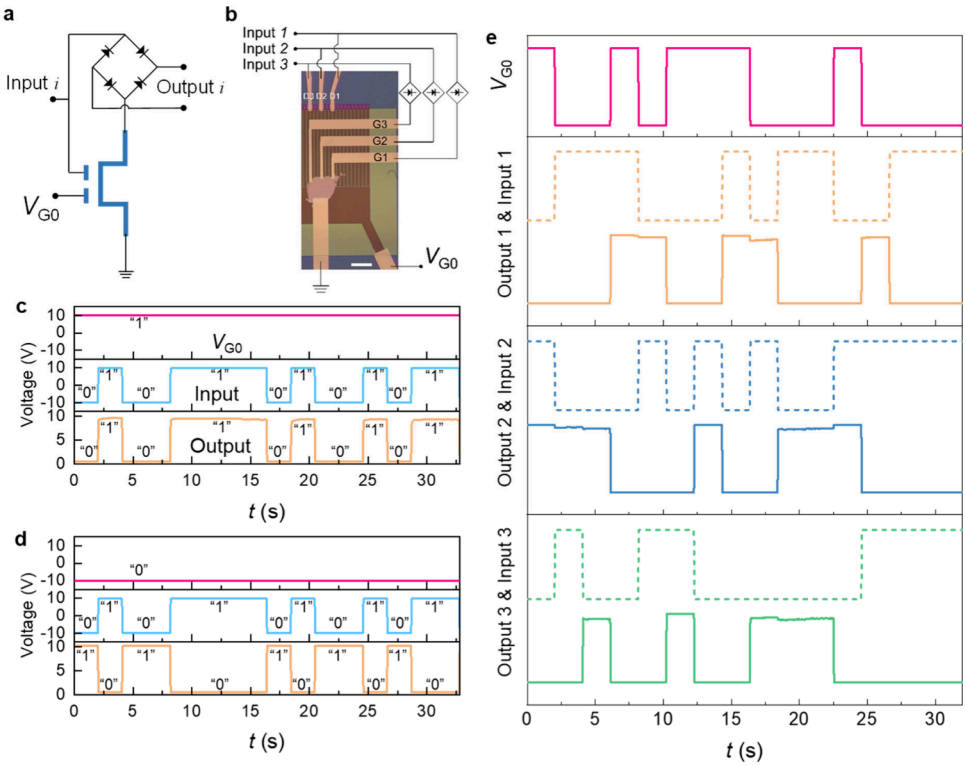


Figure 3. Implementing logic operations and encryption using ETH devices. (a) A circuit diagram. (b) A circuit integrated with a 3-input ETH device for implementing encryption. Scale bar: 4 μm. (c) Demonstration of plain code by setting V_{G0} = 10 V as the secret key. (d) To invert the input by setting V_{G0} = −10 V as the secret key. (e) Applying a random voltage sequence for V_{G0} as the secret key to encrypt 3 inputs in parallel. Dashed lines and solid lines indicate the inputs and outputs, respectively.

lower than −5 V, only positive V_{D1} up to a threshold can turn the WSe_2 channel on. The counterpart of fixing V_{G0} at −10 V also shows similar results apart from a negative V_{D1}, making the WSe_2 channel conductive (Figure 2e).

We further highlight this observation by extracting the four vertical edges of the data cube (Figure 2c and linear scale plot in Figure S6d), in which the magnitudes of V_{G0} and V_{G1} are maintained at 10 V. When 10 and −10 V are applied to V_{G0} and V_{G1} (red curve), respectively, a rectification effect is observed, i.e., a diode. When V_{G0} and V_{G1} are swapped, the direction of rectification is also swapped (blue curve). In contrast, no rectification appears for the same polarity applied to G0 and G1 (black and green curves). The rectification effects are ascribed to the formation of a p−n junction when V_{G0} and V_{G1} are set with different polarities. For instance, the red curve is related to Figure 1e,h, where the drain electrode contacts the top WSe_2 segment, where holes are accumulated (p-channel); the WSe_2 bottom segment is the location where electrons are accumulated (n-channel), and thus, by applying a positive V_{D1}, the diode would be forward biased. The same analysis is also suitable for the blue curve. The rectification data are fitted to the Shockley diode equation,[44] giving an ideality factor of $n \sim 2$ for both n−p and p−n I_{D1}−V_{D1} curves, indicating that I_{D1} is mostly limited by recombination rather than diffusion (Supplementary Note 1). In Figure S7, we reproduce the electrical results based on device 3, a 4-gate device with a 9-layer (~6.4 nm) WSe_2 flake (Figure 3b). We note that the electrically tunable rectification effects are still observed when the split distance of the gates even increases to 2.4 μm although the on-state currents are lower compared with the cases with shorter split distances (Figure S8).

In MOSFETs, only the gate voltage switches the channel on/off. By contrast, both electrical measurements and KPFM results unambiguously demonstrated that the drain voltage can also determine the conductive status of the WSe_2 channel, which makes the ETH device a unique logic unit at the component level. Next, we extract the logic rules in our ETH devices. The custom in conventional electronics is obeyed, taking positive voltage as the logic state "1" and negative voltage as the logic state "0"; thereby, e.g., Figure 2d is given with fixing V_{G0} at "1". In the first and third quadrants of Figure 2d, V_{D1} and V_{G1} have the same polarities, resulting in the same logic states. The two areas outlined by the white dashed curves indicate that V_{D1} = V_{G1} = "1" can switch the WSe_2 channel on, whereas V_{D1} = V_{G1} = "0" turns off the channel. Likewise, Figure 2e with fixed V_{G0} = "0" shows the opposite results. Figure 2f concludes the rules by further taking channel "on" as logic "1" and "off" as logic "0", which is a truth table of the XNOR logic gate and reveals that the information input by "V_{D1} = V_{G1}" can be dynamically converted by switching the logic states of V_{G0}.

Note that the KPFM results and electrical measurements are extracted from a single junction in a 2-gate ETH device, but the logic principle is also applicable for every junction of the device having multiple gates, such as the devices in Figures 1b and 3b, where G0 is the global gate used to form each p−n junction in combination with each local gate. The parallel distribution can effectively avoid crosstalk between the local gates (Supplementary Note 2). When the voltage on the global gate is altered, all of the p−n junctions are affected. This attribute gives the multiple-gate ETH devices the capacity for parallel logic operation, by contrast, which would otherwise

https://doi.org/10.1021/acs.nanolett.4c04337
Nano Lett. 2024, 24, 14420−14426

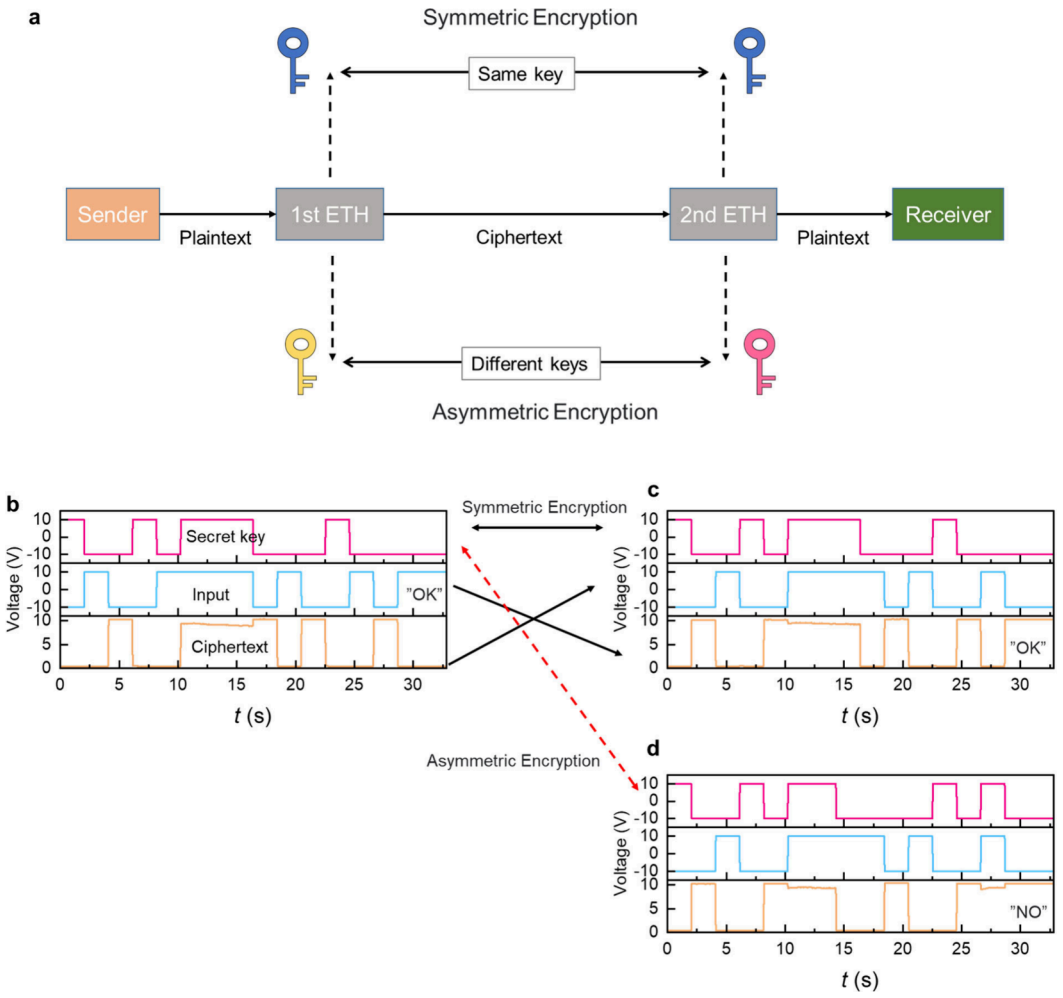


Figure 4. Confidential communication based on two ETH devices. (a) A schematic diagram of confidential communication as well as illustrating symmetric encryption and asymmetric encryption in this data transmission route integrated with two ETH devices. (b–d) Experimental results of confidential communication. (b) is associated with the first ETH device. (c) and (d) are associated with the second ETH device when it works on symmetric encryption and asymmetric encryption, respectively.

require complicated cascades of MOSFETs or 2-gate ETH devices (Supplementary Note 3).[45]

Parallel Logic Operation and Information Encryption. To perform the logic operations indicated by Figure 2f, we designed a compact circuit integrated with our ETH devices; see a circuit diagram in Figure 3a. It is found in Figure 2d,e that V_{D1} and V_{G1} have the same polarity, so two terminals of a rectifier connect a local gate and a drain to realize "$V_{D1} = V_{G1}$" and serve as an input port. V_{G0} serves as the other input port. Rectifiers also play the role of resistive dividers, which can convert the WSe_2 channel on/off states to partial voltages being accessed via the other two terminals as the output. Meanwhile, the rectification effect of rectifiers always makes the output voltages positive. It is important to note that the extra supply voltage (V_{CC}) is avoided in our circuit design, resulting in no static power consumption.

Next, we experimentally demonstrate that our ETH device can achieve the functions shown in Figure 2f. See Figure 3c,d, the experiment results from device 1 with 2 gates, in which the logic operations manifested by Figure 2f are reproduced well. For example, in Figure 3d, we set V_{G0} = "0" (pink line), and the circuit outputs "1" and "0" (brown curve) if "0" and "1" are input into the port of "$V_{D1} = V_{G1}$" (blue curve), respectively. We further consider these logic operations as information encryption processes, as follows.

In Figure 3c, the input was "01001111 01001011" representing the ASCII code of "OK", and then a plain code was output upon fixing V_{G0} = "1". Plain code refers to the output having an identical form as the input despite the output voltage range are different. Note that plain code is widely used in public radio and HTTP. By contrast, in Figure 3d, by fixing V_{G0} = "0", the input was processed using an invert operation to output "10110000 10110100". Intrinsically, setting V_{G0} = "0" or "1" is to configure a secret key, even if the secret keys in Figures 3c and 3d are too simple to protect the encrypted information. In addition, the 16-bit data representing "OK" has to be serially processed one by one because device 1 has only one input port (V_{G0} is used for the secret key), resulting in limited efficiency. A better alternative is to use fluctuating sequences as the secret keys in a multiple-input ETH device.

In Figure 3b, a circuit with a three-input ETH device (device 3 with 4 gates) is established based on the basic circuit shown in Figure 3a. Since device 3 has 3 input ports, 3 bits can be processed at the same time. Moreover, G0 is a global gate; therefore, the secret key loaded on it can be used to encrypt all inputs. In Figure 3e, a random sequence (pink curve) generated by a stochastic algorithm is loaded onto the global

https://doi.org/10.1021/acs.nanolett.4c04337
Nano Lett. 2024, 24, 14420−14426

G0 terminal to process 3 input data flows in parallel (dashed lines). This secret key applies to randomly selected input bits invert or plain operations, which output unreadable ciphertexts (solid lines). It can be found that every input can independently exert logic operations with the input from the G0 terminal, showcasing no noteworthy crosstalk among the inputs. Thus, in principle, adding more input terminals is feasible to enhance the encryption capacity of ETH devices. For example, Figure 1b shows a 9-input ETH device and a byte can be encrypted simultaneously (note that we did not test this device because of the limited capacity of our measurement system). It should be emphasized that the logic operations (plain and invert) in our ETH devices are simple but nevertheless do not mean encryptions are not secure because the determining factor of security is the algorithms used to generate the secret keys.[46]

On the contrary, thanks to the simple logic operations, the ETH devices can further become a decryptor. Figure 4a shows a confidential communication route integrated with two ETH devices. The ciphertext generated by the first ETH device can be translated by the second ETH device. We applied two different encryption strategies in this route, i.e., symmetric and asymmetric encryptions, which are widely used in daily life. Specifically, by configuring the same (different) secret key in the second ETH device as that in the first ETH device, symmetric (asymmetric) encryption can be established. Figure 4b,c experimentally demonstrates symmetric encryption. Supposing the sender wanted to transmit "OK" to the receiver (Figure 4b), a random voltage sequence (pink curve) was configured on G0 of the first ETH device as the secret key, and the ASCII code representing "OK" (blue curve) was input. Then, the ciphertext (brown curve) would be generated and transmitted. Even if the ciphertext was eavesdropped during the transmission, the cheater cannot get the right information without the right secret key. Subsequently, in Figure 4c, the ciphertext was sent into the second ETH device as the inputs before arriving at the receiver, and then by configuring the same secret key as in the first ETH device, the ciphertext was translated as "OK". Thus, a confidential communication was completed. Analogously, in Figure 4d, a different secret key was used in the second ETH device (asymmetric encryption), showing more diversified results. Note that our ETH devices are physical. Compared with software encryptors, physical ones are more secure and efficient.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.4c04337.

Experimental section, additional KPFM results and electrical transport data, and supplementary notes (PDF)

■ AUTHOR INFORMATION

Corresponding Authors

Yuliang Chen − *Max Planck Institute of Microstructure Physics, 06120 Halle, Germany;* orcid.org/0000-0002-1197-5028; Email: yuliang.chen@mpi-halle.mpg.de

Stuart S. P. Parkin − *Max Planck Institute of Microstructure Physics, 06120 Halle, Germany;* orcid.org/0000-0003-4702-6139; Email: stuart.parkin@mpi-halle.mpg.de

Authors

Zhong Wang − *Max Planck Institute of Microstructure Physics, 06120 Halle, Germany;* orcid.org/0000-0001-9263-9781

Chongwen Zou − *National Synchrotron Radiation Laboratory, School of Nuclear Science and Technology, University of Science and Technology of China, 230029 Hefei, China;* orcid.org/0000-0002-6153-081X

Complete contact information is available at: https://pubs.acs.org/10.1021/acs.nanolett.4c04337

Funding

Open access funded by Max Planck Society.

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

We acknowledge funding from the Deutsche Forschungsgemeinschaft (DFG, German Research Foundation), project no. 443406107, Priority Programme (SPP) 2244, the European Union (FUNLAYERS, project no. 101079184) and the National Natural Science Foundation of China (project no. 12235015). Y.C. thanks Wenjie Zhang for assistance with device fabrication, Tianping Ma for schematic illustration, Steven Zhang for comments and language polishing, and support of WSe_2 crystal growth from Daniel Rhodes.

■ REFERENCES

(1) Hu, C. (Invited) FinFET and UTB–How to Make Very Short Channel MOSFETs. *ECS Trans.* **2013**, *50* (9), 17−20.

(2) Ferain, I.; Colinge, C. A.; Colinge, J. P. Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors. *Nature* **2011**, *479* (7373), 310−6.

(3) Hao, Z.; Yan, Y.; Shi, Y.; Li, Y. Emerging Logic Devices beyond CMOS. *J. Phys. Chem. Lett.* **2022**, *13* (8), 1914−1924.

(4) Liu, Y.; Duan, X.; Shin, H. J.; Park, S.; Huang, Y.; Duan, X. Promises and prospects of two-dimensional transistors. *Nature* **2021**, *591* (7848), 43−53.

(5) Wu, F.; Tian, H.; Shen, Y.; Hou, Z.; Ren, J.; Gou, G.; Sun, Y.; Yang, Y.; Ren, T. L. Vertical MoS2 transistors with sub-1-nm gate lengths. *Nature* **2022**, *603* (7900), 259−264.

(6) Waldrop, M. M. The chips are down for Moore's law. *Nature* **2016**, *530* (7589), 144−7.

(7) Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Zhang, Y.; Dubonos, S. V.; Grigorieva, I. V.; Firsov, A. A. Electric field effect in atomically thin carbon films. *Science* **2004**, *306* (5696), 666−9.

(8) Akinwande, D.; Huyghebaert, C.; Wang, C. H.; Serna, M. I.; Goossens, S.; Li, L. J.; Wong, H. P.; Koppens, F. H. L. Graphene and two-dimensional materials for silicon technology. *Nature* **2019**, *573* (7775), 507−518.

(9) Hu, W.; Sheng, Z.; Hou, X.; Chen, H.; Zhang, Z.; Zhang, D. W.; Zhou, P. Ambipolar 2D Semiconductors and Emerging Device Applications. *Small Methods* **2021**, *5* (1), No. e2000837.

(10) Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-layer MoS2 transistors. *Nat. Nanotechnol.* **2011**, *6* (3), 147−50.

(11) Castellanos-Gomez, A.; Buscema, M.; Molenaar, R.; Singh, V.; Janssen, L.; van der Zant, H. S. J.; Steele, G. A. Deterministic transfer of two-dimensional materials by all-dry viscoelastic stamping. *2D Materials* **2014**, *1* (1), No. 011002.

(12) Wang, L.; Meric, I.; Huang, P. Y.; Gao, Q.; Gao, Y.; Tran, H.; Taniguchi, T.; Watanabe, K.; Campos, L. M.; Muller, D. A.; Guo, J.; Kim, P.; Hone, J.; Shepard, K. L.; Dean, C. R. One-dimensional electrical contact to a two-dimensional material. *Science* **2013**, *342* (6158), 614−7.

(13) Zomer, P. J.; Guimarães, M. H. D.; Brant, J. C.; Tombros, N.; van Wees, B. J. Fast pick up technique for high quality heterostructures of bilayer graphene and hexagonal boron nitride. *Appl. Phys. Lett.* **2014**, *105* (1), No. 013101.
(14) Li, H.; Li, Y.; Aljarb, A.; Shi, Y.; Li, L. J. Epitaxial Growth of Two-Dimensional Layered Transition-Metal Dichalcogenides: Growth Mechanism, Controllability, and Scalability. *Chem. Rev.* **2018**, *118* (13), 6134−6150.
(15) Li, J.; Yang, X.; Liu, Y.; Huang, B.; Wu, R.; Zhang, Z.; Zhao, B.; Ma, H.; Dang, W.; Wei, Z.; Wang, K.; Lin, Z.; Yan, X.; Sun, M.; Li, B.; Pan, X.; Luo, J.; Zhang, G.; Liu, Y.; Huang, Y.; Duan, X.; Duan, X. General synthesis of two-dimensional van der Waals heterostructure arrays. *Nature* **2020**, *579* (7799), 368−374.
(16) Chen, H.; Xue, X.; Liu, C.; Fang, J.; Wang, Z.; Wang, J.; Zhang, D. W.; Hu, W.; Zhou, P. Logic gates based on neuristors made from two-dimensional materials. *Nat. Electron.* **2021**, *4* (6), 399−404.
(17) Lee, S.-J.; Lin, Z.; Huang, J.; Choi, C. S.; Chen, P.; Liu, Y.; Guo, J.; Jia, C.; Wang, Y.; Wang, L.; Liao, Q.; Shakir, I.; Duan, X.; Dunn, B.; Zhang, Y.; Huang, Y.; Duan, X. Programmable devices based on reversible solid-state doping of two-dimensional semiconductors with superionic silver iodide. *Nat. Electron.* **2020**, *3* (10), 630−637.
(18) Liu, C.; Yan, X.; Song, X.; Ding, S.; Zhang, D. W.; Zhou, P. A semi-floating gate memory based on van der Waals heterostructures for quasi-non-volatile applications. *Nat. Nanotechnol.* **2018**, *13* (5), 404−410.
(19) Liu, L.; Liu, C.; Jiang, L.; Li, J.; Ding, Y.; Wang, S.; Jiang, Y. G.; Sun, Y. B.; Wang, J.; Chen, S.; Zhang, D. W.; Zhou, P. Ultrafast non-volatile flash memory based on van der Waals heterostructures. *Nat. Nanotechnol.* **2021**, *16* (8), 874−881.
(20) Mennel, L.; Symonowicz, J.; Wachter, S.; Polyushkin, D. K.; Molina-Mendoza, A. J.; Mueller, T. Ultrafast machine vision with 2D material neural network image sensors. *Nature* **2020**, *579* (7797), 62−66.
(21) Frisenda, R.; Molina-Mendoza, A. J.; Mueller, T.; Castellanos-Gomez, A.; van der Zant, H. S. J. Atomically thin p−n junctions based on two-dimensional materials. *Chem. Soc. Rev.* **2018**, *47* (9), 3339−3358.
(22) Wang, F.; Pei, K.; Li, Y.; Li, H.; Zhai, T. 2D Homojunctions for Electronics and Optoelectronics. *Adv. Mater.* **2021**, *33* (15), No. e2005303.
(23) Tong, L.; Peng, Z.; Lin, R.; Li, Z.; Wang, Y.; Huang, X.; Xue, K. H.; Xu, H.; Liu, F.; Xia, H.; Wang, P.; Xu, M.; Xiong, W.; Hu, W.; Xu, J.; Zhang, X.; Ye, L.; Miao, X. 2D materials-based homogeneous transistor-memory architecture for neuromorphic hardware. *Science* **2021**, *373* (6561), 1353−1358.
(24) Polyushkin, D. K.; Wachter, S.; Mennel, L.; Paur, M.; Paliy, M.; Iannaccone, G.; Fiori, G.; Neumaier, D.; Canto, B.; Mueller, T. Analogue two-dimensional semiconductor electronics. *Nat. Electron.* **2020**, *3* (8), 486−491.
(25) Sun, X.; Zhu, C.; Yi, J.; Xiang, L.; Ma, C.; Liu, H.; Zheng, B.; Liu, Y.; You, W.; Zhang, W.; Liang, D.; Shuai, Q.; Zhu, X.; Duan, H.; Liao, L.; Liu, Y.; Li, D.; Pan, A. Reconfigurable logic-in-memory architectures based on a two-dimensional van der Waals heterostructure device. *Nat. Electron.* **2022**, *5* (11), 752−760.
(26) Tsai, M. Y.; Huang, C. T.; Lin, C. Y.; Lee, M. P.; Yang, F. S.; Li, M. J.; Chang, Y. M.; Watanabe, K.; Taniguchi, T.; Ho, C. H.; Wu, W. W.; Yamamoto, M.; Wu, J. L.; Chiu, P. W.; Lin, Y. F. A reconfigurable transistor and memory based on a two-dimensional heterostructure and photoinduced trapping. *Nat. Electron.* **2023**, *6* (10), 755−764.
(27) Peng, R. X.; Wu, Y. H.; Wang, B. L.; Shi, R.; Xu, L. L.; Pan, T.; Guo, J.; Zhao, B. C.; Song, C.; Fan, Z. Y.; Wang, C.; Zhou, P.; Fan, S. S.; Liu, K. Programmable graded doping for reconfigurable molybdenum ditelluride devices. *Nat. Electron.* **2023**, *6* (11), 852−861.
(28) Baugher, B. W.; Churchill, H. O.; Yang, Y.; Jarillo-Herrero, P. Optoelectronic devices based on electrically tunable p-n diodes in a monolayer dichalcogenide. *Nat. Nanotechnol.* **2014**, *9* (4), 262−7.
(29) Pospischil, A.; Furchi, M. M.; Mueller, T. Solar-energy conversion and light emission in an atomic monolayer p-n diode. *Nat. Nanotechnol.* **2014**, *9* (4), 257−61.
(30) Ross, J. S.; Klement, P.; Jones, A. M.; Ghimire, N. J.; Yan, J.; Mandrus, D. G.; Taniguchi, T.; Watanabe, K.; Kitamura, K.; Yao, W.; Cobden, D. H.; Xu, X. Electrically tunable excitonic light-emitting diodes based on monolayer WSe2 p−n junctions. *Nat. Nanotechnol.* **2014**, *9* (4), 268−72.
(31) Li, D.; Chen, M.; Sun, Z.; Yu, P.; Liu, Z.; Ajayan, P. M.; Zhang, Z. Two-dimensional non-volatile programmable p−n junctions. *Nat. Nanotechnol.* **2017**, *12* (9), 901−906.
(32) Resta, G. V.; Balaji, Y.; Lin, D.; Radu, I. P.; Catthoor, F.; Gaillardon, P. E.; De Micheli, G. Doping-Free Complementary Logic Gates Enabled by Two-Dimensional Polarity-Controllable Transistors. *ACS Nano* **2018**, *12* (7), 7039−7047.
(33) Pan, C.; Wang, C.-Y.; Liang, S.-J.; Wang, Y.; Cao, T.; Wang, P.; Wang, C.; Wang, S.; Cheng, B.; Gao, A.; Liu, E.; Watanabe, K.; Taniguchi, T.; Miao, F. Reconfigurable logic and neuromorphic circuits based on electrically tunable two-dimensional homojunctions. *Nat. Electron.* **2020**, *3* (7), 383−390.
(34) Huang, X. H.; Liu, C. S.; Zhou, P. 2D semiconductors for specific electronic applications: from device to system. *npj 2d Materials and Applications* **2022**, *6* (1), 51.
(35) Resta, G. V.; Sutar, S.; Balaji, Y.; Lin, D.; Raghavan, P.; Radu, I.; Catthoor, F.; Thean, A.; Gaillardon, P. E.; de Micheli, G. Polarity control in WSe2 double-gate transistors. *Sci. Rep.* **2016**, *6*, No. 29448.
(36) Wang, H.; Bao, L.; Guzman, R.; Wu, K.; Wang, A.; Liu, L.; Wu, L.; Chen, J.; Huan, Q.; Zhou, W.; Pantelides, S. T.; Gao, H. J. Ultrafast-Programmable 2D Homojunctions Based on van der Waals Heterostructures on a Silicon Substrate. *Adv. Mater.* **2023**, *35* (32), No. e2301067.
(37) Wu, P.; Reis, D.; Hu, X. S.; Appenzeller, J. Two-dimensional transistors with reconfigurable polarities for secure circuits. *Nat. Electron.* **2021**, *4* (1), 45−53.
(38) Utama, M. I. B.; Kleemann, H.; Zhao, W.; Ong, C. S.; da Jornada, F. H.; Qiu, D. Y.; Cai, H.; Li, H.; Kou, R.; Zhao, S.; Wang, S.; Watanabe, K.; Taniguchi, T.; Tongay, S.; Zettl, A.; Louie, S. G.; Wang, F. A dielectric-defined lateral heterojunction in a monolayer semiconductor. *Nat. Electron.* **2019**, *2* (2), 60−65.
(39) Li, L.; Wang, M.; Zhou, Y.; Zhang, Y.; Zhang, F.; Wu, Y.; Wang, Y.; Lyu, Y.; Lu, N.; Wang, G.; Peng, H.; Shen, S.; Du, Y.; Zhu, Z.; Nan, C. W.; Yu, P. Manipulating the insulator-metal transition through tip-induced hydrogenation. *Nat. Mater.* **2022**, *21* (11), 1246−1251.
(40) Bonnell, D. A.; Kalinin, S. V.; Kholkin, A. L.; Gruverman, A. Piezoresponse Force Microscopy: A Window into Electromechanical Behavior at the Nanoscale. *MRS Bull.* **2009**, *34* (9), 648−657.
(41) Smyth, C. M.; Addou, R.; McDonnell, S.; Hinkle, C. L.; Wallace, R. M. WSe2 -contact metal interface chemistry and band alignment under high vacuum and ultra high vacuum deposition conditions. *2D Materials* **2017**, *4* (2), No. 025084.
(42) Zhao, W.; Ghorannevis, Z.; Chu, L.; Toh, M.; Kloc, C.; Tan, P. H.; Eda, G. Evolution of electronic structure in atomically thin sheets of WS2 and WSe2. *ACS Nano* **2013**, *7* (1), 791−7.
(43) Ren, Y.; Yang, X. Y.; Zhou, L.; Mao, J. Y.; Han, S. T.; Zhou, Y. Recent Advances in Ambipolar Transistors for Functional Applications. *Adv. Funct. Mater.* **2019**, *29* (40), No. 1902105.
(44) Banwell, T. C.; Jayakumar, A. Exact analytical solution for current flow through diode with series resistance. *Electron. Lett.* **2000**, *36* (4), 291.
(45) Lin, J.-F.; Hwang, Y.-T.; Sheu, M.-H.; Ho, C.-C. A Novel High-Speed and Energy Efficient 10-Transistor Full Adder Design. *IEEE Transactions on Circuits and Systems I: Regular Papers* **2007**, *54* (5), 1050−1059.
(46) Smart, N. P. *Cryptography: An Introduction*; McGraw-Hill: New York, 2003; Vol. *3*.

https://doi.org/10.1021/acs.nanolett.4c04337
Nano Lett. 2024, 24, 14420−14426