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Breadboard model of the LISA phasemeter

O. Gerberding¹, S. Barke¹, I. Bykov¹, K. Danzmann¹, A. Enggaard², J.J. Esteban¹, A. Gianolio³, T.V. Hansen², G. Heinzel¹, A. Hornstrup⁴, O. Jennrich³, J. Kullmann¹, S.M. Pedersen⁴, T. Rasmussen², J. Reiche¹, Z. Sodnik³ and M. Suess³

1 Max-Planck Institute for Gravitational Physics (Albert Einstein Institute) and Institute for Gravitational Physics, Leibniz University Hannover, Callinstrasse 38, 30167 Hannover, Germany

2 Axcon ApS, Diplomvej 381, DK-2800 Kgs. Lyngby, Denmark

3 European Space Research and Technology Centre, European Space Agency, Keplerlaan 1, 2200 AG Noordwijk, The Netherlands

4 DTU Space, National Space Institute, The Technical University of Denmark, Elektrovej 327, DK-2800 Kgs. Lyngby, Denmark

Abstract. An elegant breadboard model of the LISA phasemeter is currently under development by a Danish-German consortium. The breadboard is build in the frame of an ESA technology development activity to demonstrate the feasibility and readiness of the LISA metrology baseline architecture. This article gives an overview about the breadboard design and its components, including the distribution of key functionalities.

1. Introduction

One of the main building blocks of the LISA metrology system is the frequency distribution and phase measurement system (phasemeter) (Jennrich (2009)). We are currently developing a breadboard model (BB) of the LISA phasemeter in the frame of an ESA technology development activity. The BB will be used to test and validate the functionality and performance as required for the LISA metrology system. We will demonstrate the technological readiness and evaluate a future space qualification. The activity is performed by a consortium composed of the National Space Institute of the Danish Technical University (DTU Space), the Danish industry partner Axcon ApS in Copenhagen, and the Max-Planck Institute for Gravitational Physics, Albert-Einstein Institute (AEI) in Hannover.

This activity is part of a world wide effort to develop and demonstrate the metrology concepts for the LISA interferometry (Spero et al. (2011); Mitryk et al. (2010); Heinzel et al. (2011)). Tests of the full LISA metrology baseline architecture can be performed with the BB. This is achieved by combining the capabilities for phase measurements, Time-Delay interferometry, clocktone transfer, testmass readout, laser control and inter spacecraft communications into a single device.

The BB (figure 1 shows a schematic layout) consists of four types of modules, each containing different functionalities. The main module is the central part of the

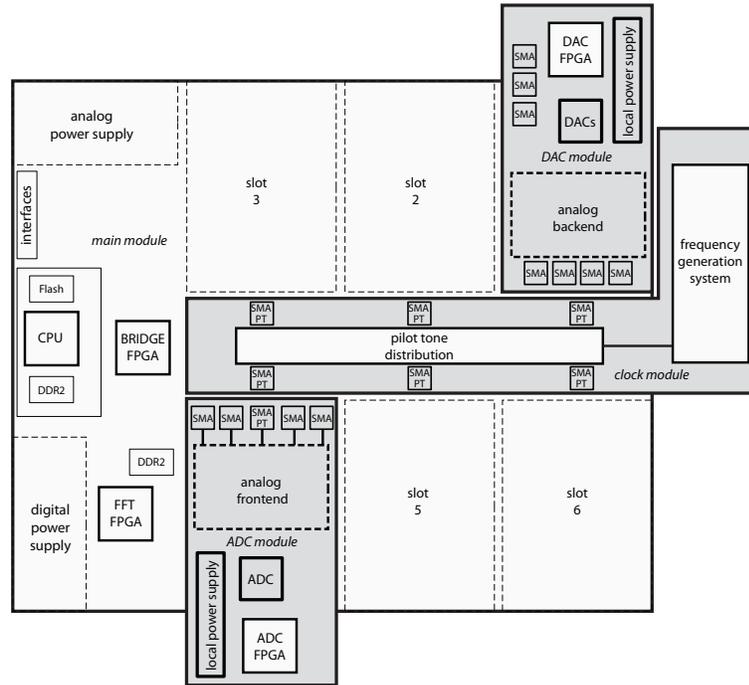


Figure 1. Schematic overview of the LISA phasemeter Breadboard model. The main module carries up to five ADC modules, one DAC module and one clock module. The pilot tone distribution is located in the middle of the BB to shorten its critical path. The FPGAs generating most of the heat in the system are located at the outside, allowing effective cooling and protection of the critical analog circuits.

BB and connects to all other modules and the outside world. One ADC module handles the readout of up to four analog input channels and one BB can carry up to five modules, leading to a total number of 20 input channels. The clock module contains the frequency generation system and the pilot tone distribution. Furthermore each BB carries a DAC module, which produces all analog output signals of the phasemeter. The modular approach was chosen to allow independent testing and optimization of critical components and to reduce production cost and risk. In the following we will give a detailed overview of each module.

2. ADC module

The actual measurement of the incoming signals is implemented on this module. The measurement chain consists of an analog frontend stage, preparing the signal for digitisation, a fast ADC, sampling with 80 MHz, and a FPGA containing the digital system processing. This includes the readout of the signal phase (Shaddock et al. (2006); Bykov et al. (2009)), the readout of inter-satellite ranging and communications (Esteban et al. (2011); Sutton et al. (2010)) and the readout of the clock tone sidebands (Heinzel et al. (2011)).

2.1. Analog frontend

The analog frontend includes a gain stage, an anti-aliasing filter, an addition of a pilot tone for ADC jitter correction and some signal conditioning for the ADC. Preinvestigations have shown that this is one of the most critical components of the BB, therefore we included the possibility of exchanging the frontend by soldering an alternative PCB board on top.

2.2. Digital signal processing

The actual phase readout of the MHz signals is performed by the use of specifically designed phase-locked loops (PLL). Each type of signal tone (science, pilot and side-band) is tracked separately and the computed signals are decimated, downsampled and streamed to the further processing chain. The decimation rates and interface speeds are designed according to the bandwidth requirements of a potential DFACS system and the implementation of a digital laser lock. The readout of the inter-satellite ranging is performed in two delay-locked loops (DLL), which are tracking the local and remote pseudo-random noise (PRN) codes. The received delays and data are also transmitted to the CPU for storage and further processing.

3. DAC Module

The BB will also generate analog signals, which is done on the DAC module. It contains an FPGA, allowing to implement low-level computations and interfacing digital to analog converters and an analog signal conditioning, including additional gains and filtering. One of the main functionality is the generation and data encoding of the PRN signals, necessary for the intersatellite communication and data transfer. We have implemented three PRN outputs, to allow tests in a three laser setup. The other functionality is the generation of control signals for local lasers, to establish the LISA locking scheme. This includes the generation of four analog signals for controlling up to two slave lasers and the implementation of control algorithms in the FPGAs. This can either be the digital equivalent to an analog frequency offset phase-lock (Diekmann et al. (2009); Cruz et al. (2006)), or the implementation of more complex algorithms, like arm-locking (Yu et al. (2011)).

4. Clock Module

The clock module supplies the system clock and the pilot tone to the BB. It either generates or receives two GHz signals with a fixed phase relation to the pilot tone, which are used for the clock tone transfer. It consists of an analog signal chain and is divided into the generation of signals in the Frequency generation section and the distribution of the pilot tone to the ADC modules. The system sampling clock is distributed via the PCB board, while the pilot tone is separated, to ensure its stability. The positioning of the clock module allows to optimize the signal distribution and allows to decrease the influence of strong heat dissipation by the FPGAs. Similar to the analog frontend of the ADC modules this component is a critical factor of the BB. It contains various testing possibilities to ensure the required functionality and performance, as well as its own stabilised power supply.

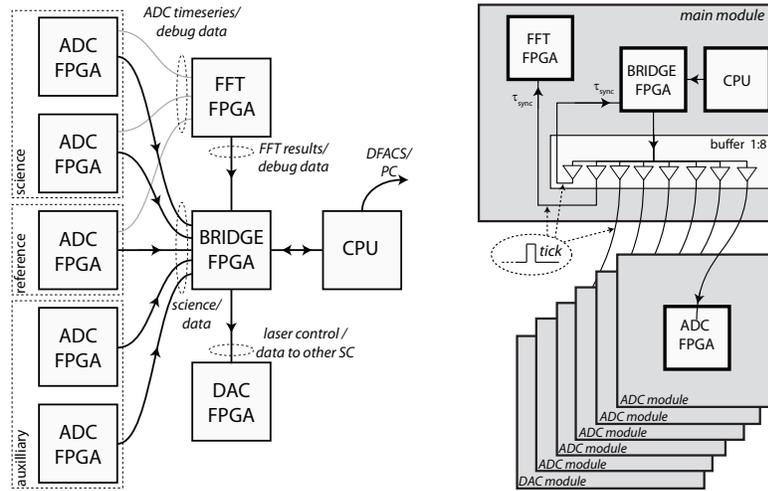


Figure 2. (left) System communication structure. All communication is routed through the bridge FPGA, with the exception of the highspeed data for the FFT FPGA. (right) Time tick distribution in the system via the bridge FPGA. All delays are matched, as well as the clock signals (not shown here), to allow a system wide hardware synchronization.

5. Main Module

Besides the function as baseplate and power supply, the main module contains central parts of the functionality. A separate "Bridge FPGA" is handling the system communication between the different FPGAs and a CPU, which is controlling the BB. A sketch of this is shown in figure 2 (left). The CPU is also performing parts of the digital signal processing, data storage and the potential communication to a DFACS simulator. In addition the main board contains another FPGA, which is dedicated to perform Fast-Fourier Transforms of the incoming signal for lock acquisition procedures.

5.1. Bridge FPGA

The bridge FPGA is the central switch for most communications and is directly interfaced to the CPU, sending data to it and distributing commands from it to the respective submodules. For synchronising the various FPGAs system a time tick can be triggered at the bridge (see figure 2, (right)). This tick is sent to all FPGAs with the same time delay, also back to the bridge. This allows to synchronize clock counters in all systems, as well as any other action to a single clockcycle. Together with the pilot tone correction it forms the basis for meeting the stringent LISA timing requirements necessary for implementing TDI and clock noise corrections.

5.2. FFT FPGA

To ensure a maximum acquisition performance the FFT FPGA can perform four full dutycycle FFTs with the complete ADC timeseries of an ADC module, transmitted by dedicated fast interfaces. It also hosts a peak detection algorithm and the possibility of storing a fullspeed datastream into dedicated DDR RAM. This stream is then read

out via the CPU and can be used to perform debugging and signal analysis for short sequences at the full sampling rate.

5.3. CPU

The CPU will control the BB, perform housekeeping procedures, change operating modes and ensure synchronisation of all submodules. It is also performing several tasks for the digital signal processing. This includes a final data filtering and decimation to prepare the data for the DFACS system or for transmission to ground. The CPU is also handling the data storage and the preparation of data for the inter spacecraft communication.

6. Outlook

After the assembly of the BB, we will perform functionality and performance tests with electronic signals. The performance goals of all subsystems are calculated from the requirement of $1 \text{ pm}/\sqrt{\text{Hz}}$ in the range of 0.1 mHz and 1 Hz with the standard noise shape. Future steps are tests in LISA like optical setups and the evaluation of a design for space qualification.

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