10 Hz and $1\,\mathrm{nm}/\sqrt{\mathrm{Hz}}$ at 1 mHz. A coupling of clock noise into the phase measurement is present and limits the performance in a single reflection zero measurement. An active clock stabilisation via a delay-locked loop allows one to reduce this noise by an order of magnitude at low frequencies.

Future, even faster implementations of this scheme might benefit from dedicated hardware that has less clock jitter between PRN code generation and ADC. A comprehensive analytic or numeric model of the effects of non-ideal modulations and bandwidth limitations will also give a better understanding of the parameters that influence the achievable low frequency performance.

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