

Design of a digital multiradian phase detector and its application in fusion plasma interferometry

A. Mlynek, G. Schramm, H. Eixenberger, G. Sips, K. McCormick,
M. Zilker, K. Behler, J. Eheberg and the ASDEX Upgrade Team
*Max-Planck-Institut für Plasmaphysik,
Garching, Germany*

We discuss the circuit design of a digital multiradian phase detector that measures the phase difference between two 10 kHz square wave TTL signals and provides the result as a binary number. The phase resolution of the circuit is 1/64 period and its dynamic range is 256 periods. This circuit has been developed for fusion plasma interferometry with submillimeter waves on the ASDEX Upgrade tokamak. The results from interferometric density measurement are discussed and compared to those obtained with the previously used phase detectors, especially with respect to the occurrence of phase jumps. It is illustrated that the new phase measurement provides a powerful tool for automatic real-time validation of the measured density, which is important for feedback algorithms that are sensitive to spurious density signals.

I. INTRODUCTION

Precise knowledge and control of the plasma density is of utmost importance when operating a fusion experiment such as the ASDEX Upgrade tokamak. Interferometry provides an accurate measurement of the line-integrated electron density along a given line of sight through the plasma, which is independent of other plasma parameters. When a laser beam (vacuum wavelength λ_0) passes through a plasma with local electron density $n_e(x)$, it experiences a phase shift

$$\varphi = \lambda_0 r_e \int n_e(x) dx \quad (1)$$

relatively to a beam that propagates in vacuum, where r_e is the classical electron radius and the integration variable x is a geometric coordinate along the beam path. This equation also holds for magnetized plasmas when the ordinary direction of polarization is chosen. On many of today's fusion experiments, submillimeter waves are used for interferometry ([1], [2], [3]). On ASDEX Upgrade, a deuterium cyanide (DCN) laser with a wavelength of 195 μm is used. For this wavelength, a phase shift of 2π corresponds to a line-integrated density of $5.72 \cdot 10^{18}$ electrons per square meter. The phase shift φ is measured with a Mach-Zehnder type interferometer with heterodyne detection system. The laser beam is split, one component is focussed on a blazed optical grating that is bent, and mounted on the surface of a rotating cylinder, as described in [4]. As the point where the beam hits the grating has a velocity component in the direction of beam incidence, the diffracted beam experiences a Doppler shift $\Delta\omega$. The second beam is split in 6 components, one acts as reference, whereas five of them enter the plasma vessel at different locations (see figure 1). They cross the plasma, are reflected off in-vessel mirrors attached to the inner column, cross the plasma again, and leave the vessel. Also the frequency shifted beam is split into 6 components, which are combined with the five probe beams leaving the vessel and

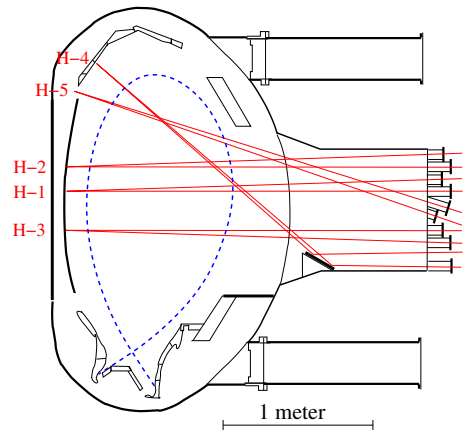


FIG. 1: A cross section of the ASDEX Upgrade vessel, illustrating the 5 lines of sight of the DCN interferometer and the last closed flux surface (dashed line) for a typical plasma discharge. The channels are labeled as 'H-1' to 'H-5'.

with the reference beam in individual detectors. According to the equation

$$\sin(\omega t + \varphi) + \sin((\omega + \Delta\omega)t) = 2 \cdot \sin\left(\frac{2\omega + \Delta\omega}{2}t + \frac{\varphi}{2}\right) \cdot \cos\left(\frac{\Delta\omega}{2}t - \frac{\varphi}{2}\right), \quad (2)$$

which includes a phase shift φ between the two combined beams, a beat signal will be obtained, where the phase of the slowly varying cosine envelope function provides the information on the phase shift between the two combined beams. The detectors do not resolve the fast oscillation given by the sine term on the right hand side of equation (2). By comparing the phase of the detector output of a given line of sight to that of the reference detector, the corresponding line-integrated electron density can be calculated from equation (1). The highest line-integrated densities obtained on ASDEX Upgrade during the flat-top phase are of the order of 10^{20} electrons per square meter, which corresponds to a phase shift of about 20 x

2π . The challenge in submillimeter interferometry therefore is to do multiradian phase detection: Each transition from one period to the next has to be carefully monitored. The measurement is therefore history dependent, as a single measurement at one point in time can only give the phase shift modulo 2π . If an error occurs in measuring the phase shift, a spurious result for the density is obtained. Such counting errors are often referred to as 'phase jumps' or 'fringe jumps' in the literature. In off-line data analysis, it is helpful to check whether the measured phase returns to zero after the end of the discharge. If this is not the case, one has a clear indication for the occurrence of at least one counting error. This is only a sufficient, but not a necessary criterion for a phase jump, as there may be several jumps whose amplitudes sum up to zero. Nevertheless, this criterion allows for quick identification of a large number of phase jumps. In contrast, real-time detection of phase jumps is much more challenging, as this criterion cannot be applied. In this article, we describe a hardware upgrade of the interferometer that opens up new possibilities in real-time phase jump detection.

II. DIGITAL PHASE COUNTER DESIGN

On ASDEX Upgrade, the angular velocity of the rotating grating is adjusted to provide a beat signal frequency of about 10 kHz . This frequency is subject to fluctuations as it is determined by a mechanical system, namely, the compressed air motor that drives the grating. The beat signals obtained at the detector outputs are preamplified and bandpass filtered in order to reject higher and lower frequency noise. Then the relative phase of these signals has to be determined. Various methods for measuring the phase shift between probe and reference signal have been described. Some of them digitize the signals with an analog-to-digital converter (ADC) and calculate the phase with a signal processor [5]. Others use binary counters that count up on a zero crossing of the reference signal and down on a zero crossing of the probe signal [6]. The counter reading is then digitized by a digital-to-analog converter (DAC) and sent through a low-pass filter, resulting in an analog voltage proportional to the phase difference. A further approach [7] uses a phase-locked loop circuit to generate two clock signals that have 128 and 16 times the frequency of the reference signal. A second PLL circuit then keeps the latter signal in a fixed phase relation to the probe signal by adding or omitting pulses. Such additional pulses or missing pulses cause a binary counter to count down or up, respectively, whose output is converted to an analog voltage with a DAC and then low-pass filtered. Such phase counters have been used on ASDEX Upgrade for about ten years.

Here we present our recent design of a fully digital phase detector that delivers two binary numbers, one representing the integer multiples and one the fractions of 2π . The separation of multiples and fractions was a basic de-

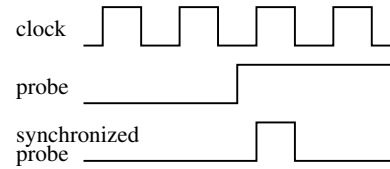


FIG. 2: Signal synchronization to the clock: Only the clock pulse after a rising edge of the probe signal passes through.

sign criterion for this circuit, as the counting of fractions immediately recovers from any perturbation (like temporary loss of the signal), whereas the number of integer multiples may be affected by counting errors after the perturbation and therefore require for correction.

The almost sinusoidal 10 kHz signals after the bandpass filter are sent to comparators, resulting in square wave TTL signals with a 50% duty cycle. A phase locked loop circuit (74HCT4046) is used to generate a square wave signal that has a 64 times this frequency and a fixed phase relation to the reference signal. This 640 kHz signal will be referred to as clock signal in the further discussion. The reference and probe signals are then synchronized to this clock signal. For this purpose, a circuit built up from two D-type flip-flops is used, which receives the clock signal and reference or probe signal as input. It suppresses 63 of the 64 clock signal pulses, only the one clock pulse that follows a rising edge of the input signal passes through (see figure 2). After synchronization, the phase shift between reference and probe signal is discretized to 64 possible steps. The circuit that counts the phase shift is divided in two units: One of them counts the integer multiples of 2π and the other the fractions, with a resolution of $1/64$ of 2π (see figure 3). Both units consist of synchronous binary counters. The counter for the integer multiples is 8 bits long and counts up on a rising edge of the reference signal and down on a rising edge of the probe signal. With short delay after the arrival of the probe signal (just in order to account for gate delays), the counter reading is transferred into an 8-bit latch. If probe and reference signal arrive simultaneously (simultaneity is one out of the 64 discrete states), both pulses are suppressed so that the counter does neither count up nor down, as both at the same time would result in undefined behavior. The counter for the fractions is 6 bits long and counts up on each rising edge of the clock signal. A rising edge of the synchronized reference signal resets the counter to zero, and a rising edge of the probe signal transfers the counter reading into a second latch. That way, the phase difference is available as binary number at the output of the two latches: From one latch, the number of integer multiples of 2π can be read as 8 bit number, i.e. has a dynamic range of 256 fringes, and on the other, the number of fractions in units of $1/64$ of 2π is available as a 6 bit number. The output of the latches is updated shortly after a rising edge of the corresponding probe signal arrives. As the frequency of the input signals is not exactly 10 kHz , the output of the de-

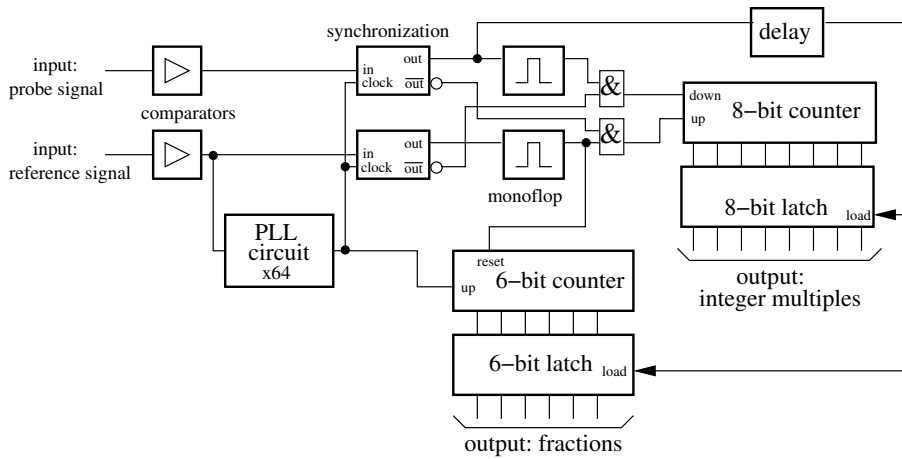


FIG. 3: Block diagram of the digital phase counter.

vice cannot be read at a fixed sampling rate of 10 kHz, as some samples would be lost and some read twice then, depending on the actual velocity of the rotating grating. Therefore, oversampling is required, which is usually performed at 50 kHz. To have an indication whether a result read from the latch has been updated since the last sample, an additional update bit has been introduced. It is set high when a new value has been written to the latch (i.e. shortly after a rising edge of the TTL probe signal) and set back to low after a readout cycle. So on the average, the update bit will be found high in each 5th sample.

There are two ways of interpreting the binary output of this device. One of them is to add both, the number of integer multiples and $1/64$ times the number of fractions. The other approach is to ignore the number of integer multiples and to use the information on fractions only. The number of integer multiples of 2π is then reconstructed by software as follows. Initially, it is set to zero. If the number of fractions decreases by more than $32/64$ in one step, this indicates a transition from one period to the other and the number of integer multiples is incremented by one. Accordingly, it is decremented by one if the number of fractions increases by more than $32/64$ in one step. Evidently, the latter method does not allow for phase changes of more than half a period per time step. This allows us to suppress phase jumps which are induced by signal noise, but may result in counting errors when there are rapid changes in plasma density. The phase resolution of $2\pi/64$ corresponds to a line-integrated density resolution of about $8.9 \cdot 10^{16} m^{-2}$, but phase shifts of this order can also be caused by a displacement of the in-vessel mirrors by about 1.5 micrometers. Vessel movement of this magnitude cannot be avoided when operating the tokamak, therefore, this high phase resolution of the phase counter comes into play only when fast density oscillations are to be investigated, which take place on a shorter time scale than the mechanical vibrations. An example of this, namely, a sawtooth precursor,

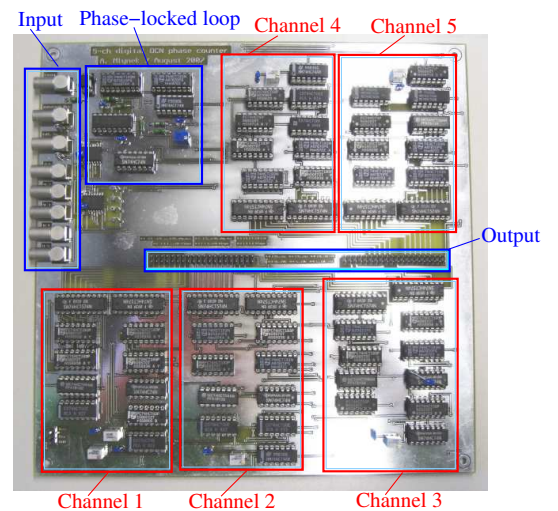


FIG. 4: A photograph of the 5-channel printed-circuit phase counter, built up from 62 discrete ICs.

will be given in the further discussion.

III. HARDWARE IMPLEMENTATIONS

After first tests with a prototype device, two versions of the digital phase detector have been built. The first one was built up with discrete 74HC/HCT series integrated circuits (ICs), see figure 4, and started operation at the end of the 2007 campaign. A single circuit board contained 5 phase counters for the 5 DCN interferometer channels. This allowed us to save components as some subcircuits, like the PLL part, are the same for all 5 channels. The output of this circuit board was connected to a multiplexer which allowed to read the 5 channels one after the other into a local personal computer with a multipurpose digital input-output ports PCI card. Data acquisition with this device revealed a weakness of the

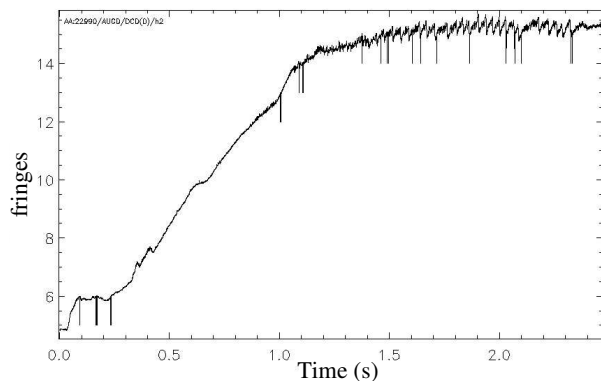


FIG. 5: Time trace of the phase shift for the interferometer channel H-2 in ASDEX Upgrade discharge #22990 as measured by the digital phase counter shown in figure 4. Noise spikes with negative sign and an amplitude of one period often occur when the phase shift is close to an integer multiple of 2π .

circuit, as illustrated in figure 5. When the phase difference between reference and probe signal crosses an integer multiple of 2π , one sometimes observes spikes with an amplitude of -2π . These spikes were removed by software in real-time. After some investigation, the reason for this could be identified: The phase locked loop that generates the clock signal has a slight jitter, due to which each 64th rising edge of the clock signal does not precisely coincide with a rising edge of the reference signal, but comes shortly before or after it. In the case it comes before it, it is possible that there are 64 clock pulses in between two rising edges of the reference signal. If probe and reference signal are almost in phase, this can result in the counter for the fractions of 2π to receive a further "count up" pulse when the counter reading is 63 already. This causes an overflow of the counter, which appears as negative spike in the output signal.

For the 2009 campaign, a second implementation of the phase counter was built that is compatible with the new standard data acquisition hardware on ASDEX Upgrade, which is described in detail in ref. [8]. As the output of the phase counter (including the update bit) is a 15-bit number, it can be easily integrated into the 16-bit backplane bus system. For this implementation of the phase counter, most of the digital circuitry was set on a complex programmable logic device (CPLD), just the PLL circuit is realized by an external IC. That way, two phase counter channels could be set on one standardized plug-in module (see figure 6). The previously mentioned spike problem could be solved by locking the counter for the fractions against further count up pulses when it has reached a counter reading of 63.

This device works reliably since April 2009.



FIG. 6: A photograph of the CPLD based 2-channel phase counter in front of the crate with the 16-bit backplane bus system.

IV. RESULTS

From the digital device, two phase results per channel can be obtained, one of them being based on the entire output, whereas the other uses information on the fractions only and reconstructs the integer multiples by software as described before. Evidently, these two results will only differ by multiples of 2π . In addition, the old phase counters based on the principle proposed in [7] are still operated in parallel, their output is digitized with additional ADCs in the new data acquisition system. That way, 3 signals per interferometer channel are available. Comparison shows that the old phase counters suffer from the low-pass filter in their output stage. Rapid changes of their output signals are delayed by approximately 200-300 microseconds, whereas the new digital devices provide quick response. In addition, the new electronics is capable of detecting fast density oscillations, for example, due to core magnetohydrodynamic activity, which are suppressed by the low-pass filter of the old system. The cutoff frequency of this filter is 4 kHz; it cannot be increased as otherwise, noise from the digital side of the preceding DAC would be present in the output signal. Figure 7 shows the output of new and old phase detector during the precursor oscillations of a sawtooth crash. Only the new device is able to resolve the oscillations.

A slight difference in density scaling of the order of one percent is observed, which is due to gain errors of analog amplifiers in the output stage of the old phase counters and scale errors of the subsequent ADCs. The new digital phase counters avoid these error sources.

The most important feature, however, becomes apparent when there are phase jumps due to perturbation of the probe signal as a result of laser beam refraction in-

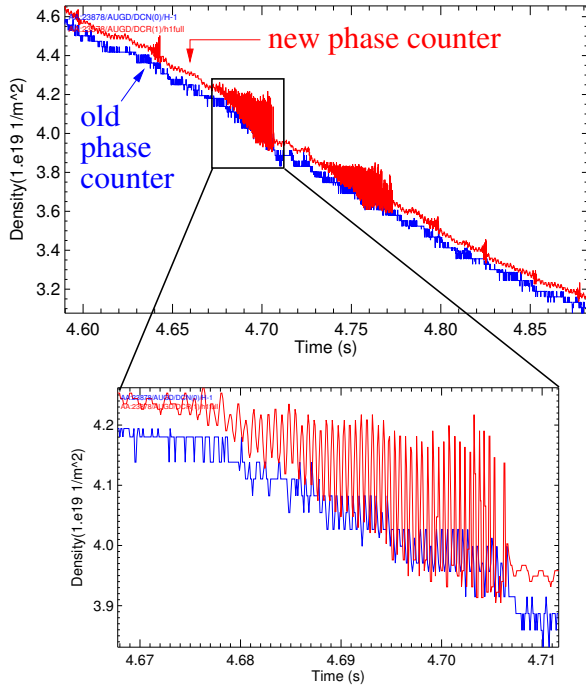


FIG. 7: Behavior of old (blue curve) and new (red curve) phase counter during precursor oscillations of a sawtooth crash. Whereas the oscillation is suppressed by the low-pass filter in the old phase counters, the new digital device can resolve it. The slight vertical offset is due to scaling inaccuracies of the old phase counters, as discussed below.

side the plasma. Such phase jumps can either be caused by plasma phenomena such as edge localized modes or disruptions, or by externally triggered events like pellet injection [9]. In such case, one, two or even all three density signals that are available per channel can suffer from phase jumps. The remarkable point about this, however, is the fact that the amplitude by which the three signals jump is in the vast majority of cases not the same. Figure 8 illustrates a case where all 3 signals for a given channel suffer from phase jumps at the same time, but jump by different multiples of 2π . That way, a very powerful criterion for automatic real-time detection of phase jumps has been identified: The three signals are compared, and only as long as they agree within a small error band, the density signal can be regarded as reliable. As soon as a discrepancy occurs, one has to assume that at least one signal is incorrect due to phase jumps. This validation criterion has been found to be rather restrictive: On the one hand, the probability that a spurious signal is able to pass the validation procedure is rather low. We have analyzed in detail a data set consisting of 841 plasma discharges which represent the full spectrum of discharge scenarios of a typical ASDEX Upgrade experimental campaign. It includes 549 H-mode discharges and 93 shots that were terminated by a disruption. As the

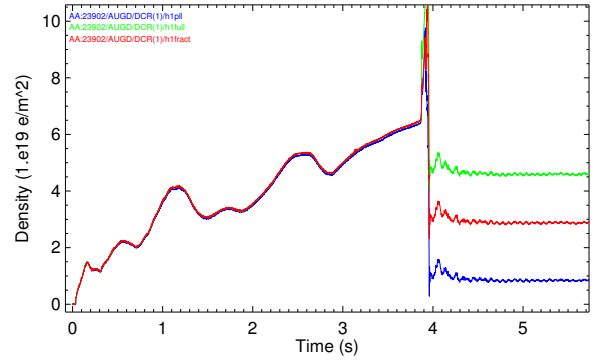


FIG. 8: Comparison of the three density signals that are available for one interferometer channel. In the disruption, there are phase jumps on all 3 signals, however, they have different amplitudes. The disagreement of the 3 signals clearly indicates the occurrence of phase jumps.

DCN interferometer has 5 channels, this data set provides a total of 4205 time traces. Among them, we have identified only 21 time traces in which phase jumps with the same amplitude occurred simultaneously on all three signals and therefore passed the validation algorithm. All other jumps, however, have been reliably detected. In 17 out of those 21 cases, the phase jump occurred during a disruption. We therefore conclude that the likelihood of having overlooked phase jumps in a validated density measurement until the end of the useful flat-top phase of a discharge is very low, as we observed only 4 such events within a data set containing 4205 time traces. On the other hand, when the validation criterion is violated, the output of one or two of the three phase detection schemes may still represent the true plasma density. For the old phase detectors, the maximum detectable phase change per time is limited due to the properties of the PLL circuit [7]. This makes them rather stable in the presence of modes in the plasma, but favors fringe loss when there are fast changes in the plasma density, like in case of pellet injection. The signal based on the full output of the digital phase detector provides faster response. Accordingly, a range of pellet sizes exists for which the old phase counters regularly suffer from fringe loss, whereas the new ones can properly resolve the short phases of rising density. However, the likelihood of having phase jumps during a phase with mode activity is higher for the new electronics. We expect that this problem can be mitigated by introducing a more advanced comparator on the input side, like the dual-threshold comparator presented in [10]. So far, only the digital part has been optimized.

Some real-time control algorithms are sensitive to spurious density measurements, like the density feedback loop that controls the gas valves and the low-density interlock of the heating systems. An incorrect density input may cause a plasma disruption. For these applications,

it is important to have a reliable validation criterion for the measured density. When this criterion is no longer fulfilled for a given interferometer channel, a different channel of the DCN system or one of the vertical CO_2 interferometer has to be used instead.

V. OUTLOOK

A fast algorithm for real-time calculation of the plasma density profile has been developed and installed on the computer that performs the density validation. As a phase jump on only one interferometer channel can significantly distort the resulting density profile, it is important to use only validated density signals for this application. As soon as one channel violates the validation criterion, the calculated density profile is labeled as invalid. On this basis, active feedback control of the profile shape has recently been demonstrated. Further applications such as real-time ray tracing, which allows us to predict the deposition region of the electron cyclotron resonance heating as a function of the launcher angle,

are in preparation.

The new electronics also opens up new possibilities in off-line data analysis. The fast response of the new phase counters is an essential property when density profiles are calculated with high temporal resolution via integrated data analysis from the data of different diagnostics [11]. The delay due to the low-pass filtering in the old electronics set a lower limit of some hundreds of microseconds up until now when including interferometry data into analysis.

In [10], an approach for automatic phase jump correction is described which is based on setting upper and lower limits to the time delay between two rising edges in the digitized probe signal. When the next rising edge occurs outside this plausible time window, correction is performed. As the information on the time of arrival of the rising edges in the probe signal is still present in the output of the digital phase counter in form of the update bit, this method of correction could most likely be implemented on the ASDEX Upgrade interferometer in the near future just by modifying the software used for the real-time data interpretation.

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